

# **JEDEC STANDARD**

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## **DDR5MDB02 Multiplexed Rank Data Buffer**

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**JEDEC SOLID STATE TECHNOLOGY ASSOCIATION**



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## DDR5MDB02 Multiplexed Rank Data Buffer

(From JEDEC Board Ballot JCB-26-06, formulated under the cognizance of the JC-40.4 subcommittee on Registered and Fully Buffered Memory Support Logic, item 708.99H).

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### 1 Scope

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This standard defines standard specifications for features and functionality, DC and AC interface parameters and test loading for definition of the DDR5MDB02 data buffer for driving DQ and DQS nets on DDR5 MRDIMM applications.

The purpose is to provide a standard for the DDR5MDB02 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE: The designation DDR5MDB02 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

This document uses DDR5MDB02, DDR5MDB, Data Buffer, MDB, or Buffer interchangeably throughout for the DDR5MDB02 device naming.

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### 2 Mechanical Outline

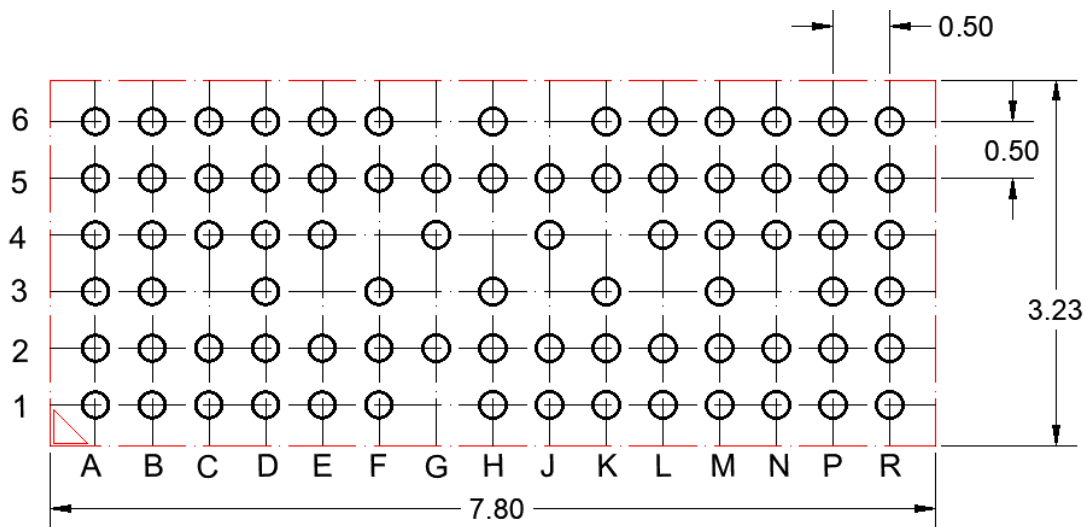
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The DDR5MDB02 Package is a 78-ball Fine-Pitch BGA (FBGA) with 0.5 mm ball pitch, 15 x 6 grid with 12 balls depopulated, and 7.8 mm x 3.23 mm as defined in MO-276<sup>1</sup>. The device pinout options support the register link inputs in the center columns to support signal routing matching from alternate sides of the DIMM to the DDR5MRCD02. Corresponding Host side data/strobe balls are placed in a way to match the corresponding pin location on the connector if the device is mounted on the backside of the module. Each VDD and VSS is located close to an associated no ball position to allow low-cost via technology combined with the small 0.50 mm ball pitch.

---

1. This variation defines a nominal package thickness of 0.90 mm with tolerance of +/- 0.1 mm.

## 2 Mechanical Outline (cont'd)



Recommended PCB footprint

Figure 1 — 78 Ball Configuration 15 x 6 (TOP VIEW)

Ball pitch: 0.50 mm x 0.50 mm, Size ( $\varnothing$  0.3 mm), SMD Pad SRO ( $\varnothing$  0.275 mm), X-ray view from topside

### 2.1 Pinout 15 x 6

Table 1 specifies the pinout for the DDR5MDB02. The device has (mostly) symmetric pinout with Host interface at the south side and DRAM interface at the north side.

Table 1 — Ball Assignment -78 ball FBGA, 15 x 6 Grid, TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
6	A_MDQ7	A_MDQ5	A_MDQ6	A_MDQ4	A_MD-QS1_t	A_MD-QS1_c		BCOM1		A_MD-QS0_t	A_MD-QS0_c	A_MDQ3	A_MDQ1	A_MDQ2	A_MDQ0
5	VSS	VSS	VSS	VSS	B_MD-QS1_t	B_MD-QS1_c	BCOM0	VSS	BCOM2	B_MD-QS0_t	B_MD-QS0_c	VSS	VSS	VSS	VSS
4	B_MDQ7	B_MDQ5	B_MDQ6	B_MDQ4	VSS		VSS		VSS		VSS	B_MDQ3	B_MDQ1	B_MDQ2	B_MDQ0
3	ZQCAL	VDD		VDD		VDD		VDD		VDD		VDD		VDD	BRST_n
2	VSS	DQ5	VSS	DQ4	VSS	VSS	BCS_n	BCK_t	LBTXDQ	VSS	VSS	DQ3	VSS	DQ2	VSS
1	DQ7	VSS	DQ6	VSS	DQS1_t	DQS1_c		BCK_c	LBTXDQ	DQS0_c	DQS0_t	VSS	DQ1	VSS	DQ0

## 2.2 Terminal Functions for 78-Ball Data Buffer Package Configuration

**Table 2 — Terminal Functions for 78-Ball Package Configuration**

Signal Group	Signal Name	Type	Description
Data buffer control inputs	BCS_n	POD $V_{REF}$ based <sup>1</sup>	Chip Select Input
	BRST_n	CMOS	Level Triggered Reset, when BCOM is '000' or '111' resets device to default values, otherwise used for BCOM Strap mode defined in Chapter 6, "BCOM Training Mode (BCOMTM) - Data Buffer Interface,"
	BCOM[2:0]	POD $V_{REF}$ based <sup>1</sup>	Register communication bus for data buffer programming and control access
Clock inputs	BCK_t, BCK_c	POD differential	Differential clock input pair
Host Interface	DQ[3:0] DQ[7:4]	POD $V_{REF}$ based bidirectional	Host side data lower nibble Host side data upper nibble
	DQS0_t DQS0_c DQS1_t DQS1_c	POD differential bidirectional	Host side data strobe for lower nibble Host side data strobe complement for lower nibble Host side data strobe for upper nibble Host side data strobe complement for upper nibble When DQ Bus CRC feature is enabled, DQS1_t/c signals are used as CRC data.
DRAM Interface	A_MDQ[3:0] A_MDQ[7:4]	POD $V_{REF}$ based bidirectional	x4 Mode DRAM side data for PS0 or {Rank0, Rank1} group lower nibble DRAM side data for PS0 or {Rank0, Rank1} group upper nibble x8 Mode DRAM side data byte for PS0 or {Rank0, Rank1} group
	B_MDQ[3:0] B_MDQ[7:4]	POD $V_{REF}$ based bidirectional	x4 Mode DRAM side data for PS1 or {Rank2, Rank3} group lower nibble DRAM side data for PS1 or {Rank2, Rank3} group upper nibble x8 Mode DRAM side data byte for PS1 or {Rank2, Rank3} group
	A_MDQS0_t A_MDQS0_c	POD differential bidirectional	x4 Mode DRAM side data strobe for PS0 or {Rank0, Rank1} group lower nibble DRAM side data strobe complement for PS0 or {Rank0, Rank1} group lower nibble x8 Mode DRAM side data strobe for PS0 or {Rank0, Rank1} group data byte

**Table 2 — Terminal Functions for 78-Ball Package Configuration (cont'd)**

Signal Group	Signal Name	Type	Description
DRAM Interface (cont'd)	A_MDQS1_t A_MDQS1_c	POD differential bidirectional	x4 Mode DRAM side data strobe for PS0 or {Rank0, Rank1} group upper nibble DRAM side data strobe complement for PS0 or {Rank0, Rank1} group upper nibble x8 Mode Not Used
	B_MDQS0_t B_MDQS0_c	POD differential bidirectional	x4 Mode DRAM side data strobe for PS1 or {Rank2, Rank3} group lower nibble DRAM side data strobe complement for PS1 or {Rank2, Rank3} group lower nibble x8 Mode DRAM side data strobe for PS1 or {Rank2, Rank3} group data byte
	B_MDQS1_t B_MDQS1_c	POD differential bidirectional	x4 Mode DRAM side data strobe for PS1 or {Rank2, Rank3} group upper nibble DRAM side data strobe complement for PS1 or {Rank2, Rank3} group upper nibble x8 Mode Not Used
Loopback	LBTXDQ LBTXDQS	POD	Loopback DQ Transmit Loopback DQS Transmit
Miscellaneous pins	V <sub>DD</sub>	Power Input	Power supply voltage
	V <sub>SS</sub>	Ground Input	Ground
	ZQCAL	Reference	Reference pin for driver calibration

NOTE 1 These receivers use the internal BVref as the switching point reference.

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## 3 Device Description and Features

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### 3.1 Description

This dual 4-bit bidirectional data register with differential strobes is designed for 1.1 V,  $V_{DD}$  operation. The device has a dual nibble Host bus interface that is connected to a memory controller. For the DRAM interface it will be configurable, to two nibbles for x4 DRAMS, or one byte for x8 DRAMS. It also has an input-only control bus interface that is connected to the DDR5MRCD02.

The following two parameters are defined as the timing reference of the MDB interface signals:

- $t_{BCK}$ , representing the period of the input clock BCK, is used for the BCK/BCS/BCOM signals and the MDQS/MDQ signals.
- $t_{HDQS}$ , representing the virtual period or 2UI time of the DQS, is used for the DQS/DQ signals. In Mux mode,  $t_{HDQS} = t_{BCK}/2$ ; In Rank mode,  $t_{HDQS} = t_{BCK}$ .

#### 3.1.1 Data Bus Operation

The clock inputs BCK\_t and BCK\_c are used to sample the control inputs BCS\_n and BCOM[2:0]. The BCOM[2:0] inputs are used to write device internal control registers. The buffer control word (RW) mechanism is described in more detail in Chapter 11, “Control Words,”. BCK\_t, BCK\_c, BCS\_n and BCOM[2:0] signals are terminated to VDDQ on the DDR5 MRDIMM.

All DQ inputs are pseudo-differential with an internal voltage reference. All DQ outputs are  $V_{DD}$  terminated drivers optimized to drive single or dual terminated traces in MRDIMM applications. The differential DQS strobes are used to sample the DQ inputs and are regenerated in the DDR5MDB02 for driving out the DQ outputs on the opposite side of the device. When Host interface is configured in x8 mode, only DQS0\_t/c is used as the strobe pair.

The DDR5MDB02 also supports a dedicated pin for ZQ calibration.

#### 3.1.2 Host Interface Strobe Modes

##### 3.1.2.1 Byte Mode

The MDB02 supports Byte Mode on the Host interface at speed greater than or equal to 8.0 GT/s; i.e., using only DQS0\_t/c as the strobe between the Host and the MDB02. DQS1\_t/c signals are reserved for differential CRC signals when CRC checking function is enabled. The CRC checking function is only supported at speed greater than or equal to 8.8 GT/s. By default, CRC checking function is disabled. The CRC checking function is enabled via PG[70]RWE0[3:2].

##### 3.1.2.2 Nibble Mode

The MDB02 supports Nibble Mode on the Host interface at speed less than or equal to 8.8 GT/s; i.e., DQS0\_t/c and DQS1\_t/c are always used as data strobe between the Host and the MDB02. The CRC checking function is not supported. By default, CRC checking function is disabled.

### 3.2 Data Path Operation in Mux Mode

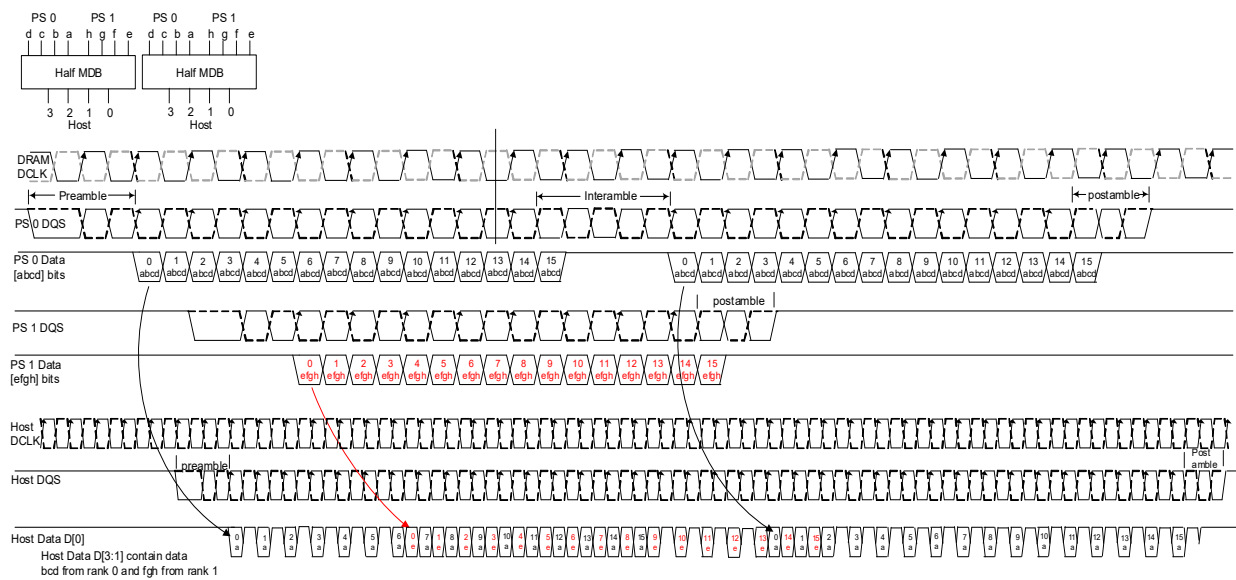
The two pseudo-channels cannot be transferring data in opposite directions at the same time as they share data and strobe signals on the Host side. It is the Host controller's responsibility to provide proper turnaround times based on the last pseudo-channel transferring in one direction to the first pseudo-channel transferring in the other direction.

When transferring data, the data offset between pseudo-channels can be any number of DRAM clocks. They may start on the same DRAM clock, be offset by 1, 2, 3, etc. clocks from each other with either starting first. One pseudo-channel may be transferring data without the other transferring any data at all.



### 3.2 Data Path Operation in Mux Mode (cont'd)

**Figure 4** shows read operations on the two pseudo-channels of a sub-channel. PS 0 begins its transfer 3 DRAM clocks before PS 1. The two pseudo-channels are interleaved on the data bus on a UI basis, with PS0 transferring on the first (even UI) followed by PS1 (odd UI). When only one of the pseudo-channels are transferring data, the other pseudo channel's bit positions will be high. The strobes are common to the two pseudo-channels. The preamble begins when the first pseudo-channel transfers data. When PS0 completes its transfer, PS 1 is still transferring, so the strobes continue to toggle. Effectively the strobes are the OR of data being transferred on either pseudo-channel. The postamble will appear at the end of a pseudo-channel transfer while the other pseudo-channel is not transferring, or when both end at the same time. All interambles have the same rules as for the DDR5 DRAMs, with the gaps defined as the time when NEITHER pseudo-channel is transferring.



**Figure 4 — Interambles in Mux Mode**

#### 3.2.1 DRAM Interface x4 Mode Operation in Mux Mode

The Data Buffer does support x4 mode on the DRAM interface, requiring the data buffers to use a single strobe pair for each nibble of the data, configured in [PG70RWF0\[0\]](#). MDQS[0] is used for lower nibble and MDQS[1] is used for upper nibble when the MDB is connected to x4 DRAMs.

The MDQS[1:0] strobes will remain at the MDQS\_RTT\_Park termination value except when terminations are disabled due to self refresh, or when driving data during writes.

### 3.2.1 DRAM Interface x4 Mode Operation in Mux Mode (cont'd)

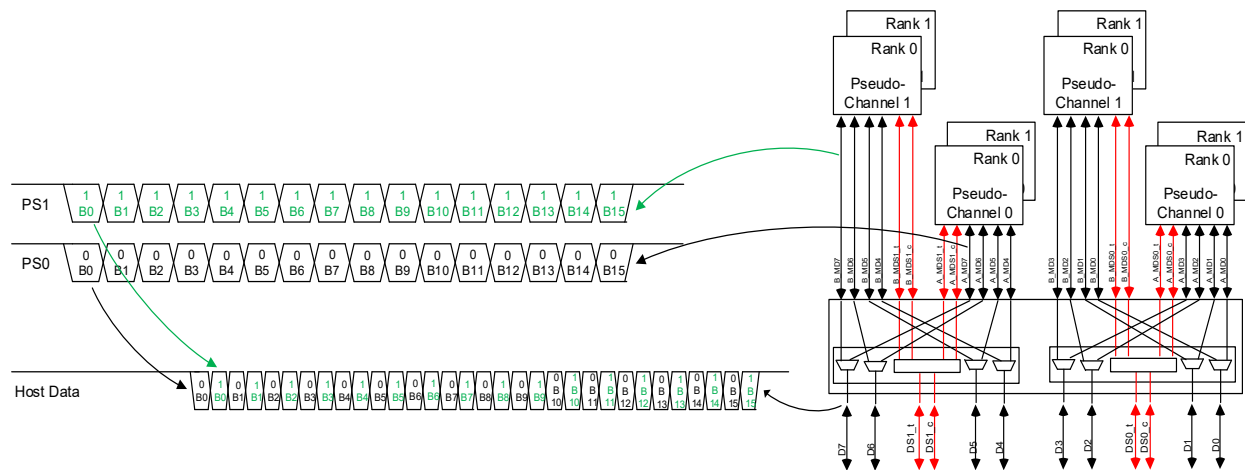


Figure 5 — MDB x4 Mux Mode

### 3.2.2 DRAM Interface x8 Mode Operation in Mux Mode

The Data Buffer does support x8 mode on the DRAM interface, requiring the data buffers to use a single strobe pair for both nibbles of the data. MDQS[0] is used with x8 DRAMs, with MDQS[1] disconnected configured in [PG70RWF0\[0\]](#). The MDQS[0] strobes are used for both lower and upper nibbles. The MDQS[1] strobes will remain at the MDQS\_RTT\_Park termination value at all times when in the x8 mode except when terminations are disabled due to self refresh. The MDQS[1] strobes are NOT driven during writes in this mode.

The diagram below shows the strobe connections and schematic level internal routing in the data buffer.

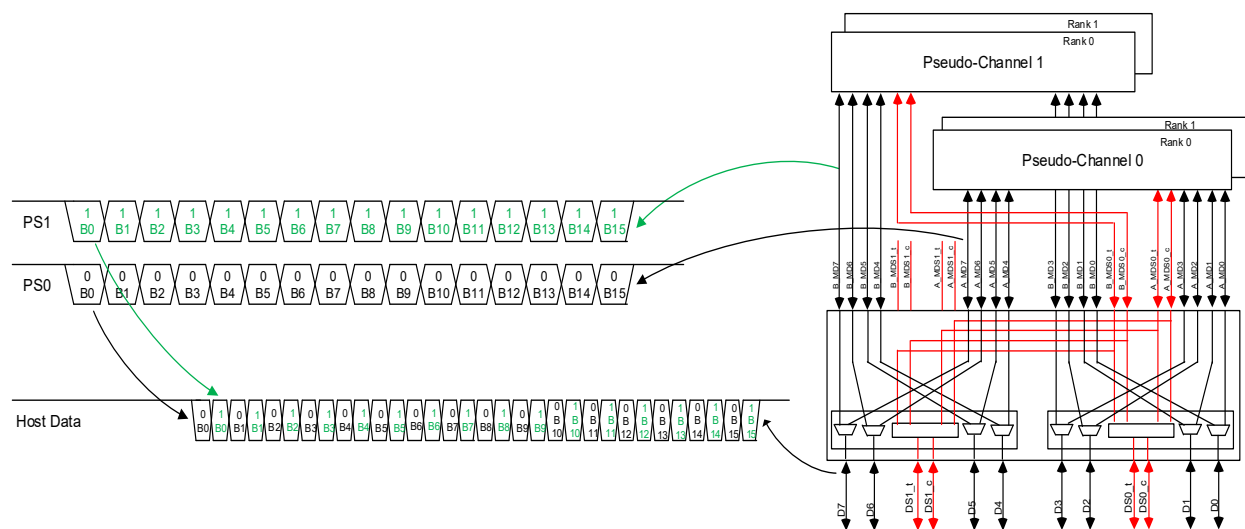


Figure 6 — MDB x8 Mux Mode

Note: The timing registers in [PG\[1:0\]](#) and [PG\[73:72\]](#) of the register space are still independent per nibble when the x8 strobes are used.

### 3.2.3 Supported Operation Combinations in Mux Mode

**Table 3 — Supported Operation Combinations in Mux Mode**

System Parameter	Units	Values						
Host Interface Bit Rate	MT/s	12800	12000	11200	10400	9600	8800	8000
DRAM Interface Bit Rate	MT/s	6400	6000	5600	5200	4800	4400	4000
Supported CAS Latency	tBCK	52,56	48,54	46,50	42,46	40,42	36,40	32,36
Host Interface Write Preamble	tHDQS	5,6,7	5,6,7	5,6,7	4,5,6	4,5,6	4,5,6	3,4,5
Host Interface Write Postamble	tHDQS	1.5	1.5	1.5	1.5	0.5,1.5	0.5,1.5	0.5,1.5
Host Interface Read Preamble	tHDQS	6,7,8	6,7,8	6,7,8	4,5,6	4,5,6	4,5,6	3,4,5
Host Interface Read Postamble	tHDQS	1.5	1.5	1.5	1.5	0.5,1.5	0.5,1.5	0.5,1.5
DRAM Interface Write Preamble	tBCK	3,4	3,4	3,4	3,4	2,3,4	2,3,4	2,3,4
DRAM Interface Write Postamble	tBCK	1.5	1.5	1.5	1.5	0.5,1.5	0.5,1.5	0.5,1.5
DRAM Interface Read Preamble	tBCK	3,4	3,4	3,4	3	2,3	2,3	2,3
DRAM Interface Read Postamble	tBCK	1.5	1.5	1.5	1.5	0.5,1.5	0.5,1.5	0.5,1.5
DWL range Integer Part <sup>1,2</sup>	tBCK	+/-4	+/-4	+/-4	+/-4	+/-4	+/-4	+/-4
MRE range Integer Part <sup>3,2</sup>	tBCK	+/-4	+/-4	+/-4	+/-4	+/-4	+/-4	+/-4

NOTE 1 The spread between the min and max settings across all ranks, nibbles, and pseudo-channels is limited by tWR<sub>-</sub>VAR.

NOTE 2 The MDB supports the full range of -7 to 7 tBCK. Raw Cards A, B, C, D, and E were evaluated to calculate the values in the table. Range values of +/-5, +/-6, and +/-7 are not subject to production testing but are guaranteed by design.

NOTE 3 The spread between the min and max settings across all ranks, nibbles, and pseudo-channels is limited by tRD<sub>-</sub>VAR.

## 3.3 Data Path Operation in Rank Mode

In Rank mode, the Data Buffer supports either x4 mode or x8 mode at the DRAM interface. The DRAM interface x4 or x8 mode is configured in [PG70RWF0\[0\]](#). The Host interface supports x4 mode only as configured in [PG70RWF0\[1\]](#). During normal read or write operations, only one of the four ranks at the DRAM interface is allowed to transfer data with the Host interface.

### 3.3.1 DRAM Interface x4 Mode Operation in Rank Mode

The Data Buffer does support x4 mode on the DRAM interface, requiring the data buffers to use a single strobe pair for each nibble of the data, configured in [PG70RWF0\[0\]](#). MDQS[0] is used for lower nibble and MDQS[1] is used for upper nibble when the MDB is connected to x4 DRAMs.

The MDQS[1:0] strobes will remain at the MDQS\_RTT\_Park termination value except when terminations are disabled due to self refresh, or when driving data during writes.

### 3.3.1 DRAM Interface x4 Mode Operation in Rank Mode (cont'd)

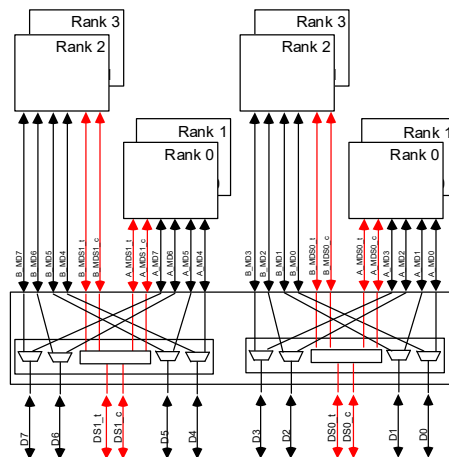


Figure 7 — MDB x4 Rank Mode

### 3.3.2 DRAM Interface x8 Mode Operation in Rank Mode

The Data Buffer does support x8 mode on the DRAM interface, requiring the data buffers to use a single strobe pair for both nibbles of the data. MDQS[0] is used with x8 DRAMs, with MDQS[1] disconnected configured in [PG70RWF0\[0\]](#). The MDQS[0] strobes are used for both lower and upper nibbles. The MDQS[1] strobes will remain at the MDQS\_RTT\_Park termination value at all times when in the x8 mode except when terminations are disabled due to self refresh. The MDQS[1] strobes are NOT driven during writes in this mode.

The diagram below shows the strobe connections and schematic level internal routing in the data buffer.

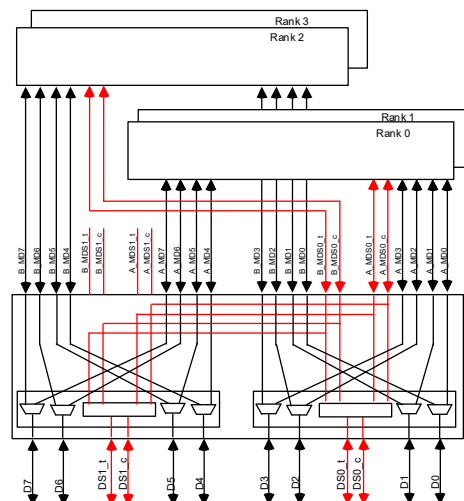


Figure 8 — MDB x8 Rank Mode

Note: The timing registers in [PG\[1:0\]](#) and [PG\[73:72\]](#) of the register space are still independent per nibble when the x8 strobes are used.

### 3.3.3 Supported Operation Combinations in Rank Mode

**Table 4 — Supported Operation Combinations in Rank Mode**

System Parameter	Units	Values			
Bit Rate	MT/s	6400	6000	5600	5200
Supported CAS Latency	tBCK	52,56	48,54	46,50	42,46
Host Interface Write Preamble	tHDQS	3,4	3,4	3,4	3,4
Host Interface Write Postamble	tHDQS	1.5	1.5	1.5	1.5
Host Interface Read Preamble	tHDQS	3,4	3,4	3,4	3,4
Host Interface Read Postamble	tHDQS	1.5	1.5	1.5	1.5
DRAM Interface Write Preamble	tBCK	3,4	3,4	3,4	3,4
DRAM Interface Write Postamble	tBCK	1.5	1.5	1.5	1.5
DRAM Interface Read Preamble	tBCK	3,4	3,4	3,4	3
DRAM Interface Read Postamble	tBCK	1.5	1.5	1.5	1.5
DWL range Integer Part <sup>1,2</sup>	tBCK	+/-4	+/-4	+/-4	+/-4
MRE range Integer Part <sup>3,2</sup>	tBCK	+/-4	+/-4	+/-4	+/-4

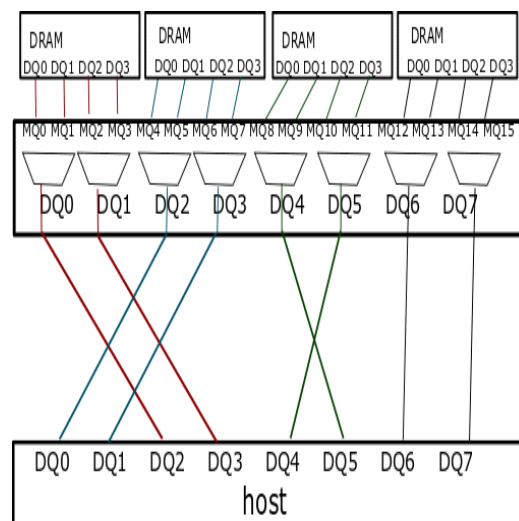
NOTE 1 The spread between the min and max settings across all ranks, nibbles, and pseudo-channels is limited by tWR\_VAR.

NOTE 2 The MDB supports the full range of -7 to 7 tBCK. Raw Cards A, B, C, D & E were evaluated to calculate the values in the table. Range values of +/-5, +/-6, and +/-7 are not subject to production testing but are guaranteed by design.

NOTE 3 The spread between the min and max settings across all ranks, nibbles, and pseudo-channels is limited by tRD\_VAR.

### 3.4 Early Swizzle Discovery

The MDB supports early swizzle discovery, prior to QCS training. A Control Word is added to drive a static value to the Host on each DQ pin. The DQS pins do not toggle in this mode. This mode allows a 0 to be walked through the bits to discover the Host to data buffer swizzle.



**Figure 9 — Swizzle Discovery**

PG[70]RWE4[1] enables Swizzle Discovery Static Mode, which is used to enable driving DQ pin with a static value for Swizzle Discovery Static Mode.

PG[70]RWE6 is used to select the static value of each DQ when Swizzle Discovery Static Mode is enabled.

### 3.5 Power-on Initialization

To ensure defined outputs from the register before a stable clock has been supplied, the memory buffer must enter the reset state during power-up. After the voltage ramp, stable power is held for a minimum of  $t_{RINIT1}$  in the Power-on RESET state. During this time, a static value of  $BCOM[2] = BCOM[1] = BCOM[0] = \text{HIGH}$  or  $\text{LOW}$  shall be applied to ensure Normal Operation RESET. In addition to  $t_{RINIT1}$ ,  $t_{Strap\_Hold}$  also applies (see Table 246). In the Power-on RESET state all Strobe and Data input receivers are disabled and can be left floating. In the Power-on RESET state, all control registers are restored to their default states (which is “0”, except when explicitly defined otherwise). All Strobe and Data outputs must float. In the Power-on RESET state the data buffer is in low-power state and Host interface and DRAM interface ODT terminations are disabled.

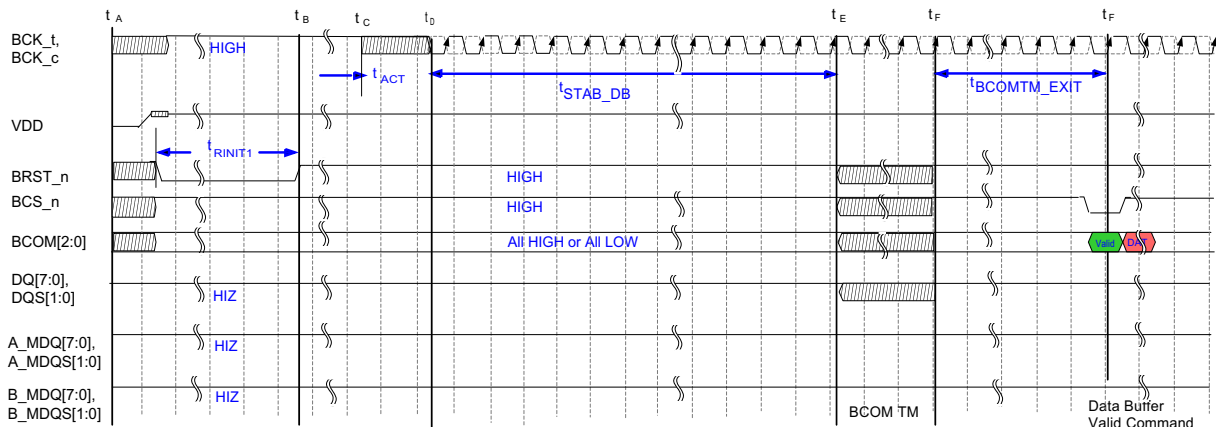


Figure 10 — Data Buffer Initialization Sequence

#### 3.5.1 Clock Stabilization Time $t_{STAB\_DB}$

During PLL stabilization time  $t_{STAB\_DB}$  the data buffer is not fully operational. To ensure correct operation, some rules apply to the inputs of the buffer:

- $BCS\_n$  must remain HIGH.

These rules apply to any instance where stabilization time  $t_{STAB\_DB}$  is required:

- Exit from Reset state
- Exit from clock stop power down
- Changing clocking related registers

Since the data buffer has not reached a stable state the termination on the Host interface will be undefined before the end of the stabilization time.

After reset and after the stabilization time ( $t_{STAB\_DBDATA}$ ) the MDB must meet the input setup and hold specification, as well as accept and transfer input signals to the corresponding outputs.

BCOM VREF and Command Timing settings are set through a Static mode defined in the BCOM Training section.

### 3.5.2 Reset Initialization with Stable Power

The timing diagram in Figure 11 depicts the initialization sequence with stable power and clock. For this sequence, the BCK continues toggling with stable phase and frequency. The data buffer remains in the RESET state for a minimum of  $t_{RINIT1}$ . During this time, a static value of  $BCOM[2] = BCOM[1] = BCOM[0] = \text{HIGH}$  or  $\text{LOW}$  shall be applied to ensure Normal Operation RESET. In addition to  $t_{RINIT1}$ ,  $t_{Strap\_Setup}$  and  $t_{Strap\_Hold}$  also apply (see Table 246). In the RESET state, all non-sticky control registers are restored to their default states.

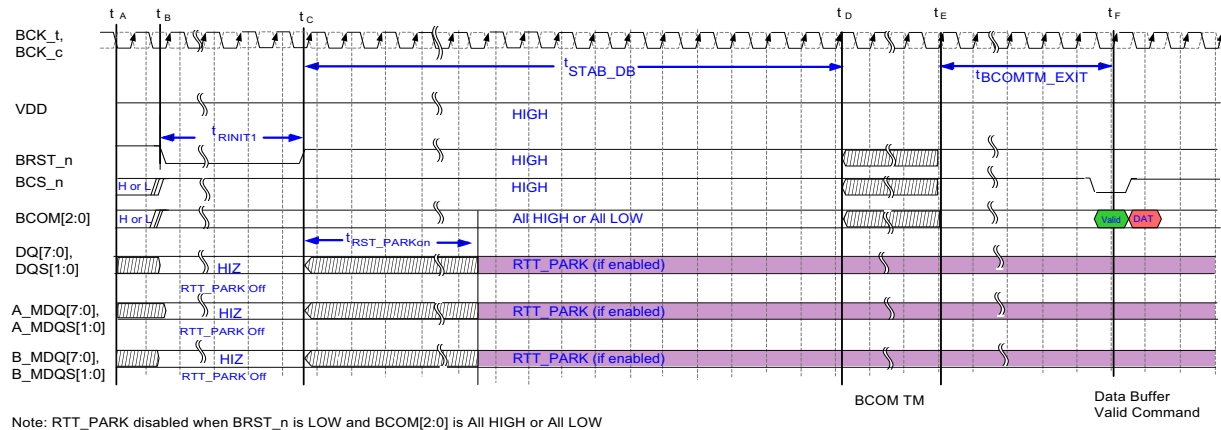


Figure 11 — Data Buffer Reset with Stable Power and Clock

Figure 11 depicts the initialization sequence with stable power and stopped clock. For this sequence, the BCK clock is allowed to stop (i.e.,  $BCK\_t = BCK\_c = \text{HIGH}$ ). The data buffer remains in the RESET state for a minimum of  $t_{RINIT1}$ . During this time, a static value of  $BCOM[2] = BCOM[1] = BCOM[0] = \text{HIGH}$  or  $\text{LOW}$  shall be applied to ensure Normal Operation RESET. In addition to  $t_{RINIT1}$ ,  $t_{Strap\_Setup}$  and  $t_{Strap\_Hold}$  also apply (see Table 246). In the RESET state, all non-sticky control registers are restored to their default states.

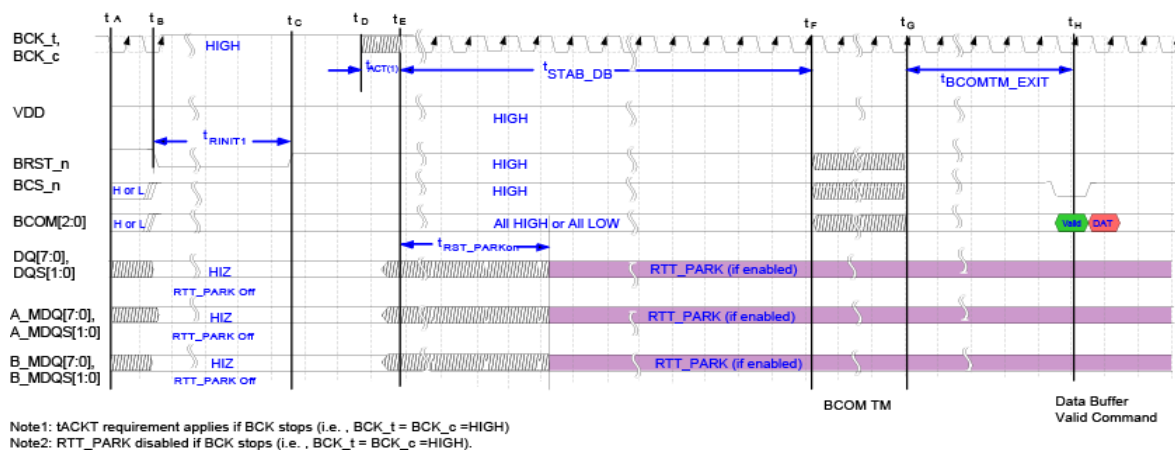


Figure 12 — Data Buffer Reset with Stable Power and Stopped Clock

### 3.6 Transparent Mode

Transparent mode is enabled in the DDR5MDB02 by setting [RW82\[0\]](#) to 1. While in transparent mode, the MDB does not interpret BCS\_n and BCOM commands as defined in Table 17. For BCS\_n input value of “1” and BCOM[2:0] input values of “111” it directs the data flow from Host interface to DRAM interface, and it enables or disables the on-die termination at the Host interface based on the setting in [RW82\[1\]](#). For BCS\_n input value of “1” and BCOM[2:0] input values of “000”, the Data Buffer directs the data flow from DRAM interface to Host interface and it enables or disables the on-die termination at the DRAM interface based on the setting in [RW82\[1\]](#). Any other input values of BCS\_n and BCOM[2:0] are invalid.

The Data Buffer does not support high-speed changes in direction of data flow. The Host will wait for 32 clock cycles of settling time after the direction in data flow is reversed in transparent mode.

In Mux mode, when the write direction is selected, DQ/DQS are broadcast to MDQ/MDQS of both PS0 and PS1. When the read direction is selected, the data flow from MDQS to DQS is controlled by [PG\[70\]RWE4\[2\]](#), and the data flow from MDQ to DQ is controlled by [PG\[70\]RWE4](#) and [PG\[70\]RWE5](#). When [PG\[70\]RWE4\[0\] = 1](#) the DQ Static Mux Mode for DQ Pass Through and Transparent modes is enabled, the pseudo channel can be selected for each DQs in [PG\[70\]RWE5\[7:0\]](#). When [PG\[70\]RWE4\[0\] = 0](#) the DQ Static Mux Mode for DQ Pass Through and Transparent modes is disabled, DQ Pass through mode and transparent mode PS selection is determined by [PG\[70\]RWE4\[2\]](#) and applies to all DQ bits.

In Mux mode with the DQ Bus CRC function enabled, when transparent mode is entered with read direction selected, DQS1\_t and DQS1\_c will be driven to both HIGH or differential HIGH by the MDB.

In Rank mode, when the write direction is selected, DQ/DQS are broadcast to MDQ/MDQS of both A and B ports. When the read direction is selected, the data flow from MDQ/MDQS to DQ/DQS is controlled by [PG\[60\]RWE4\[0\]](#). When [PG\[60\]RWE4\[0\] = 0](#), the A\_MDQS and A\_MDQ interface signals are selected for the data flow to the Host interface. When [PG\[60\]RWE4\[0\] = 1](#), the B\_MDQS and B\_MDQ interface signals are selected for the data flow to the Host interface.

When forwarding from a x8 interface to a x4 interface, the single strobe on the x8 interface will be forwarded to both strobes on the x4 interface. When forwarding from a x4 interface to a x8 interface, the upper strobe on the x4 interface is not forwarded.

In the Transparent mode, the data rate is the same between DQ/DQS interface and MDQ/MDQS interface regardless of Mux mode or Rank mode for both read and write directions.

In transparent mode the Data Buffer statically enables the input receivers of the interface that is receiving signals and permanently enables the output drivers of the interface that is sending signals out. In this mode, the data and data strobe signals flow asynchronously through the MDB. Propagation delays for all the signals within each DQ/DQS and MDQ/MDQS nibble must be matched closely enough to meet parameter  $D_{TPM\_DQ}$  in Table 247. All the clock frequencies available in test mode and normal operation mode in the Data Buffer will be supported in transparent mode. DQSs are treated as differential. This means if a DQSx\_t and the corresponding DQSx\_c are both HIGH or both LOW, the associated MDQSx\_t and MDQSx\_c will be invalid. MDQSs are treated as differential as well.

In transparent mode, the strength of the DRAM interface termination is controlled by the MDQ RTT Buffer Control Word and the strength of the Host Interface termination is controlled by the RTT\_PARK Buffer Control Word.

To exit transparent mode in the DDR5MDB02 device, it is necessary to apply power cycle or Normal Operation RESET (as defined in Table 34).



### 3.6 Transparent Mode (cont'd)

**Table 5 — MDB Termination Control in Transparent Mode**

BCS_n, BCOM[2:0]	TPM Termination Control RW82[1]	Host Interface Termination	DRAM Interface Termination
= “1111”	0 (default)	ON	OFF
	1	OFF	OFF
= “1000”	0 (default)	OFF	ON
	1	OFF	OFF

### 3.7 DQ Pass-Through Mode

For initialization and training applications, DDR5MDB02 supports DQ pass through mode.

DQ pass-through mode is enabled in the DDR5MDB02 by setting [RW82\[2\]](#) to 1. While in the DQ pass-through mode, the DDR5MDB02 only supports MRW BCOM commands and any commands other than MRW are not allowed.

When DQ pass-through mode is enabled, if the direction select control word bit [RW82\[3\]](#) is set to 0 (default value), then DQ pass-through mode is enabled in the Write direction from Host interface DQ/DQS to DRAM interface MDQ/MDQS. The DDR5MDB02 directs the data flow from Host interface to DRAM interface, and it enables or disables the on-die termination at the Host interface based on the setting in [RW82\[1\]](#).

When DQ pass-through mode is enabled, if the direction select control word bit [RW82\[3\]](#) is set to 1, then DQ pass-through mode is enabled in the read direction from DRAM interface MDQ/MDQS to Host interface DQ/DQS. The DDR5MDB02 directs the data flow from DRAM interface to Host interface, and it enables or disables the on-die termination at the DRAM interface based on the setting in [RW82\[1\]](#).

In Mux mode, when the write direction is selected, DQ/DQS are broadcast to MDQ/MDQS of both PS0 and PS1. When the read direction is selected, the data flow from MDQS to DQS is controlled by [PG\[70\]RWE4\[2\]](#), and the data flow from MDQ to DQ is controlled by [PG\[70\]RWE4](#) and [PG\[70\]RWE5](#). When [PG\[70\]RWE4\[0\] = 1](#), the DQ Static Mux Mode for DQ Pass Through and Transparent modes is enabled, the pseudo channel can be selected for each DQs in [PG\[70\]RWE5\[7:0\]](#). When [PG\[70\]RWE4\[0\] = 0](#), the DQ Static Mux Mode for DQ Pass Through and Transparent modes is disabled, DQ Pass through mode and transparent mode PS selection is determined by [PG\[70\]RWE4\[2\]](#) and applies to all DQ bits.

In Mux mode with the DQ Bus CRC function enabled, when the DQ Pass-through mode is entered with read direction selected, DQS1\_t and DQS1\_c will be driven to both HIGH or differential HIGH by the MDB.

In Rank mode, when the write direction is selected, DQ/DQS are broadcast to MDQ/MDQS of both A and B ports. When the read direction is selected, the data flow from MDQ/MDQS to DQ/DQS is controlled by [PG\[60\]RWE4\[0\]](#). When [PG\[60\]RWE4\[0\] = 0](#), the A\_MDQS and A\_MDQ interface signals are selected for the data flow to the Host interface. When [PG\[60\]RWE4\[0\] = 1](#), the B\_MDQS and B\_MDQ interface signals are selected for the data flow to the Host interface.

When forwarding from a x8 interface to a x4 interface, the single strobe on the x8 interface will be forwarded to both strobes on the x4 interface. When forwarding from a x4 interface to a x8 interface, the upper strobe on the x4 interface is not forwarded.

In the DQ pass-through mode, the data rate is always the same between DQ and MDQ regardless of Rank mode or Mux mode. The data rate between DQS and MDQS is the same except when Mux mode is enabled and write direction is selected. Please refer to the PDA description in Chapter 7.1, “Per DRAM Addressability (PDA) Mode,”.

### 3.7 DQ Pass-Through Mode (cont'd)

In the DQ pass-through mode, the strength of the DRAM interface termination is controlled by the MDQ RTT Buffer Control Word and the strength of the Host Interface termination is controlled by the RTT\_PARK Control Word. In the DQ pass-through mode, the Data Buffer statically enables the input receivers of the interface that is receiving signals and enables the output drivers of the interface that is sending signals out. In this mode, the data and data strobe signals flow asynchronously through the MDB. Propagation delays for all the signals within each DQ/DQS-MDQ/MDQS nibble must be matched closely enough to meet parameter  $D_{TPM\_DQ}$  in Table 247. All the clock frequencies available in test mode and normal operation mode will be supported. DQSs are treated as differential. This means if a  $DQSx\_t$  and the corresponding  $DQSx\_c$  are both HIGH or both LOW, the associated  $MDQSx\_t$  and  $MDQSx\_c$  will be invalid. MDQSs are treated as differential as well.

**Table 6 — MDB Termination Control in DQ Pass-Through Mode<sup>1</sup>**

DQ Pass Through Mode	Termination Control RW82[1]	Host Interface Termination	DRAM interface Termination
Enabled for write direction	0 (default)	ON	OFF
	1	OFF	OFF
Enabled for read direction	0 (default)	OFF	ON
	1	OFF	OFF

NOTE 1 The MDB termination control during DQ pass-through mode is irrelevant to the {BCS\_n, BCOM} patterns.

After the DQ pass-through mode is enabled or disabled, the controller will wait for 32 clock cycles of data path settling time.

The DDR5MDB02 exits the DQ pass-through mode when RW82[2] is set to 0.

### 3.8 DQ Bus CRC

#### 3.8.1 CRC Polynomial and Bit Mapping

8 bit CRC feature is used to protect the data bus link between the Host controller and the Data Buffers, and is supported in Mux mode only. The DRAM CRC feature is not supported when MDB is configured in Mux mode. When CRC is enabled in PG[70]RWE0, the feature is applied to both sub-channels and both pseudo channels within a sub-channel. The CRC calculation is separate for each data buffer, and separate per pseudo-channel.

The  $DQS1\_t/c$  signals on each data buffer are used to send the CRC data differentially between the Host and the Data Buffer. When  $DQS1\_t/c$  signals are differential HIGH, the CRC data is HIGH. When  $DQS1\_t/c$  signals are differential LOW, the CRC data is LOW. When CRC is enabled, MDB always uses byte strobes between the Host and MDB, using only  $DQS0\_t/c$ . The byte strobes are used in both the read and write direction.

The CRC polynomial is the ATM-8 HEC  $X^8 + X^2 + X^1 + 1$  which is the same as the polynomial used on both DDR4 and DDR5 DRAMs. The pseudo-channels are interleaved on the data bus on a per bit basis; therefore, the CRC is also interleaved in the same manner. Unlike the MRCD02 DCA bus CRC, which sends the CRC continuously regardless of whether commands are being sent, the Host controller only sends the data bus CRC with each data burst. During a data bus transmission, when one pseudo-channel is not sending data, the corresponding CRC bits are not being sent for this pseudo-channel with the signals indicating a “1”.

The following diagrams show the bit mapping of the two pseudo-channels sending data starting at the same time.

Pseudo Channel	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
DQ0	D0	D0	D1	D1	D2	D2	D3	D3	D4	D4	D5	D5	D6	D6	D7	D7	D8	D8	D9	D9	D10	D10	D11	D11	D12	D12	D13	D13	D14	D14	D15	D15
DQ1	D8	D8	D9	D9	D10	D10	D11	D11	D12	D12	D13	D13	D14	D14	D15	D15	D8	D8	D9	D9	D10	D10	D11	D11	D12	D12	D13	D13	D14	D14	D15	D15
DQ2	D16	D16	D17	D17	D18	D18	D19	D19	D20	D20	D21	D21	D22	D22	D23	D23	D16	D16	D17	D17	D18	D18	D19	D19	D20	D20	D21	D21	D22	D22	D23	D23
DQ3	D24	D24	D25	D25	D26	D26	D27	D27	D28	D28	D29	D29	D30	D30	D31	D31	D24	D24	D25	D25	D26	D26	D27	D27	D28	D28	D29	D29	D30	D30	D31	D31
DQ4	D32	D32	D33	D33	D34	D34	D35	D35	D36	D36	D37	D37	D38	D38	D39	D39	D32	D32	D33	D33	D34	D34	D35	D35	D36	D36	D37	D37	D38	D38	D39	D39
DQ5	D40	D40	D41	D41	D42	D42	D43	D43	D44	D44	D45	D45	D46	D46	D47	D47	D40	D40	D41	D41	D42	D42	D43	D43	D44	D44	D45	D45	D46	D46	D47	D47
DQ6	D48	D48	D49	D49	D50	D50	D51	D51	D52	D52	D53	D53	D54	D54	D55	D55	D48	D48	D49	D49	D50	D50	D51	D51	D52	D52	D53	D53	D54	D54	D55	D55
DQ7	D56	D56	D57	D57	D58	D58	D59	D59	D60	D60	D61	D61	D62	D62	D63	D63	D56	D56	D57	D57	D58	D58	D59	D59	D60	D60	D61	D61	D62	D62	D63	D63
DQS1_c	CRC0	CRC0	CRC1	CRC1	CRC2	CRC2	CRC3	CRC3	CRC4	CRC4	CRC5	CRC5	CRC6	CRC6	CRC7	CRC7	CRC0	CRC0	CRC1	CRC1	CRC2	CRC2	CRC3	CRC3	CRC4	CRC4	CRC5	CRC5	CRC6	CRC6	CRC7	CRC7

64 bits Data + 8 bits CRC for Pseudo Channel 0 and  
64 bits Data + 8 bits CRC for Pseudo Channel 1      64 bits Data + 8 bits CRC for Pseudo Channel 0 and  
64 bits Data + 8 bits CRC for Pseudo Channel 1

Pseudo Channel	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
DQ0	HI	D0	HI	D1	HI	D2	HI	D3	D0	D4	D1	D5	D2	D6	D3	D7	D4	D0	D5	D1	D6	D2	D7	D3	D0	D4	D1	D5	D2	D6	D3	D7	D4	HI	D5	HI	D6	HI	D7	HI								
DQ1	HI	D8	HI	D9	HI	D10	HI	D11	D8	D12	D9	D13	D10	D14	D11	D15	D12	D8	D13	D9	D14	D10	D15	D11	D8	D12	D9	D13	D10	D14	D11	D15	D12	HI	D13	HI	D14	HI	D15	HI								
DQ2	HI	D16	HI	D17	HI	D18	HI	D19	D16	D20	D17	D21	D18	D22	D19	D23	D20	D16	D21	D17	D22	D18	D23	D19	D16	D20	D17	D21	D18	D22	D19	D23	D20	HI	D21	HI	D22	HI	D23	HI								
DQ3	HI	D24	HI	D25	HI	D26	HI	D27	D24	D28	D25	D29	D26	D30	D27	D31	D28	D24	D29	D25	D30	D26	D31	D27	D24	D28	D25	D29	D26	D30	D27	D31	D28	HI	D29	HI	D30	HI	D31	HI								
DQ4	HI	D32	HI	D33	HI	D34	HI	D35	D32	D36	D33	D37	D34	D38	D35	D39	D36	D32	D37	D33	D38	D34	D39	D35	D32	D36	D33	D37	D34	D38	D35	D39	D36	HI	D37	HI	D38	HI	D39	HI								
DQ5	HI	D40	HI	D41	HI	D42	HI	D43	D40	D44	D41	D45	D42	D46	D43	D47	D44	D40	D45	D41	D46	D42	D47	D43	D40	D44	D41	D45	D42	D46	D43	D47	D44	HI	D45	HI	D46	HI	D47	HI								
DQ6	HI	D48	HI	D49	HI	D50	HI	D51	D48	D52	D49	D53	D50	D54	D51	D55	D52	D48	D53	D49	D54	D50	D55	D51	D48	D52	D49	D53	D50	D54	D51	D55	D52	HI	D53	HI	D54	HI	D55	HI								
DQ7	HI	D56	HI	D57	HI	D58	HI	D59	D56	D60	D57	D61	D58	D62	D59	D63	D60	D56	D61	D57	D62	D58	D63	D59	D56	D60	D57	D61	D58	D62	D59	D63	D60	HI	D61	HI	D62	HI	D63	HI								
DQS1_t/c	HI	CRC0	HI	CRC1	HI	CRC2	HI	CRC3	CRC0	CRC4	CRC1	CRC5	CRC2	CRC6	CRC3	CRC7	CRC4	CRC0	CRC5	CRC1	CRC6	CRC2	CRC7	CRC3	CRC0	CRC4	CRC1	CRC5	CRC2	CRC6	CRC3	CRC7	CRC4	HI	CRC5	HI	CRC6	HI	CRC7	HI								

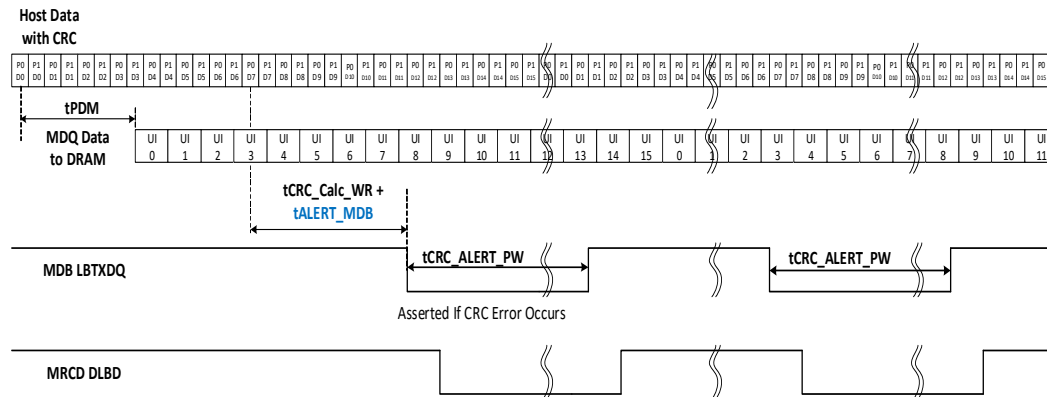
Diagram illustrating the bit sequence for Pseudo Channels 0 and 1. The channels are defined by the following bit patterns:

- Pseudo Channel 1:** 64 bits Data + 8 bits CRC for Pseudo Channel 1.
- Pseudo Channel 0:** 64 bits Data + 8 bits CRC for Pseudo Channel 0.

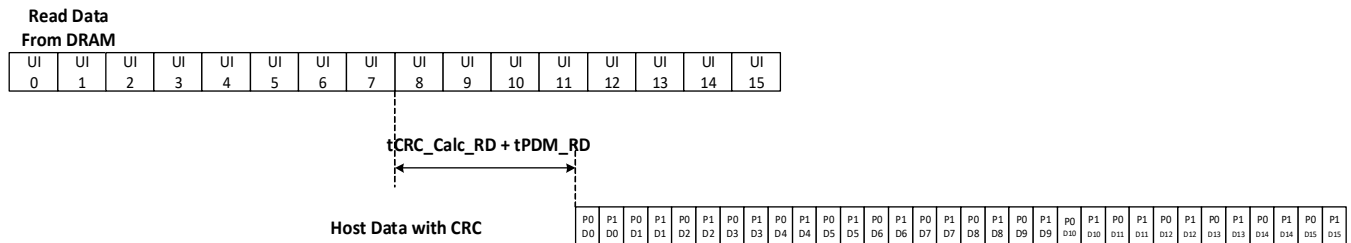
Upon a Write CRC error, the MDB sends an alert signal to LBTXDQ by driving it Low for tCRC\_ALERT\_PW, and set Write CRC Error Status bit in PG[70]RWE0[4] to 1. The Write CRC Error Status bit remains at “1” until the Host clears it by using an MRW command to write it to 0. The latency from the last UI of a 64-bit data block to LBTXDQ Low is the sum of tCRC\_Calc\_WR and tALERT\_MDB. The CRC error alert is sent to the MRCD via the LBTXDQ (Loopback Data) signal to the MRCD DLBD input and is re-driven to the Host controller. If there are multiple CRC errors from other MDBs on the DIMM, the pulse may be seen longer. When there is a CRC error, the data will still be written to the DRAMs, as it will be rewritten later during the error recovery by the Host.

The data bus write and read CRC timing is shown in Figure 15 and Figure 16.

### 3.8.1 CRC Polynomial and Bit Mapping (cont'd)



### Figure 15 — Write Data with CRC



### Figure 16 — Read Data with CRC

### 3.8.2 DQ Bus CRC Polynomial and Logic Equation

The CRC polynomial used by MRDIMM is the ATM-8 HEC  $X^8+X^2+X+1$ . A combinatorial logic for this 8-bit CRC is implemented for 64-bit data as shown below. D[63:56] are mapped from 8-UI of DQ[7:0] as shown in Figure 13 and Figure 14.

CRC COMBINATORIAL LOGIC EQUATIONS

```
module CRC8_D64;
```

```
// polynomial: (0 1 2 8)
```

```
// data width: 64
```

```
// convention: the first serial data bit is D[63]
```

```
// initial condition all 0 implied
```

function [7:0]

```
nextCRC8_D64;
```

```
input [63:0] Data;
```

```
reg [63:0] D;
```

```
reg [7:0] NewCRC;
```

begin

D = Data;

### 3.8.2 DQ Bus CRC Polynomial and Logic Equation (cont'd)

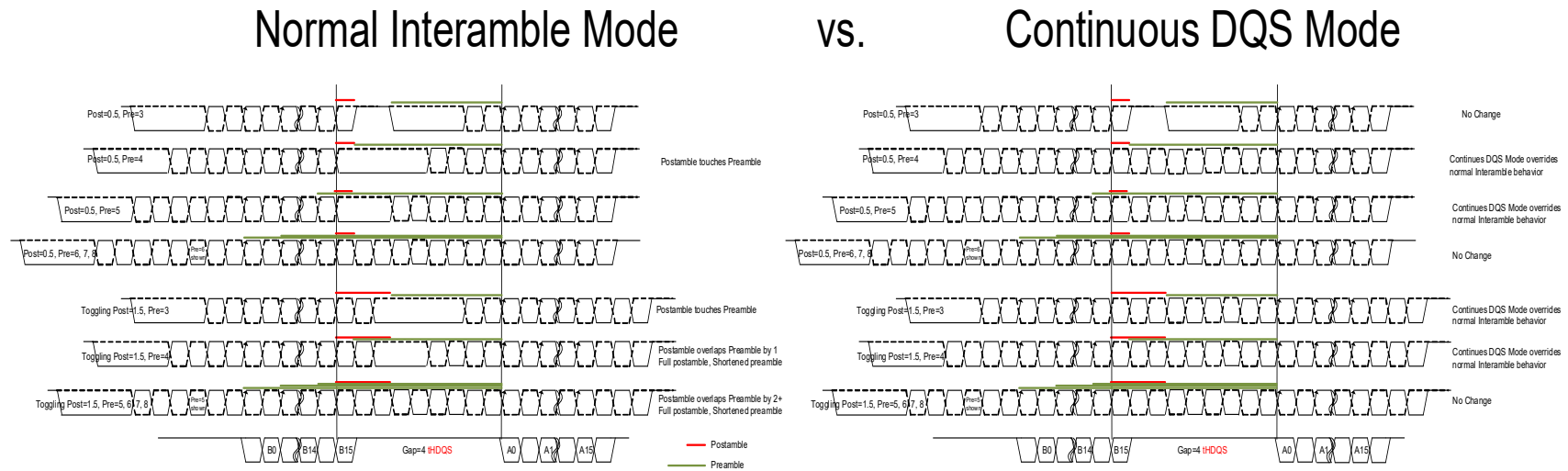
```

NewCRC[0] = D[63] ^ D[60] ^
D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0];
NewCRC[1] = D[63] ^ D[61] ^ D[60] ^ D[57] ^
D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
NewCRC[2] = D[63] ^ D[62] ^ D[61] ^ D[60] ^
D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
NewCRC[3] = D[63] ^ D[62] ^ D[61] ^ D[59] ^
D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];
NewCRC[4] = D[63] ^ D[62] ^ D[60] ^
D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
NewCRC[5] = D[63] ^ D[61] ^ D[60] ^
D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];
NewCRC[6] = D[62] ^ D[61] ^ D[58] ^
D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];
NewCRC[7] = D[63] ^ D[62] ^ D[59] ^
D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];
nextCRC8_D64 = NewCRC;

```

### 3.9 Continuous DQS Toggle during Interamble between Host and MDB

This functionality allows for the DQS to continue toggling any time the postamble of one DQS burst touches the preamble of the next DQS burst instead of following the traditional patterns defined by the interamble specification. When the spacing gap between two bursts is extended to the point where the postamble and preambles do not touch, the traditional interamble patterns shall be followed. This mode is only available in Mux mode, will be configured with a register bit and is an override just between the Host and the MDB. This mode does not transition to the DRAMs (backside bus = MDB to DRAM). The Normal interamble behavior is the default mode as defined in the [PG\[70\]RWF6](#).



**Figure 17 — Example of Traditional Interamble vs Continuous DQS Toggle Mode for Consecutive Reads Operation: Gap = 4 tHDQS**

### 3.10 Extended Read and Write Preamble Modes between Host and MDB

This functionality allows for the Host to utilize longer read and write preambles for the DQS pins. The range has been expanded to grow the preamble to 8tHDQS. This does not change the behavior of the backside channel (MDB to DRAMs) which are still driven by the snoop based registers for determining the correct preambles and postambles.

Figure 18 and Figure 19 are examples of the Read Preamble/Postamble waveforms.

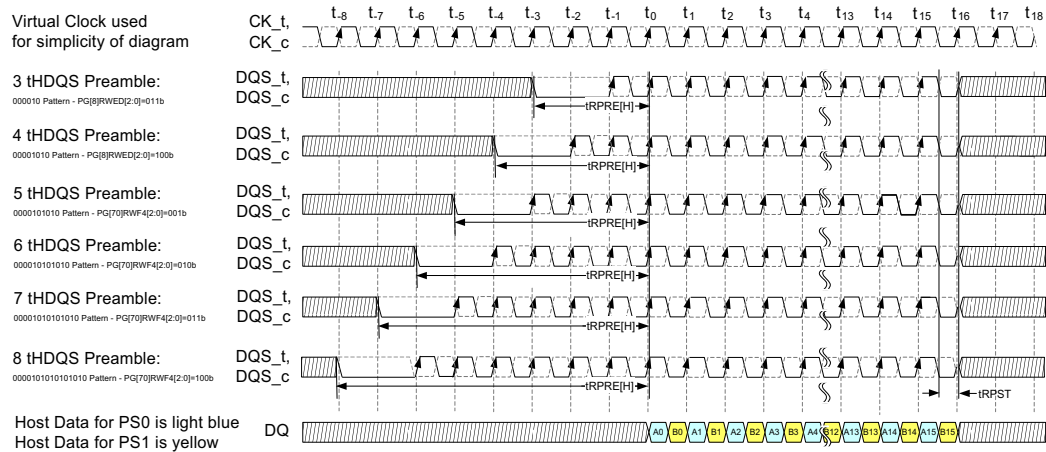


Figure 18 — Read Preamble with 0.5tHDQS Postamble

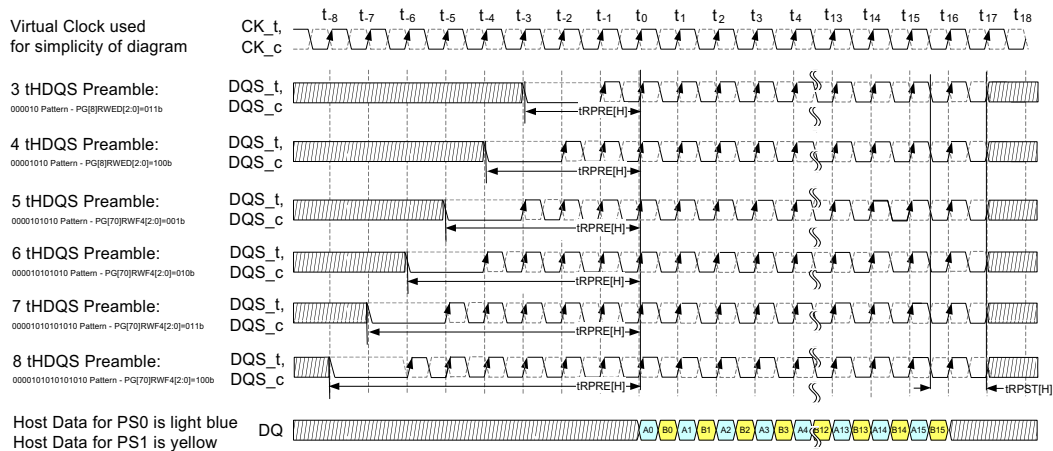
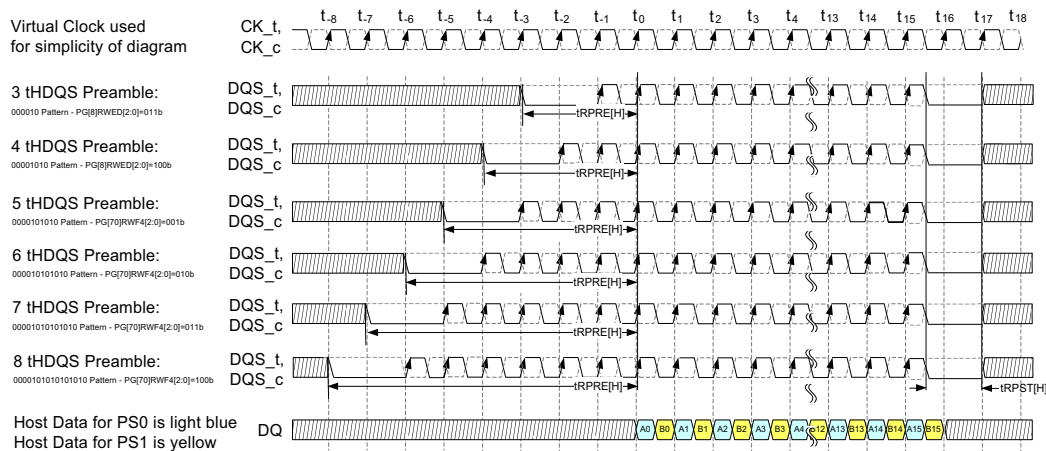


Figure 19 — Read Preamble with 1.5tHDQS Toggling Postamble

### 3.10 Extended Read and Write Preamble Modes between Host and MDB (cont'd)



**Figure 20 — Read Preamble with 1.5tHDQS Static Postamble**

Figure 20 shows the extended preambles for 5/6/7/8 tHDQS options as well as the original DRAM supported versions for reference.

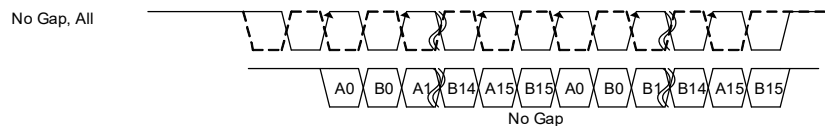
#### 3.10.1 Read Interamble Timing Diagrams

In Read to Read operations with  $t_{CCD} = BL/2$ , the postamble for the 1st command and the preamble for the 2nd command shall disappear to create consecutive DQS latching edge for seamless burst operations.

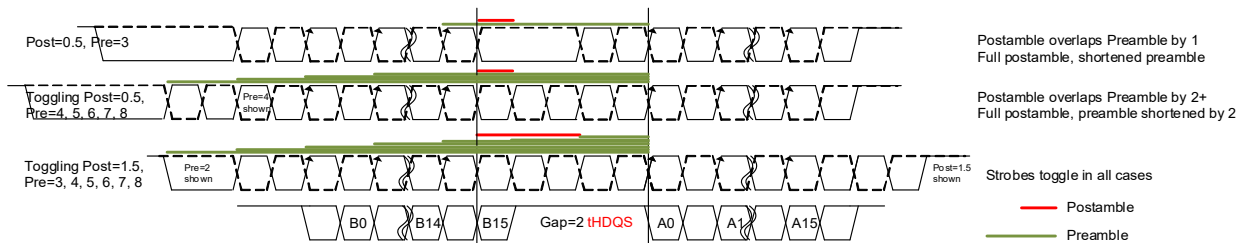
In the case of Read to Read operations, if the postamble and preambles overlap, the toggles take precedence over static portion of the preambles or postambles.

In the case that Continuous Toggle Mode ( $PG[70]RWF6[0]=1$ ) is enabled, anytime the postambles and preambles touch or overlap, the DQS continues to toggle nonstop through the end of the bursts.

Note: These diagrams are drawn for the Host side in the Mux mode.



**Figure 21 — Example of Seamless Reads Operation: No Gap**



**Figure 22 — Example of Consecutive Reads Operation: Gap = 2 tHDQS**



### 3.10.1 Read Interamble Timing Diagrams (cont'd)

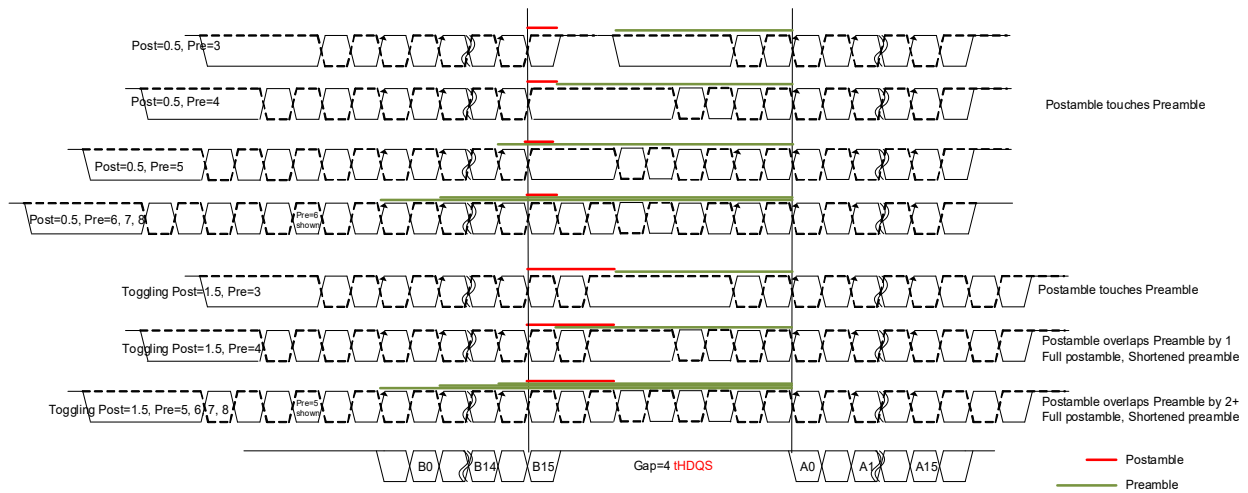


Figure 23 — Example of Consecutive Reads Operation: Gap = 4 tHDQS

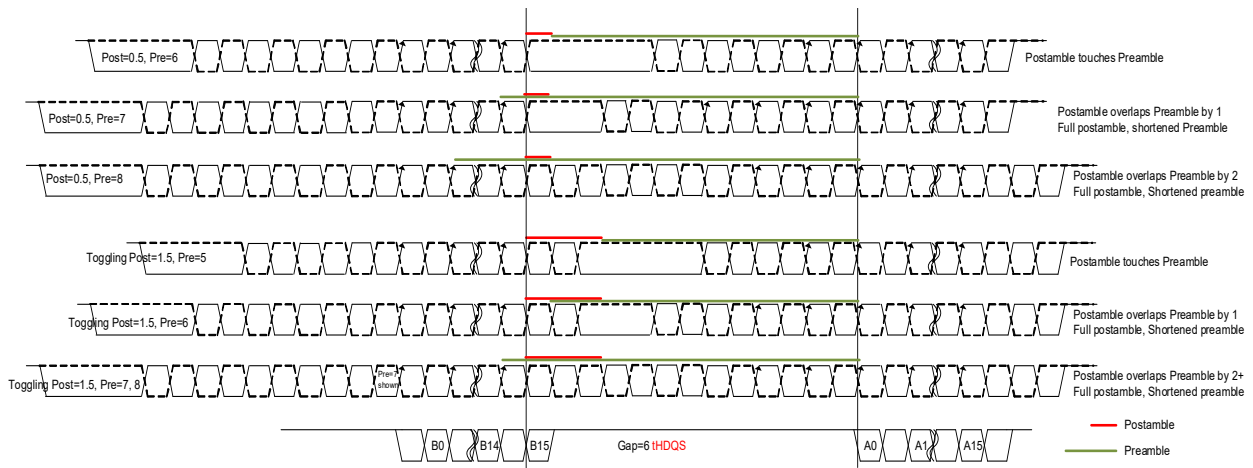


Figure 24 — Example of Consecutive Reads Operation: Gap = 6 tHDQS

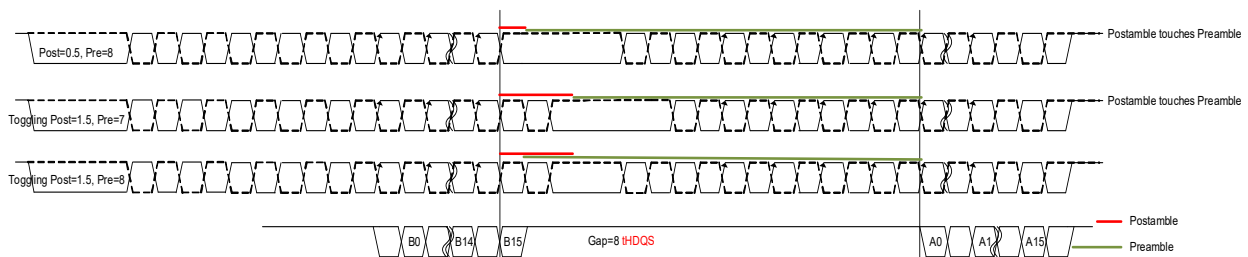


Figure 25 — Example of Consecutive Reads Operation: Gap = 8 tHDQS

### 3.10.2 Write Preamble and Postamble Diagrams

Figure 26 and Figure 27 are examples of the Write Preamble/Postamble waveforms.

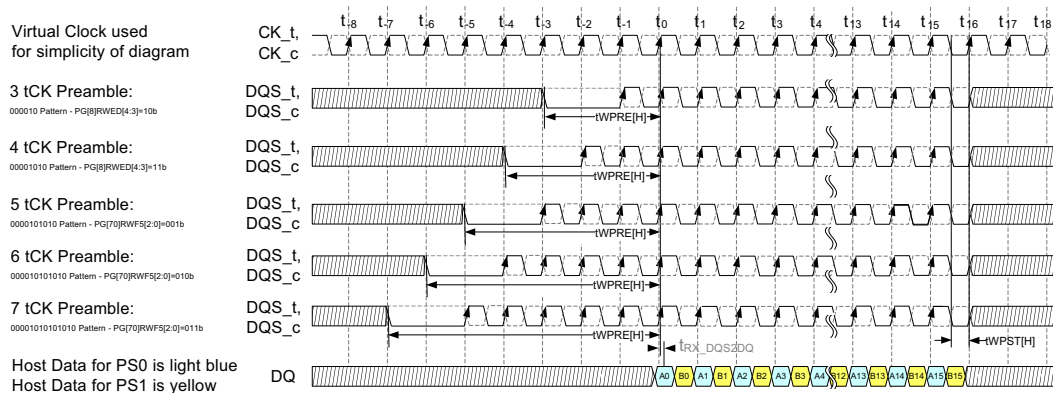


Figure 26 — Write Preamble with 0.5tHDQS Postamble

Figure 26 shows the extended preambles for 5/6/7tHDQS options as well as the original DRAM supported versions for reference.

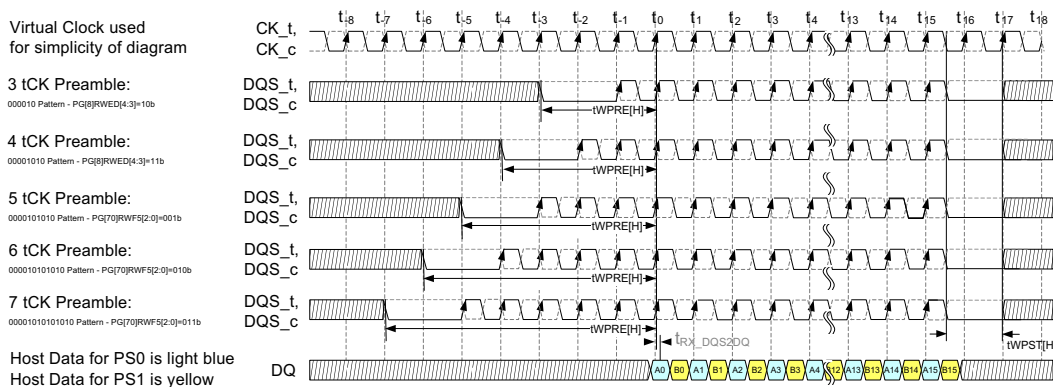


Figure 27 — Write Preamble with 1.5tHDQS Postamble

Figure 27 shows the extended preambles for 5/6/7tHDQS options as well as the original DRAM supported versions for reference. For write with 1.5tHDQS postamble, only static option is supported.

### 3.10.3 Write Interamble Timing Diagrams

In Write to Write operations with t<sub>CCD</sub>=BL/2, the postamble for the 1st command and the preamble for the 2nd command shall disappear to create consecutive DQS latching edge for seamless burst operations.

In the case of Write to Write operations, if the postamble and preambles overlap, the toggles take precedence over static portion of the preambles or postambles.

In the case that Continuous Toggle Mode (PG[70]RWF6[0]=1) is enabled, anytime the postambles and preambles touch or overlap, the DQS continues to toggle nonstop through the end of the bursts.

### 3.10.3 Write Interamble Timing Diagrams (cont'd)

When the n-Tap DFE is enabled, the DQs shall be high during Interamble for a minimum of nUI prior to the first Write data bit of the second write command. If there are nUI or less and the DFE is enabled, the Host shall drive DQs high during the full Write Interamble period.

Note: These diagrams are drawn for the Host side in the Mux mode.

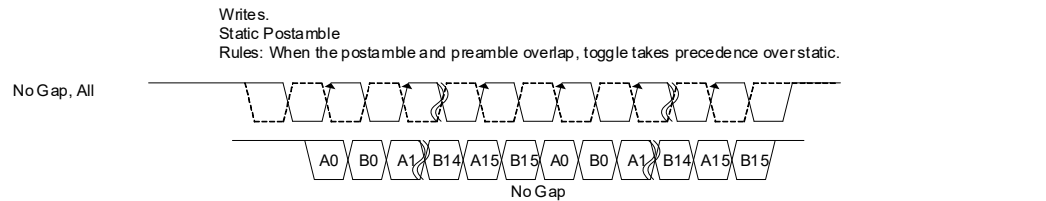


Figure 28 — Example of Seamless Writes Operation: No Gap

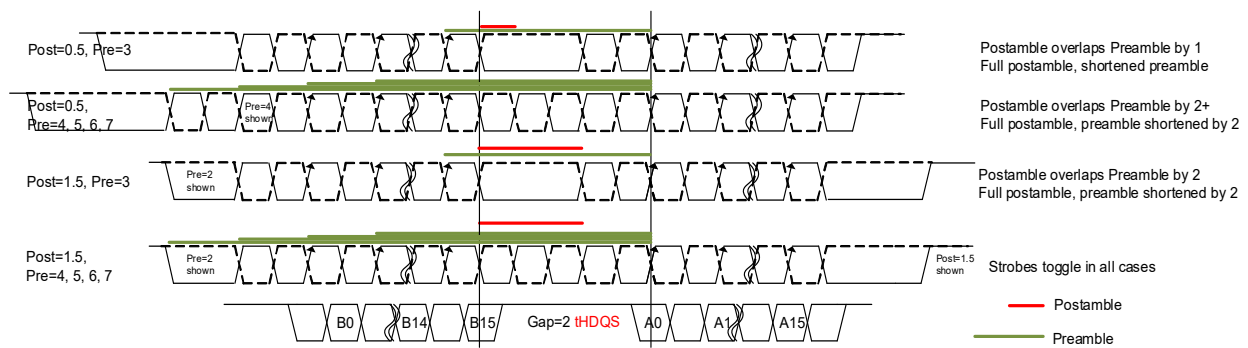


Figure 29 — Example of Consecutive Writes Operation: Gap = 2 tHDQS

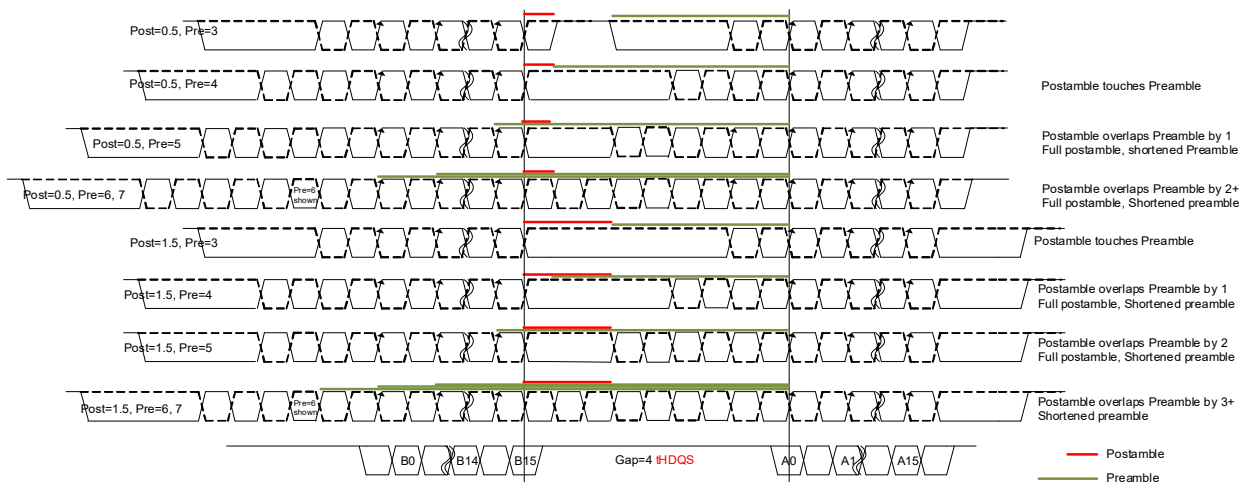


Figure 30 — Example of Consecutive Writes Operation: Gap = 4 tHDQS

3.10.3 Write Interamble Timing Diagrams (cont'd)

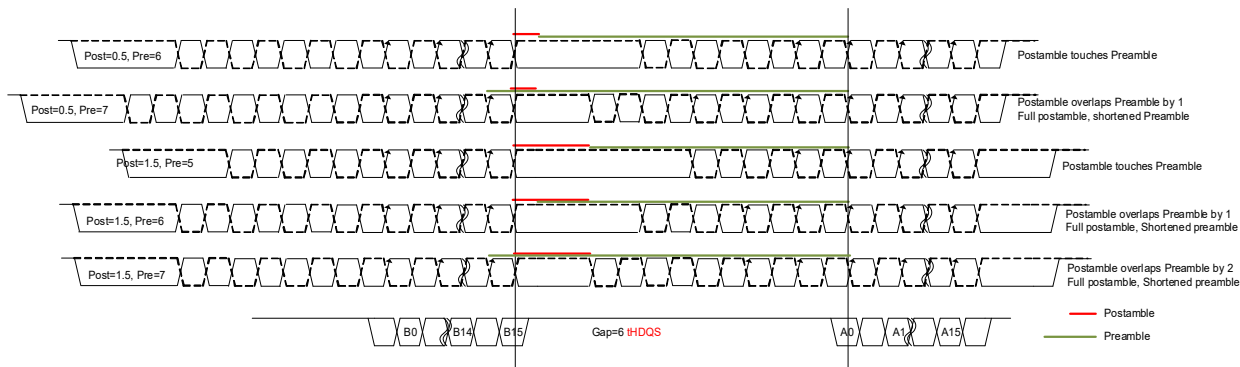


Figure 31 — Example of Consecutive Writes Operation: Gap = 6 tHDQS

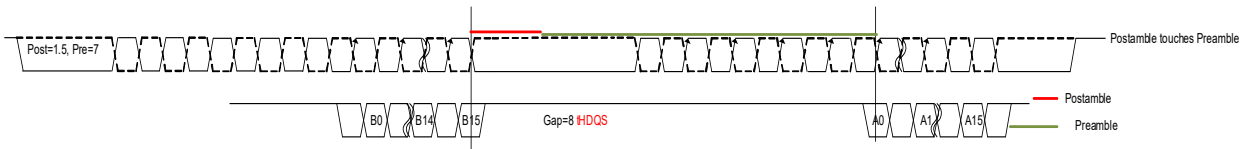


Figure 32 — Example of Consecutive Writes Operation: Gap = 8 tHDQS

3.11 Programmable Read Delay

When the device is in Mux mode only, the MDB shall support a programmable read delay feature. This feature will delay Read DQS and Data over a sub UI window referenced to BCK. This is additional delay adjustment from the nominal read BCK to DQS. This feature mitigates potential crosstalk conditions between adjacent byte lanes during read conditions to optimize performance on the Host interface at the high data rates. When enabled, [PG\[70\]RWF9\[7\] = 1](#), the system will make adjustments during system training by configuring [PG\[70\]RWF9\[3:0\]](#) to an optimal setting.

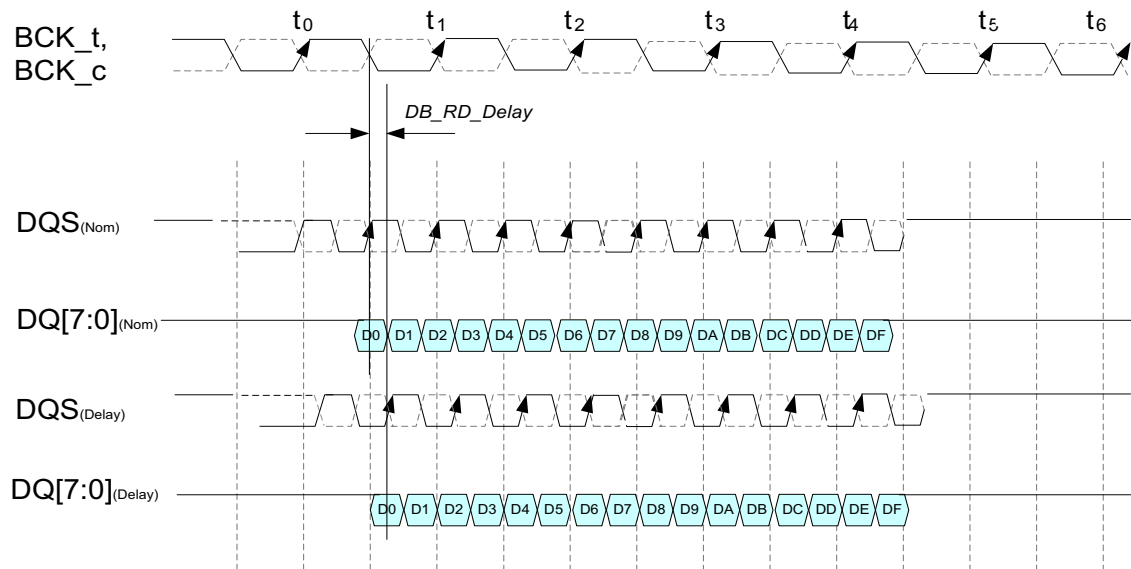


Figure 33 — Programmable Read Delay Example Relative to Nominal BCK and DQS Read

### 3.11 Programmable Read Delay (cont'd)

**Table 7 — Read Delay<sup>1</sup>**

Parameter	Min	Nom	Max	Units
RD Delay Range	0.8	1	1.2	UI
RD Delay Step Size	1/16	1/8	3/16	UI

NOTE 1 The test should be done under typical temperature and voltage conditions (i.e., 1.1 V, 25 °C).

### 3.12 Loopback Mode

With loopback circuit the DDR5MDB02 can feed a received signal or data back out to an external receiver for debugging, testing, and/or training purposes. Loopback is necessary in order for the Host memory controller or test instrument to immediately read back data that was written to the MDB without having to issue multiple DRAM WRITE/READ commands. There are also inherent limitations when characterizing the receiver using statistical analysis methods such as Bit Error Rate (BER) analysis.

For example, at  $BER=10^{-16}$ :

1. There is not enough memory depth in the DRAM to store all the  $10^{16}$  data.
2. The amount of time to perform multiple WRITE/READ commands to and from the array is prohibitively long.
3. Since the amount of time involved performing these operations is much longer than the DRAM refresh rate interval, the Host or memory controller must also manage Refreshes during testing to ensure data retention.
4. Limited pattern depth means limited Intersymbol Interference (ISI). Loopback is a necessity for characterizing the receiver without the limitations and complexities of other traditional methods.

#### 3.12.1 Loopback Output Definition

The Loopback circuitry requires two output pins (one single ended Loopback data, LBTXDQ, and one single ended Loopback strobe, LBTXDQS). The Loopback circuitry also consists of multiplexers to select the DQ and Phase for Loopback. Pin assignment location for Loopback pins are defined as J2 for LBTXDQ and J1 for LBTXDQS. The DDR5MDB will support only ¼ rate.

It is the Host's responsibility to put the device into a normal operating mode prior to sending BCOM commands.

The default RTT state for Loopback when  $RW8D[0] = 0$  is RZQ/5 (48 Ω), designated by  $RW8E[2:0] = 101$ . In this state, both the LBTXDQS and LBTXDQ outputs are disabled. If the Loopback pins of several MDB devices are connected together and some devices need disabled termination, there is RTT\_OFF option available by setting  $RW8E[2:0] = 000$ .

Enabling the Loopback Output value via  $RW8D[0] = 1$  will result in the LBTXDQS and LBTXDQ pins to transition from the RTT\_Loopback state to a MDB Drive State.

The LBTXDQS output will transition with the differential input crossing point of  $DQS\_t/DQS\_c$ , plus latency.

The LBTXDQ output will transition with the receiver data state of the DQ pin selected by  $RW8D[4:2]$ .

**Table 8 — Loopback Output Definition**

Condition	LBTXDQS	LBTXDQ	NOTE
Loopback Disabled	RTT_Loopback	RTT_Loopback	
Loopback Enabled	Selected Phase	Selected Phase and Selected DQ	

### 3.12.2 Loopback Phase

Due to the high data rates of the DDR5 Data Buffer, Loopback is implemented with 4-way interleaved outputs. With a 4-way implementation, the DQS and selected DQ will be sampled and output every 4 UI. To be able to sample all bits with a 4-way interleave implementation, the Loopback Phase Select programmed in [RW8D\[6:5\]](#) allows selection of the DQS/DQ phase to be output. In 4-way mode, Phase A, Phase B, Phase C and Phase D, are valid options. As the speeds of the link are increasing this feature will be available to the MDB through [RW8D](#).

Figure 34 shows an example of a Loopback implementation for 4-way interleave Data Buffer. This example requires a divided clock to produce DQS\_0 (PHASE A), DQS\_90 (PHASE B), DQS\_180 (PHASE C) and DQS\_270 (PHASE D). The output of the DQ slicer runs at 1/4 the speed as received data. In a 4-way interleave design, the data are received at full speed, but internally the data is latched only at quarter speed.

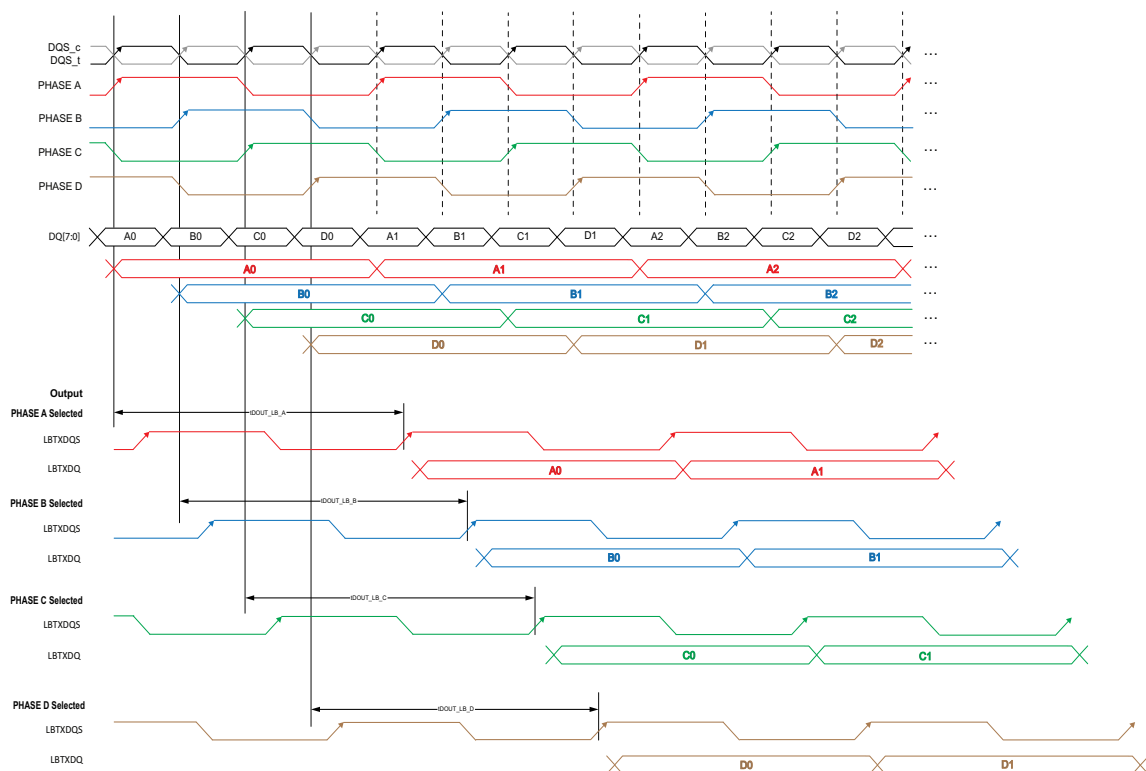


Figure 34 — Data Buffer Internal 4 Phase Selection

### 3.12.3 Loopback Output Mode

Loopback Output Mode selects whether to output LBTXDQS and LBTXDQ in DQS Qualified Output Mode or WE (Write Enable) Qualified Output Mode, based on [RW8D\[1\]](#). In the default DQS Qualified Output Mode ([RW8D\[1\]](#) = 0), the selected DQ state is captured with every DQS\_t/DQS\_c toggle for the selected Loopback Phase. In WE Qualified Output Mode ([RW8D\[1\]](#) = 1), the selected DQ state will be output on LBTXDQ when qualified by the write enable, which means data is only captured during the write burst and not during the preamble or postamble.

### 3.12.3 Loopback Output Mode (cont'd)

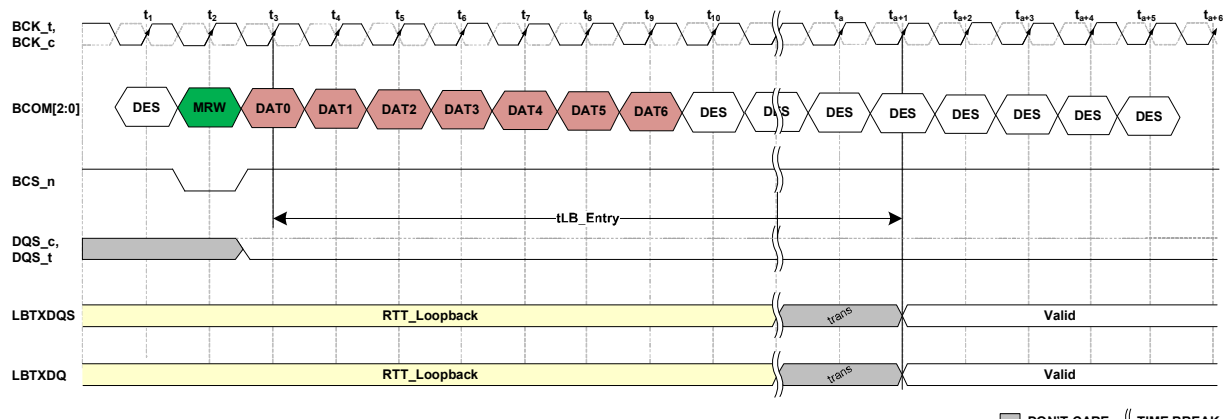


Figure 35 — Loopback Mode Entry for Output Modes Qualified by DQS or Qualified by WE

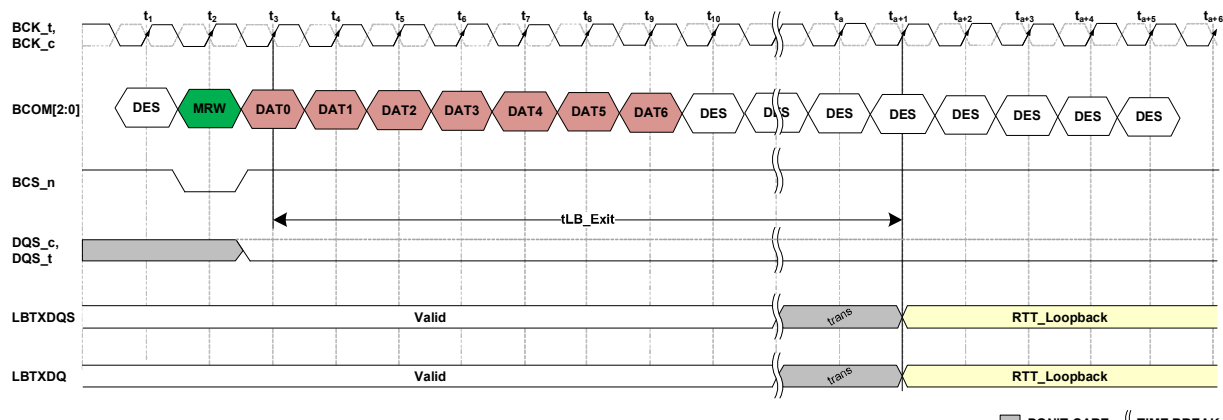


Figure 36 — Loopback Mode Exit for Output Modes Qualified by DQS or Qualified by WE

#### 3.12.3.1 Loopback DQS Qualified Output Mode (Default)

In DQS Qualified Output Mode (**RW8D[1]** = 0), the selected DQ state is captured with every DQS\_t/DQS\_c toggle for the selected Loopback Phase and output on LBTXDQ. The LBTXDQS output will be delayed by tDOUT\_LB\_\* from the selected DQS\_t/DQS\_c Loopback Phase. Since no Write commands are required in DQS Qualified Output Mode, MR settings pertaining to preamble, postamble, CWL are ignored by the Loopback function.

Additional requirements for DQS Qualified Output Mode:

- DQS must be driven differentially LOW (DQS\_t LOW, DQS\_c HIGH) prior to entry into DQS Qualified Output Mode.
- DQS\_t/DQS\_c must be continuously driven during Loopback operation. (Hi-Z state not allowed.)
- Only DES or MRW commands can be applied at BCOM[2:0]/BCS\_n command pins during DQS Qualified Output Mode.

No DFE Reset is assumed after first rising edge of DQS\_t. DRAM WR/RD operations are not supported after entering DQS Qualified Output Mode.

### 3.12.3.2 Loopback DQS Qualified Output Mode 4-Way Timing Diagrams

Loopback DQS Qualified Output Mode entry and output example timing diagrams are shown in Figure 37. The timing diagrams in the figure assume there have been other previous bursts of Loopback data.

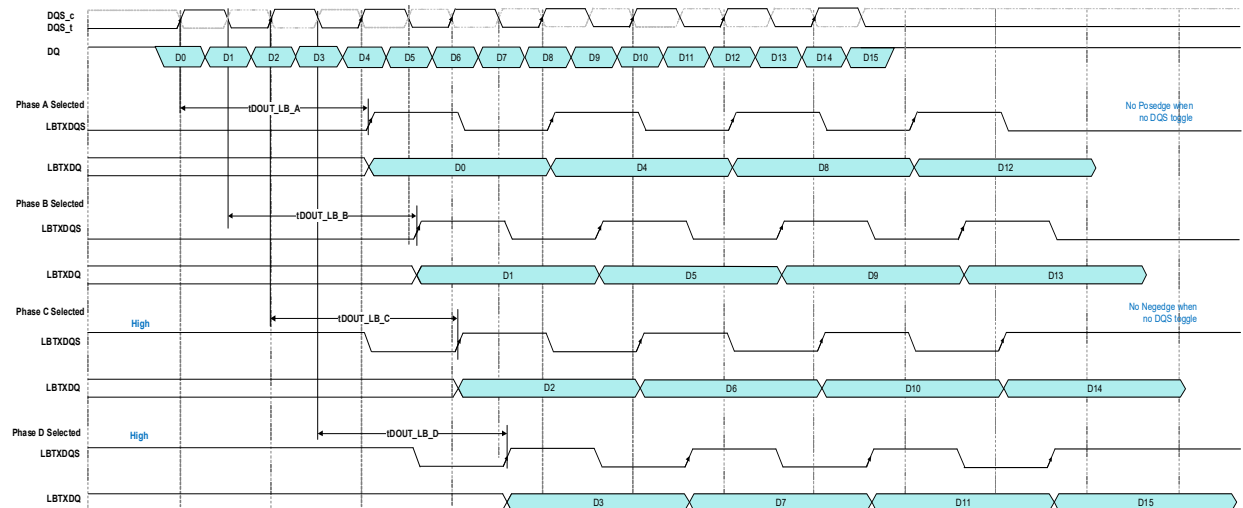


Figure 37 — Loopback DQS Qualified Output Mode 4-Way Timing Diagram

### 3.12.3.3 Loopback WE Qualified Output Mode

In WE Qualified Output Mode ( $RW8D[1] = 1$ ), Loopback data is only generated during the write burst, so it is effectively masked for the DQS toggles during the preamble or postamble. Normal Write operation for the Command, DQS and DQ is assumed. MR settings pertaining to preamble, postamble, CWL apply, as they do for any Write command.

Implementation of 4-way interleave Loopback introduces complexity in Write Burst Mode when the DQS toggle is not continuous.

If the DQS toggle is continuously generated by Write commands spaced  $BL/2$ , Loopback will align the LBTXDQS/LBTXDQ output with the selected phase for all write bursts. If the DQS toggle is not continuous due to gaps in Write commands spaced greater than  $BL/2$ , LBTXDQS/LBTXDQ may not align with the selected phase after the first write burst unless the “gap” is at least 16 tBCK (Write,  $BL/2 + 16 \text{ tBCK}$ , Write).

Table 9 — Loopback Output Phase

Write to Write Separation	Phase	NOTE
$X = BL/2$	Selected	
$BL/2 < X < BL/2 + 16\text{tBCK}$	Determined via analysis of specific conditions	1
$X \geq BL/2 + 16\text{tBCK}$	Selected	

NOTE 1 Specific conditions include selected phase, data rate, preamble, postamble, and write burst gap duration.



### 3.12.3.3 Loopback WE Qualified Output Mode (cont'd)

In the case where continuous bursts are not issued in Loopback WE Qualified Output Mode, selection of Phase C and Phase D in 4-way mode may result in the last tHW\_LBTDQS width of a burst that does not comply with spec.

Additional requirements for WE Qualified Output Mode:

Write Leveling training is required prior to Write Burst Loopback operation.

All Write timing and voltage requirements must be followed. Failure to meet this requirement results in unknown data sent to MDB, and the Loopback pins may not output the captured input data as expected.

### 3.12.3.4 Loopback WE Qualified Output Mode 4-way Timing Diagrams

Loopback Write Burst Output Mode timing diagram examples are shown below. In Mux mode,  $n = 32$ . In Rank mode,  $n = 16$ . The timing diagrams in Figure 38 through Figure 45 assume there have been other previous bursts of Loopback data and the Loopback settings in RW8D have not be modified.

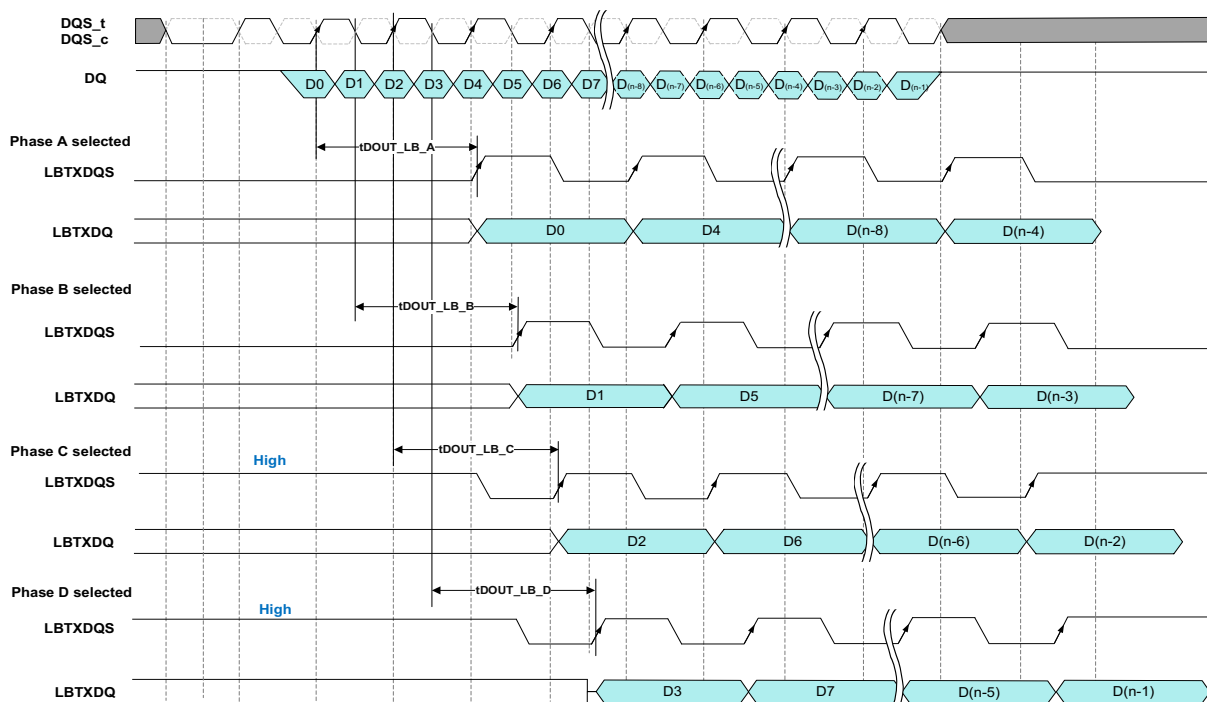


Figure 38 — 3tHDQS Preamble – 4-way WE Qualified

3.12.3.4 Loopback WE Qualified Output Mode 4-way Timing Diagrams (cont'd)

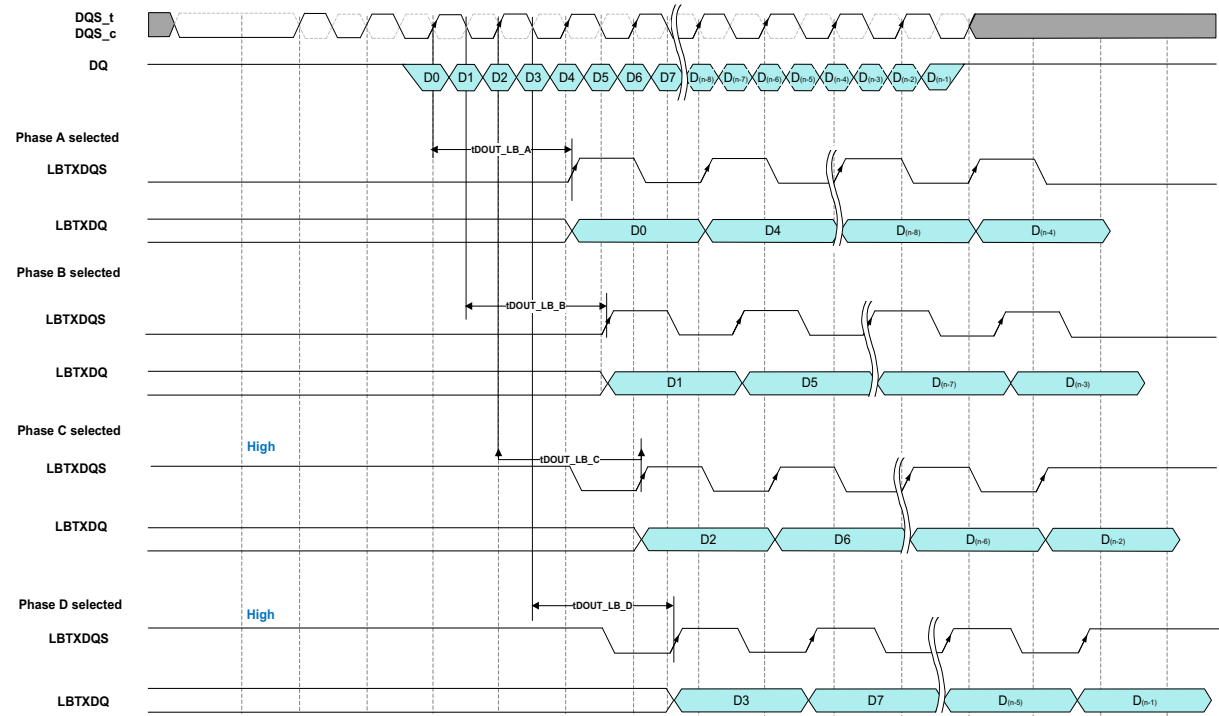


Figure 39 — 4tHDQS Preamble - 4-way WE Qualified

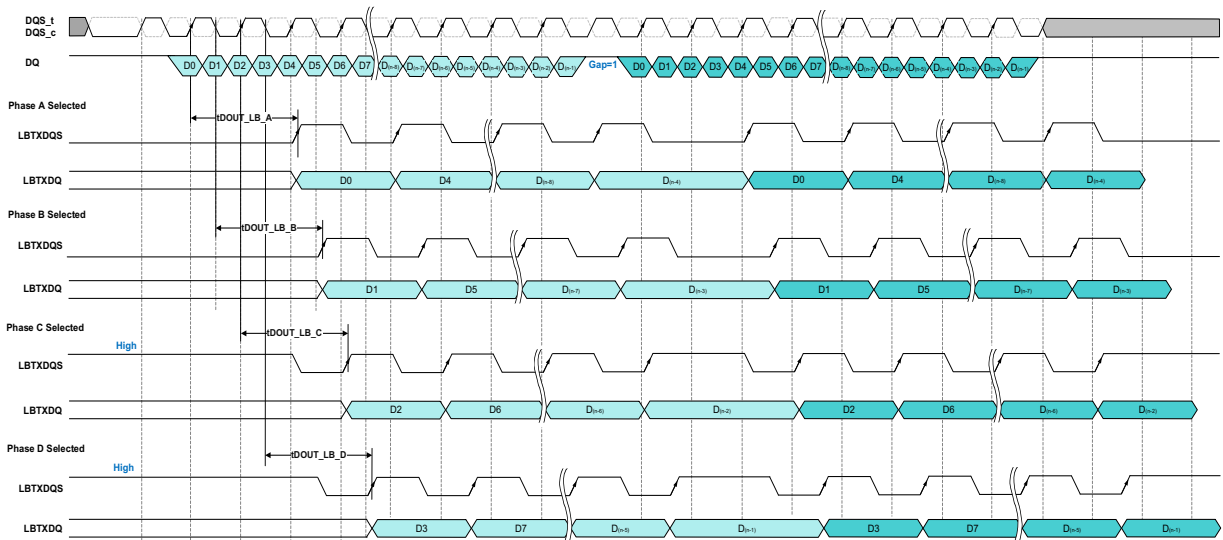


Figure 40 — 3tHDQS Preamble and 1tHDQS Gap - 4-way WE Qualified

### 3.12.3.4 Loopback WE Qualified Output Mode 4-way Timing Diagrams (cont'd)

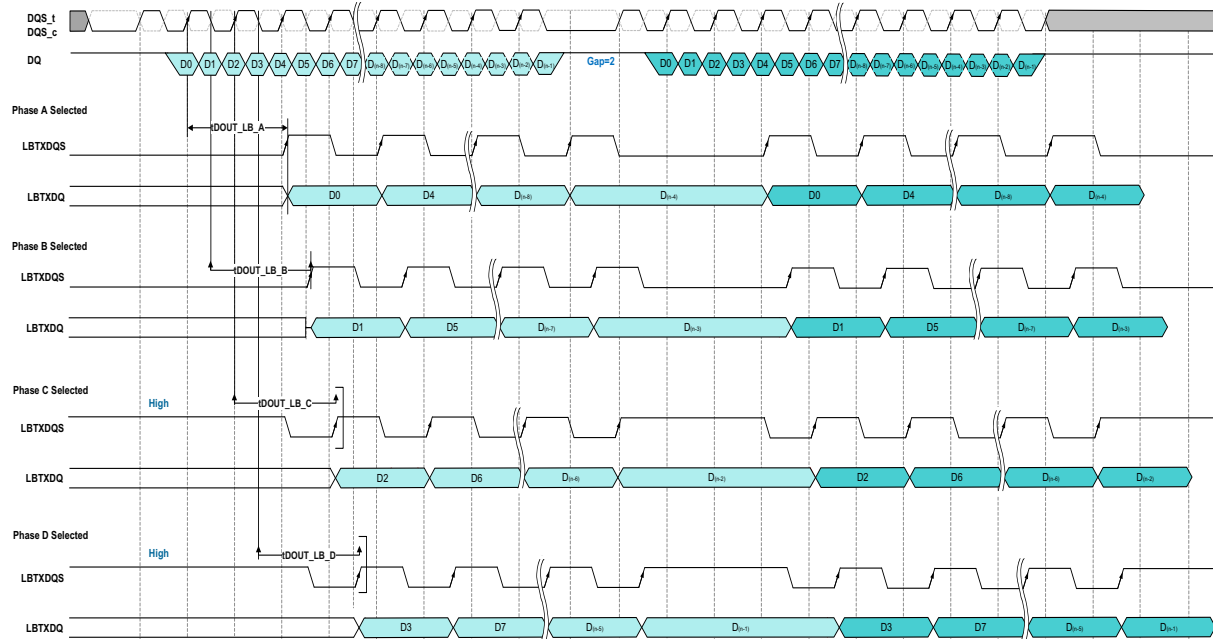


Figure 41 — 3tHDQS Preamble and 2tHDQS Gap - 4-way WE Qualified

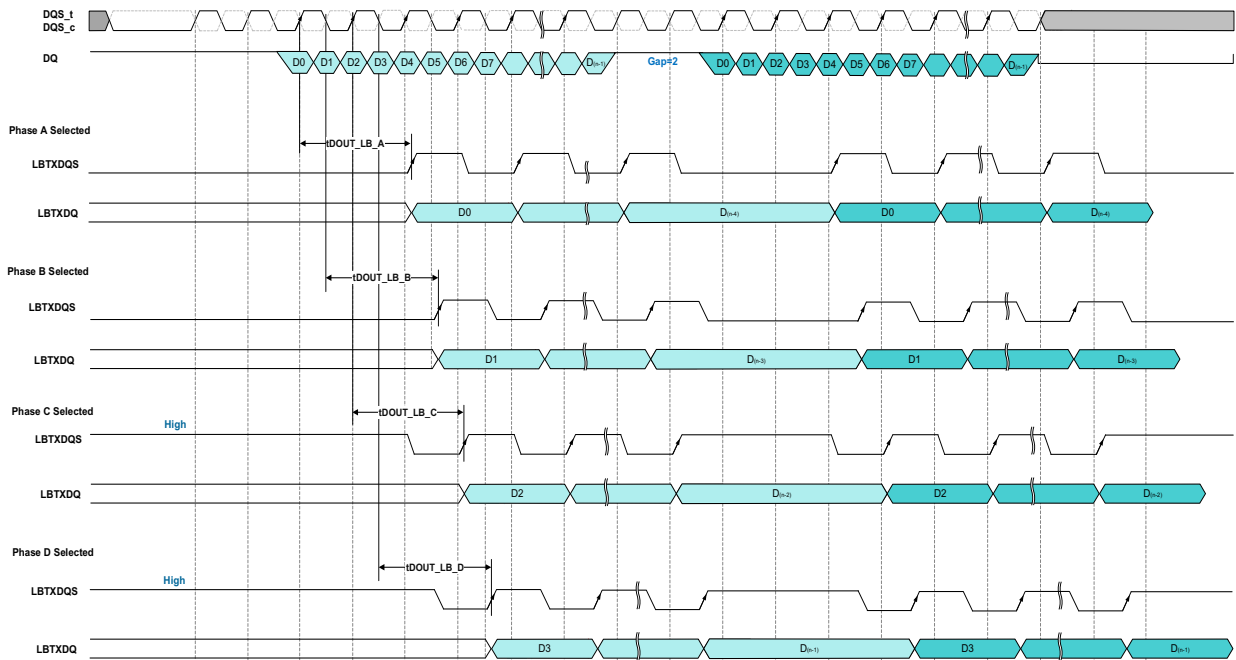
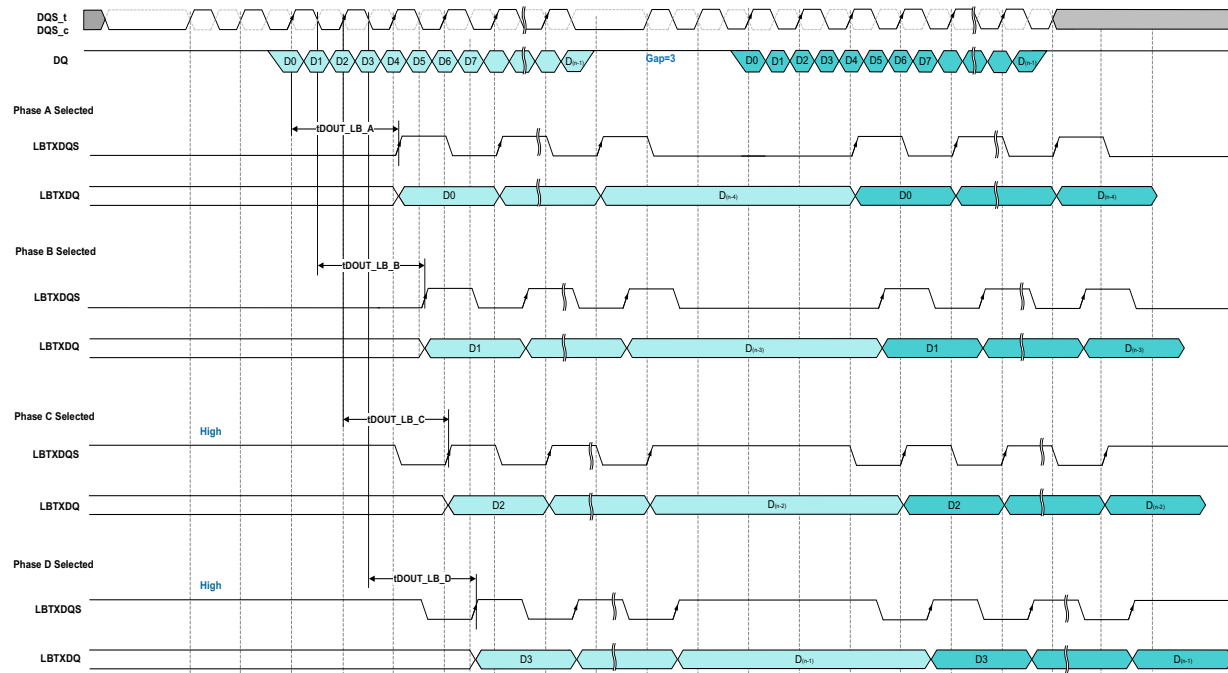
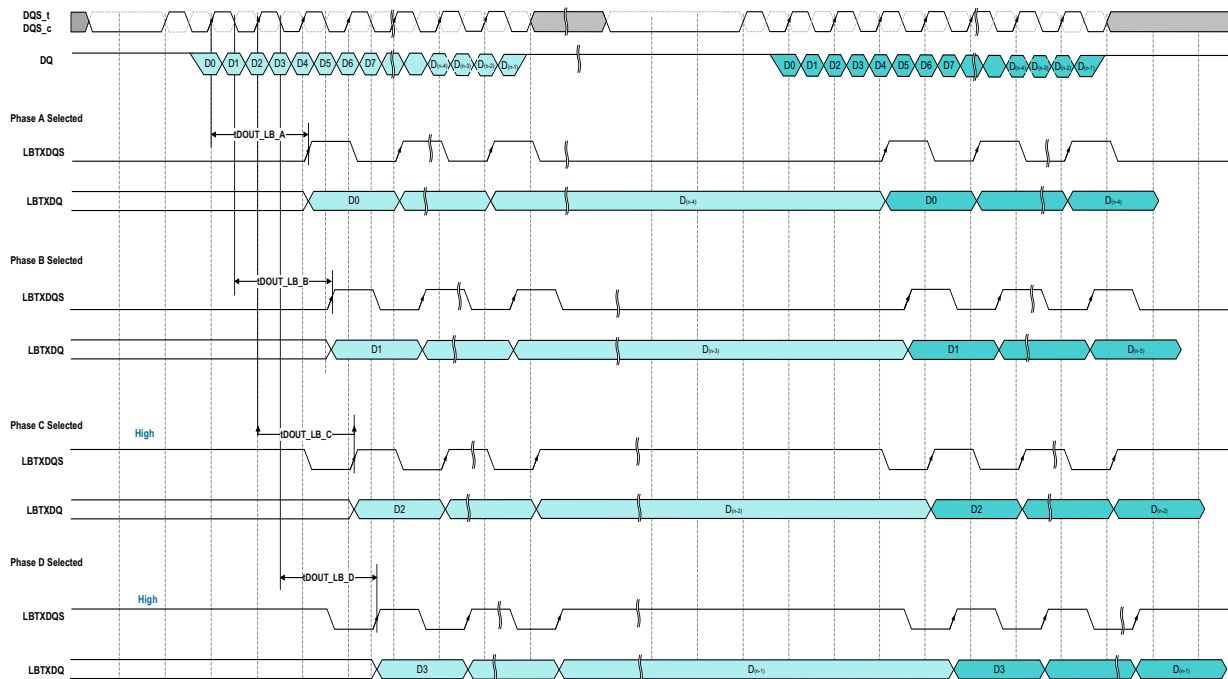


Figure 42 — 4tHDQS Preamble and 2tHDQS Gap - 4-way WE Qualified

### 3.12.3.4 Loopback WE Qualified Output Mode 4-way Timing Diagrams (cont'd)



**Figure 43 — 4tHDQS Preamble and 3tHDQS Gap - 4-way WE Qualified**



**Figure 44 — 3tHDQS Preamble without any Overlap - 4-way WE Qualified**

### 3.12.3.4 Loopback WE Qualified Output Mode 4-way Timing Diagrams (cont'd)

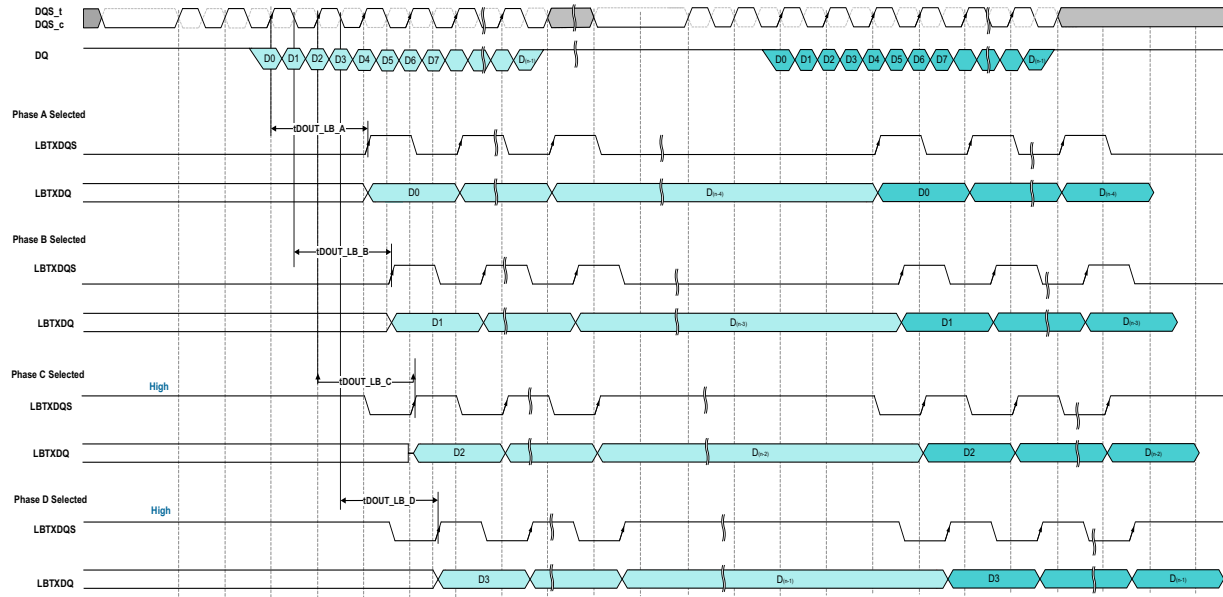


Figure 45 — 4tHDQS Preamble without any Overlap - 4-way WE Qualified

### 3.12.4 4-way Loopback Output Mode with WR\_CRC Enabled

Regardless of the DQS qualified or WE qualified output mode, the 4-way loopback output bit sequence is as follows:

Table 10 — 4-Way Loopback Output Sequence with WR\_CRC Enabled in Rank Mode

4-Way Loopback Output Sequence With WR_CRC Enabled															
Phase A	D0	D4	D8	D12	D16	GAP <sup>1</sup>	-	D2	D6	D10	D14	GAP <sup>1</sup>	D0	D4	...
Phase B	D1	D5	D9	D13	D17		-	D3	D7	D11	D15		D1	D5	...
Phase C	D2	D6	D10	D14	-		D0	D4	D8	D12	D16		D2	D6	...
Phase D	D3	D7	D11	D15	-		D1	D5	D9	D13	D17		D3	D7	...

NOTE 1 In the DQS qualified mode, there may not be any gaps. In the WE qualified mode, the gap is the interamble between two bursts. The interamble can be 0tHDQS, 1tHDQS, 2tHDQS, or more.

### 3.12.5 Loopback Output Timing Parameters

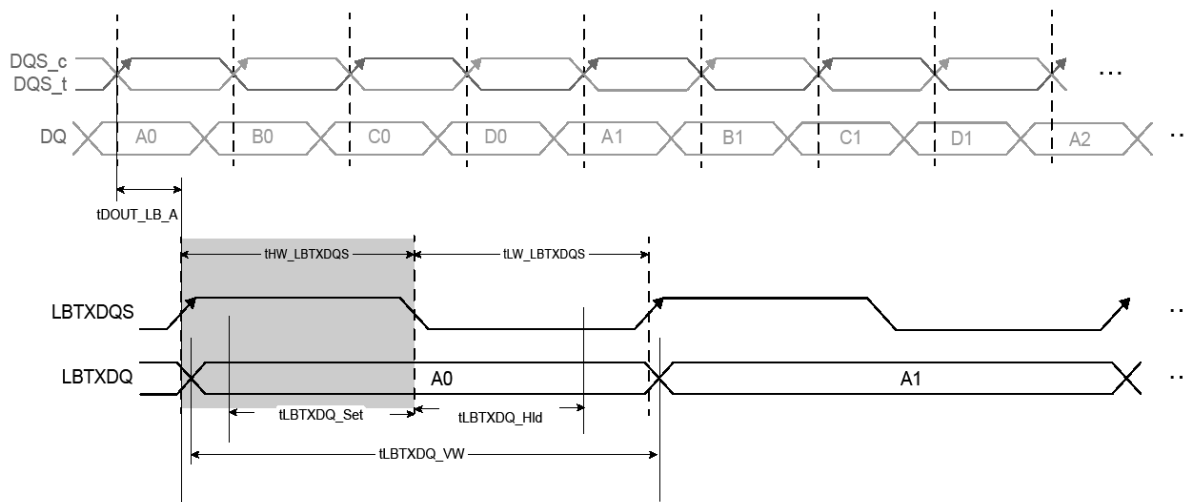
The LBTXDQS output will be delayed from the selected DQS\_t/DQS\_c Loopback Phase. The timing parameter, tDOUT\_LB\_A/tDOUT\_LB\_B/tDOUT\_LB\_C/tDOUT\_LB\_D, is shown in Table 247.

Loopback strobe LBTXDQS to Loopback data LBTXDQ relationship is illustrated in Figure 46.

- tHW\_LBTXDQS describes the single-ended LBTXDQS strobe HIGH pulse width
- tLW\_LBTXDQS describes the single-ended LBTXDQS strobe LOW pulse width
- tLBTXDQ\_Set describes the setup time of LBDQS and where LBDQ needs to remain stable
- tLBTXDQ\_Hld describes the hold time of LBDQS and where LBDQ needs to remain stable
- tLBTXDQ\_VW describes the data valid window per device per UI

### 3.12.5 Loopback Output Timing Parameters (cont'd)

Table 247 documents the values for these timing parameters.



**Figure 46 — Loopback Output 4-way Timing Parameters**

ODT for Loopback is described in 15.2. Output driver electrical characteristics for Loopback is described in 16.2.

### 3.13 ZQ Calibration

The DDR5MDB02 performs I/O circuit calibration when it receives a ZQ calibration in the MPC command. In order to use ZQ calibration command, a  $240\ \Omega \pm 1\%$  resistor must be connected between the ZQCAL pin and  $V_{SS}$ .

Proper Host interface RTT\_PARK DQ/DQS drive strength, DRAM interface RTT and MDQ/MDQS drive strength not guaranteed until a ZQ calibration has been performed. The Host sends ZQCal Start and ZQCal Latch calibration commands through the DDR5MRCD02 and forwards to DRAM and Data Buffer.

There are two ZQ Calibration modes initiated with the MPC command: ZQCal Start, and ZQCal Latch. ZQCal Start initiates the Data Buffer's calibration procedure, and ZQCal Latch captures the result and loads it into the Data Buffer's drivers. A ZQCal Start command may be issued anytime the MDB is in a state in which it can receive valid commands.

There are two timing parameters associated with ZQ Calibration.  $t_{ZQCAL}$  is the time from when the ZQCal Start MPC command is sent to when the Host can send the ZQCal Latch MPC command.  $t_{ZQLAT}$  is the time from when the ZQCal Latch MPC command is sent by the Host to when the DQ bus can be used for normal operation. A ZQCal Latch Command may be issued anytime outside of power-down after  $t_{ZQCAL}$  has expired and all DQ bus operations have completed. The DQ Bus must maintain a Deselect state during  $t_{ZQLAT}$  to allow ODT calibration settings to be updated.

After a ZQCal Start and until  $t_{ZQCAL}$  finishes, neither another ZQCal Start nor a ZQCAL Latch is allowed.

No other commands that cause data transfers on the Host interface DQ/DQS outputs or the DRAM interface MDQ/MDQS outputs are allowed during ZQCal Latch.

The DDR5MDB02 may or may not perform any calibration for its own I/O circuits on receipt of ZQCal Start.

### 3.14 Continuous Burst Mode

A continuous burst mode is configured with MRW to [RW90\[0\]](#) = 1. There are three usage models, two for DRAM interface test and the other for Host interface test.

In Mux mode, for PS0 and PS1 MDQ/MDQS test on the DRAM interface, the test sequence is as below:

1. Configure LFSR control words
  - For PS0, LFSR0 in [PG\[8\]RWE3](#) and LFSR1 in [PG\[8\]RWE4](#)
  - For PS1, LFSR0 in [PG\[8\]RWE9](#) and LFSR1 in [PG\[8\]RWEA](#)
2. Enable Continuous Burst mode by setting [RW90\[0\]](#) to 1
3. Enable MWD training mode in [RW83](#)
4. To run the continuous burst on MDQ/MDQS, the controller may send one WR command to one of the two pseudo-channels, so that MDB will continuously drive MDQ/MDQS on the selected pseudo-channel. The controller may also send two WR commands to both pseudo-channels in parallel, so that MDB will continuously drive MDQ/MDQS on both pseudo-channels.

In Rank mode, for MDQ/MDQS test on the DRAM interface, the test sequence is as below:

1. Configure LFSR control words
  - For access to Rank 0 or Rank 1 in Port-A, LFSR0 in [PG\[8\]RWE3](#) and LFSR1 in [PG\[8\]RWE4](#)
  - For access to Rank 2 or Rank 3 in Port-B, LFSR0 in [PG\[8\]RWE9](#) and LFSR1 in [PG\[8\]RWEA](#)
2. Enable Continuous Burst mode by setting [RW90\[0\]](#) to 1
3. Enable MWD training mode in [RW83](#)
4. To run the continuous burst on MDQ/MDQS, the controller sends one WR command to one of the four DRAM ranks, so that MDB will continuously drive the corresponding MDQ/MDQS.

Then the MDB will start the pattern output on MDQ/MDQS and will automatically continue to output the appropriate pattern until it is stopped by either a system reset or receiving an MRW [RW90\[0\]](#) = 0 command to disable the continuous burst mode. After the WR command in Step 4 only MRW commands are allowed.

In Mux mode, for DQ/DQS test on the Host interface, the test sequence is as below:

1. Configure LFSR control words
  - Set [PG\[10\]RWF1\[1:0\]](#) to select 8-bit or 16-bit LFSR pattern mode
  - For PS0, set the patterns in [PG\[8\]RWE3](#) and [PG\[8\]RWE4](#), or in [PG\[11\]](#)
  - For PS1, set the patterns in [PG\[8\]RWE9](#) and [PG\[8\]RWEA](#), or in [PG\[13\]](#)
2. Enable Continuous Burst mode by setting [RW90\[0\]](#) to 1
3. Enable HIR training mode in [RW83](#)
4. To run the continuous burst, the controller may send one RD command to one of the two pseudo-channels, so that MDB will drive the pattern output on DQ bus at the corresponding rising or falling edge of DQS and drive High at the other edge of DQS. The controller may also send two RD commands to both pseudo-channels in parallel, so that MDB will drive the pattern output on DQ bus at both rising and falling edges of DQS.

In Rank mode, for DQ/DQS test on the Host interface, the test sequence is as below:

1. Configure LFSR control words
  - Set [PG\[10\]RWF1\[1:0\]](#) to select 8-bit pattern mode
  - For Rank0 or Rank1 access, LFSR0 in [PG\[8\]RWE3](#) and LFSR1 in [PG\[8\]RWE4](#)
  - For Rank2 or Rank3 access, LFSR0 in [PG\[8\]RWE9](#) and LFSR1 in [PG\[8\]RWEA](#)

### 3.14 Continuous Burst Mode (cont'd)

2. Enable Continuous Burst mode by setting [RW90\[0\]](#) to 1
3. Enable HIR training mode in [RW83](#)
4. To run the continuous burst, the control sends one RD command to one of the four DRAM ranks.

Then the MDB will start the pattern output on DQ/DQS and will automatically continue to output the appropriate pattern until it is stopped by either a system reset or receiving an MRW [RW90\[0\] = 0](#) command to disable the continuous burst mode. After the RD command in step 4 only MRW commands are allowed.

Once the MRW [RW90\[0\] = 0](#) is registered by the MDB, it will stop all pattern traffic by tCont\_Exit. Since there is no min time for tCont\_Exit, the MDB may stop the pattern prior to tCont\_Exit, potentially truncating any current burst pattern. After tCont\_Exit\_Delay has expired, any other valid command is then legal. All training patterns (modes) are supported in the continuous burst mode.

Using the continuous burst mode restarts the Data Pattern/LFSR. The MDB will not store the current seed value, or the current LFSR state when it exits continuous burst mode, and it may clear the pattern values stored in [PG\[8\]RW\[EA,E9,E4,E3\]](#) or [PG\[11,13\]](#). The Host is required to program the seed/pattern again for subsequent runs. Any subsequent pattern reads will restart the seed to the programmed values of [PG\[8\]RW\[E4,E3\]](#) and [PG\[8\]RW\[EA,E9\]](#), or [PG\[11,13\]](#).

### 3.15 Static MRR Mode

DDR5MDB02 supports a Static MRR mode. It is for the Host Controller to read out the MDB internal control word bits on DQ signals prior to training on the DQ/DQS bus. The Host Controller will select the read page and byte address in [RWC0](#) and [RWC1](#). After the page and byte are selected, the Static MRR mode is enabled in the DDR5MDB02 by setting [RWC2\[7\]](#) to 1 with an MRW CMD and disabled by setting [RWC2\[7\]](#) to 0. When Static MRR mode is enabled, the DDR5MDB02 will drive the selected register result on the DQ bus instead of the training status result from any enabled MDB strobe/data training mode (see Table 40). Static MRR mode entry and exit will not cause a change in the state of any enabled training functionality (e.g., LFSR state, error counter state, etc.). While in Static MRR mode, the MDB only supports MRW commands. No other commands are allowed. Static MRR Mode is a test feature that MDB drives the 8-bit value or selected bit of a selected control word on the DQ interface continuously and asynchronously, allowing the contents to be monitored before any Host or DRAM training has taken place. The Host controller must disable Static MRR mode prior to writing [RWC0](#) or [RWC1](#).

There are two Static MRR data return formats:

- When [RWC2\[6\] = 0](#), the RW bit selected by [RWC2\[2:0\]](#) will be driven to all eight DQ bits output. The MDB continues to drive the same value until another bit is selected or Static MRR is disabled in [RWC2](#).
- When [RWC2\[6\] = 1](#), each bit of the selected RW byte will be driven to the corresponding bit of the eight DQ bits output. [RWC2\[2:0\]](#) will be ignored. RW bit 0 will be driven to DQ bit 0, RW bit 1 will be driven to DQ bit 1, and so on. The MDB continues to drive the same value until [RWC2](#) is written. In the Static MRR mode, the MDB continuously enables its DQ drivers and disables its DQ receivers and DQ termination (DQ\_RTT\_PARK). Also, the MDB disables its DQS, MDQ, and MDQS drivers and receivers and applies Park (DQS\_RTT\_PARK, MDQ\_RTT\_PARK, MDQS\_RTT\_PARK) continuously, if enabled.

Three control words are defined to support the Static MRR mode: [RWC0](#), [RWC1](#) and [RWC2](#).



### 3.15 Static MRR Mode (cont'd)

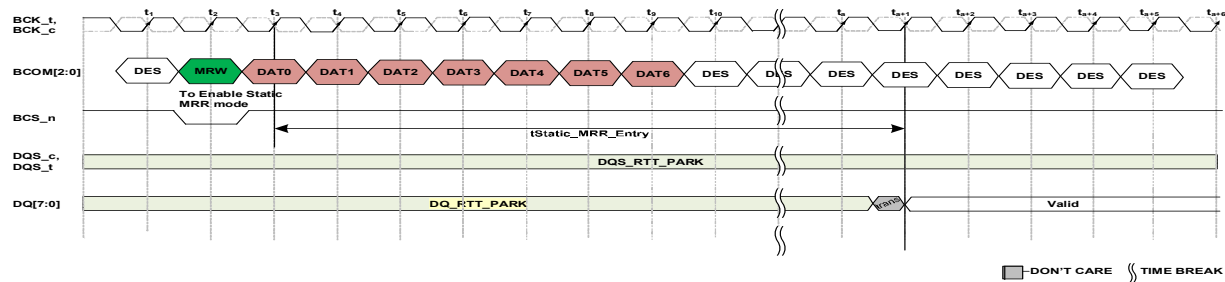


Figure 47 — Static MRR Mode Entry Diagram

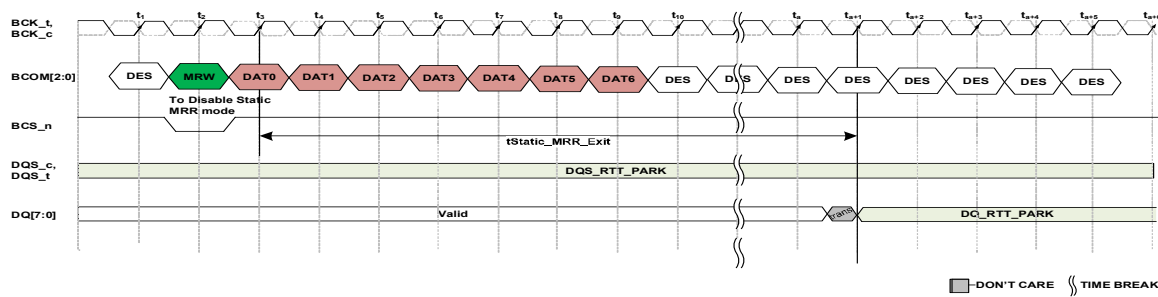


Figure 48 — Static MRR Mode Exit Diagram

#### 3.15.1 Example Static MRR Sequences

##### 3.15.1.1 Read One bit from a Control Word $RWC2[6] = 0$

As an example to read out BVref value bit 3,  $PG[2]RWFA[3]$ , the Host Controller shall use the following sequence:

1. Configure  $RWC0 = 0x02$  to select  $PG[2]$ .
2. Configure  $RWC1 = 0xFA$  to select  $PG[2]RWFA$ .
3. Configure  $RWC2 = 0x83$  to enable the Static MRR mode, and select bit 3 in the read one RW bit mode. Then wait  $t_{Static\_MRR\_Entry}$ .
4. The  $PG[2]RWFA[3]$  will be driven by MDB on  $DQ[7:0]$ .

##### 3.15.1.2 Read Multiple Bits from a Control Word $RWC2[6] = 1$ Page Control Word Read

As an example to read out Rank 1 MDQ0/4-Read delay control word,  $PG[1]RWEA$ , the Host Controller shall use the following sequence:

1. Configure  $RWC0 = 0x01$  to select  $PG[1]$ .
2. Configure  $RWC1 = 0xEA$  to select  $PG[1]RWEA$ .
3. Configure  $RWC2 = 0xC0$  to enable the Static MRR mode, and select to read eight RW bits mode. Then wait  $t_{Static\_MRR\_Entry}$ .
4. The  $PG[1]RWEA[7:0]$  will be driven by MDB on  $DQ[7:0]$ . RW bit 0 is on  $DQ[0]$ , RW bit 1 is on  $DQ[1]$ , and so on.

### 3.15.1.3 Consecutive Direct Control Word Reads

As an example to read out Internal Receive Enable Offset Fine Lower Nibble Status Control Word, [RW95](#), followed by Internal Receive Enable Offset Fine Upper Nibble Status Control Word, [RW96](#), the Host Controller shall use the following sequence:

1. Configure [RWC0](#) = 0x00.
2. Configure [RWC1](#) = 0x95 to select [RW95](#).
3. Configure [RWC2](#) = 0xC0 to enable the Static MRR mode, and select to read eight RW bits mode. Then wait  $t_{Static\_MRR\_Entry}$ .
4. The [RW95\[7:0\]](#) will be driven by MDB on DQ[7:0]. RW bit 0 is on DQ[0], RW bit 1 is on DQ[1], and so on.
5. Configure [RWC2](#) = 0x0 to disable the Static MRR mode. Then wait for  $t_{Static\_MRR\_Exit}$ .
6. Configure [RWC1](#) = 0x96 to select [RW96](#).
7. Configure [RWC2](#) = 0xC0 to enable the Static MRR mode, and select to read eight RW bits mode. Then wait  $t_{Static\_MRR\_Entry}$ .
8. The [RW96\[7:0\]](#) will be driven by MDB on DQ[7:0]. RW bit 0 is on DQ[0], RW bit 1 is on DQ[1], and so on.

### 3.15.2 MRR Static Mode Exit

The Host Controller shall use the following sequence to restore the control word settings after reading out the target control word bit or bits.

1. Configure [RWC2](#) = 0x00 (this must be written first)
2. Configure [RWC1](#) = 0x80
3. Configure [RWC0](#) = 0x00

## 3.16 Dual Frequency Support

The DDR5 MDB supports operation at a second, i.e. lower than nominal, frequency as a means to save MRCD/MDB and DRAM power when the memory bandwidth demand allows. To enable fast frequency switching without the need for retraining every time the frequency is changed, the DDR5MDB02 can be trained at two, or more, different frequencies at boot up time. When only two frequencies need to be supported, the DDR5MDB02 can retain register settings associated with each of the two frequencies. The two sets of MDB registers are listed in Table 11. The MDB hardware will take care of updating any other frequency-dependent internal settings in each frequency context as needed. In cases where more than two frequencies of operation are necessary, MDB training information will need to be stored in memory space available to the Host controller for this purpose since the DDR5MDB02 device only contains two sets of frequency context registers.

**Table 11 — Control Words Duplicated for Frequency Context Support**

Register	Description
<a href="#">RW86</a>	DQS RTT Park Termination Control Word
<a href="#">RW87</a>	Host Interface DQ RTT Termination Control Word
<a href="#">RW8A</a>	Host Interface DQ Driver Control Word
<a href="#">RW8B</a>	DRAM Interface MDQ Driver Control Word
<a href="#">RW8C</a>	MDQS and MDQ Park Termination Control Word
<a href="#">RW8F</a>	Host Interface Read DQS Offset Timing Control Word
<a href="#">RWA0</a>	DFE Control Word Control Word
<a href="#">RWB0[0]</a>	DRAM $t_{DQS2DQ}$ tracking mode selection

**Table 11 — Control Words Duplicated for Frequency Context Support (cont'd)**

Register	Description
PG[73:72, 1:0]RWE0	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable
PG[73:72, 1:0]RWE1	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling
PG[73:72, 1:0]RWE2	Lower Nibble DRAM Interface Receive Enable training control
PG[73:72, 1:0]RWE3	Upper Nibble DRAM Interface Receive Enable training control
PG[73:72, 1:0]RWE4	Lower Nibble MDQS Read delay control
PG[73:72, 1:0]RWE5	Upper Nibble MDQS Read delay control
PG[73:72, 1:0]RWE6	Lower Nibble MDQ Write Baseline delay control
PG[73:72, 1:0]RWE7	Upper Nibble MDQ Write Baseline delay control
PG[73:72, 1:0]RWE8	Lower Nibble DRAM Interface Write Leveling control
PG[73:72, 1:0]RWE9	Upper Nibble DRAM Interface Write Leveling control
PG[73:72, 1:0]RW[ED:EA]	MDQ0/4, MDQ1/5, MDQ2/6, MDQ3/7 - Read Delay control
PG[73:72, 1:0]RW[F1:EE]	MDQ0/4, MDQ1/5, MDQ2/6, MDQ3/7 - Write Delay control
PG[2]RW[E7:E0]	Host DQ Vref
PG[2]RW[F3:F0]	DRAM MDQ Vref
PG[2]RWFA <sup>1</sup>	BCOM Vref
PG[5:4]RW[E0, E8, F0, F8]	DQ[7:0] Receiver DFE Gain Offset
PG[5:4]RW[E1, E9, F1, F9]	DQ[7:0] Receiver DFE Tap 1 Coefficients
PG[5:4]RW[E2, EA, F2, FA]	DQ[7:0] Receiver DFE Tap 2 Coefficients
PG[5:4]RW[E3, EB, F3, FB]	DQ[7:0] Receiver DFE Tap 3 Coefficient
PG[5:4]RW[E4, EC, F4, FC]	DQ[7:0] Receiver DFE Tap 4 Coefficients
PG[5:4]RW[E5, ED, F5, FD]	DQ[7:0] Receiver DFE Tap 5 Coefficient
PG[5:4]RW[E6, EE, F6, FE]	DQ[7:0] Receiver DFE Tap 6 Coefficients
PG[7B]RW[E0,E4,E8,EC,F0,F4,F8,FC]	DQ[7:0] Receiver DFE Tap 7 Coefficient
PG[7B]RW[E1,E5,E9,ED,F1,F5,F9,FD]	DQ[7:0] Receiver DFE Tap 8 Coefficients
PG[71, A]RW[EF:E8]	Initial DRAM DQS Clock Tree Delay of PS1 and PS0, or {R3, R2} group and {R1, R0} group.
PG[71, A]RW[FF:F8]	Current DRAM DQS Clock Tree Delay of PS1 and PS0, or {R3, R2} group and {R1, R0} group.
PG[C]RW[E4:E1]	Per-nibble DCA Adjustments
PG[C]RW[FD:F8, F5:F0]	Per-pin DCA Adjustments
PG[D]RWE0[1:0], PG[D]RWE1, PG[D]RWE2[0], PG[D]RW[F8:F0]	Rx CTLE Control Words
PG[F]RW[FD,F8:F0]	CRC lane DFE tap 1-8 control
PG[70]RWE2	Host Interface DQS Driver Control Word
PG[70]RWE3	DRAM Interface MDQS Driver Control Word
PG[70]RWE8[3:0]	DFE Tap 8/7/6/5 Enable
PG[70]RW[F6:F4]	Extended preamble and continuous toggling mode Control Words
PG[70]RWF9[7, 3:0]	Programmable Read Delay

NOTE 1 The BCOM Vref does not need to be changed across the frequency range. It is required that BCOM Vref is programmed to the same value for both contexts.

### 3.16 Dual Frequency Support (cont'd)

Switching between the two frequency contexts is achieved by writing to control word [RW84](#). [RW84\[6\]](#) = 0 selects the default Frequency Context 1 while [RW84\[6\]](#) = 1 selects Frequency Context 2. Changing the setting in [RW84\[6\]](#) by itself only affects which copy of frequency dependent registers responds to MRW writes and MRR reads. However, when [RW84\[6\]](#) is different from the value it had in the previous Exit from Clock Stop event, any updates in [RW84\[3:0\]](#), [RW85](#), and the dual-context registers listed in Table 11 will not be applied internally in the MDB until after the MDB and DRAMs have entered and exited Self Refresh with Clock Stop mode. The MDB will use the value of [RW84\[6\]](#) at the time of Exit from Self Refresh with Clock Stop to determine which context to switch to. A context switch only occurs when the value of [RW84\[6\]](#) is different from the value it had in the previous Exit from Self Refresh with Clock Stop event.

#### 3.16.1 Input Clock Frequency Change

Once the DDR5MDB02 is initialized, the DDR5MDB02 requires the clock to be stable during almost all states of normal operation. This means that, once the clock frequency has been set and is in a stable state, the clock period must not deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate only by going through Self Refresh with Clock Stop power down mode. The sequence must allow the Host controller to update the frequency dependent registers in the background during normal operation. The sequence of steps for an input frequency change to an MRDIMM is outlined below.

1. Set [RW05\[6\]](#) in MRCD space to choose a frequency context different from the current one. At the same time update the Frequency Information settings for the next operating speed in [RW05\[4:0\]](#). These updates will only be applied internally after the MRCD exits from Self Refresh with Clock Stop.
2. Set [RW84\[6\]](#) in MDB space to choose a frequency context different from the current one. At the same time, update the Frequency Information settings for the next operating speed in [RW84\[4:0\]](#). These updates will only be applied internally after the MDB exits from Self Refresh with Clock Stop.
3. Write Fine Granularity Frequency information in MRCD space for the next operating speed in [RW06](#). The new setting will only be applied internally after the MRCD exits from Self Refresh with Clock Stop.
4. Write Fine Granularity Frequency information in MDB space for the next operating speed in [RW85](#). The new setting will only be applied internally after the MDB exits from Self Refresh with Clock Stop.
5. Set new values for the frequency specific registers listed in Table 11—as well as the MRCD frequency specific settings—in the background as needed during normal operation. These changes will only be applied internally after the MDB and MRCD exit from Self Refresh with Clock Stop mode.
6. Go through Entry and Exit from Self Refresh with Clock Stop. The MDB and the MRCD will apply the new settings upon Exit from Self Refresh with Clock Stop.

With the exception of Self Refresh Entry, normal DRAM traffic and operations are supported intermingled with Steps 3, 4, and 5 of the transition sequence defined above.

### 3.17 Rx CTLE for Host Interface DQ

In DDR5MDB02, Rx CTLE for Host Interface DQ signals and DQS1 as CRC is required. The Rx CTLE settings are encoded in control words [PG\[D\]RW\[F8:F0\]](#). The Host controller can step through all possible combinations of the Rx CTLE settings and choose the settings that is best optimized for the system based on the performance metric of interest.

### 3.17.1 CTLE Setting Definitions

The equation below represents the CTLE transfer function implemented in the DDR5MDB02 device.

$$\frac{A_{dc} \left( 1 + \frac{s}{Z} \right)}{\left( 1 + \frac{s}{P_1} \right) \left( 1 + \frac{s}{P_2} \right)}$$

Where

- $A_{dc}$  is the gain of the CTLE at DC
- $Z$  is the location of the zero,
- $P_1$  is the location of the first pole
- $P_2$  is the location of the second pole.

The device revision can only support one of the CTLE Configuration Ranges: A, B, C, or D. The Host can read out the supported range from the CTLE Configuration Control Word, [PG\[D\]RWE0\[7:5\]](#).

**Table 12 — CTLE Configuration Settings<sup>1</sup>**

Range	CW Bits OP[3:0] in <a href="#">PG[D]RW[F7:F0]</a>	Gain ( $A_{dc}$ ) <sup>2</sup>	Zero (Z) [GHz]	Pole 1 ( $P_1$ ) [GHz]	Pole 2 ( $P_2$ ) [GHz]
A	0000 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	0001 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	0010 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	0011 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	0100 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	0101 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	0110 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	0111 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	1000 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	1001 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	1010 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	1011 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	1100 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	1101 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	1110 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$
	1111 <sub>B</sub>	$VS_A$	$VS_A$	$VS_A$	$VS_A$

**Table 12 — CTLE Configuration Settings<sup>1</sup> (cont'd)**

Range	CW Bits OP[3:0] in PG[D]RW[F7:F0]	Gain ( $A_{dc}$ ) <sup>2</sup>	Zero (Z) [GHz]	Pole 1 ( $P_1$ ) [GHz]	Pole 2 ( $P_2$ ) [GHz]
B	0000 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	0001 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	0010 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	0011 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	0100 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	0101 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	0110 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	0111 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	1000 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	1001 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	1010 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	1011 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	1100 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	1101 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	1110 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
	1111 <sub>B</sub>	$VS_B$	$VS_B$	$VS_B$	$VS_B$
C	0000 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	0001 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	0010 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	0011 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	0100 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	0101 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	0110 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	0111 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	1000 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	1001 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	1010 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	1011 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	1100 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	1101 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	1110 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$
	1111 <sub>B</sub>	$VS_C$	$VS_C$	$VS_C$	$VS_C$

**Table 12 — CTLE Configuration Settings<sup>1</sup> (cont'd)**

Range	CW Bits OP[3:0] in PG[D]RW[F7:F0]	Gain ( $A_{dc}$ ) <sup>2</sup>	Zero (Z) [GHz]	Pole 1 ( $P_1$ ) [GHz]	Pole 2 ( $P_2$ ) [GHz]
D	0000 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	0001 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	0010 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	0011 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	0100 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	0101 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	0110 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	0111 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	1000 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	1001 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	1010 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	1011 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	1100 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	1101 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	1110 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$
	1111 <sub>B</sub>	$VS_D$	$VS_D$	$VS_D$	$VS_D$

NOTE 1 The Gain, Zero and Pole values are vendor specific. For the four ranges, these values are  $VS_A$  (Vendor Specific A),  $VS_B$  (Vendor Specific B),  $VS_C$  (Vendor Specific C),  $VS_D$  (Vendor Specific D).

NOTE 2 The  $A_{dc}$  gain parameter is implemented by overriding the DFE Gain coefficient settings in PG[5:4]RW[E0,E8,F0,F8] and PG[F]RW[F8]. When CTLE is enabled in a given receiver through PG[D]RWE0[0], PG[D]RWE1[7:0] and PG[D]RWE2[0], the gain settings for that receiver are determined only by the values programmed in PG[D]RW[F8:F0], and the values in PG[5:4]RW[E0,E8,F0,F8] and PG[F]RW[F8] are ignored for that receiver. This applies regardless of any one or more of the following features being enabled or disabled: DFE, DFE Training, or DFE Training Acceleration.

### 3.18 ODT Functional Description

- DQ only has one RTT value which is RTT\_PARK

- DQS only has one RTT value which is DQS\_RTT\_PARK.

- The value for DQ *RTT\_PARK* is preselected via RW87[2:0]
- The value for DQS *DQS\_RTT\_PARK* is preselected via RW86[7:4, 2:0]
- DQS\_RTT\_PARK when terminating is based on the value programmed in the RW listed above.

### 3.18.1 ODT tADC Clarifications

$t_{ADC}$  is defined as the time it takes for the Data Buffer to transition from one RTT state to the next RTT state. In case of the read, it is the time from the RTT state to the Data Buffer Drive state. Unless the RTT is specifically disabled, no High-Z state shall be allowed during  $t_{ADC}$ . During Data Buffer Drive state, the Data Buffer RON shall keep the DQ signal HIGH prior to the first DQ transition. The 8-tap DFE should assume that 8UI prior to D0 the signal is HIGH. The following figure shows a Rank mode example. In Mux mode, the BCK frequency is only half of what is shown.

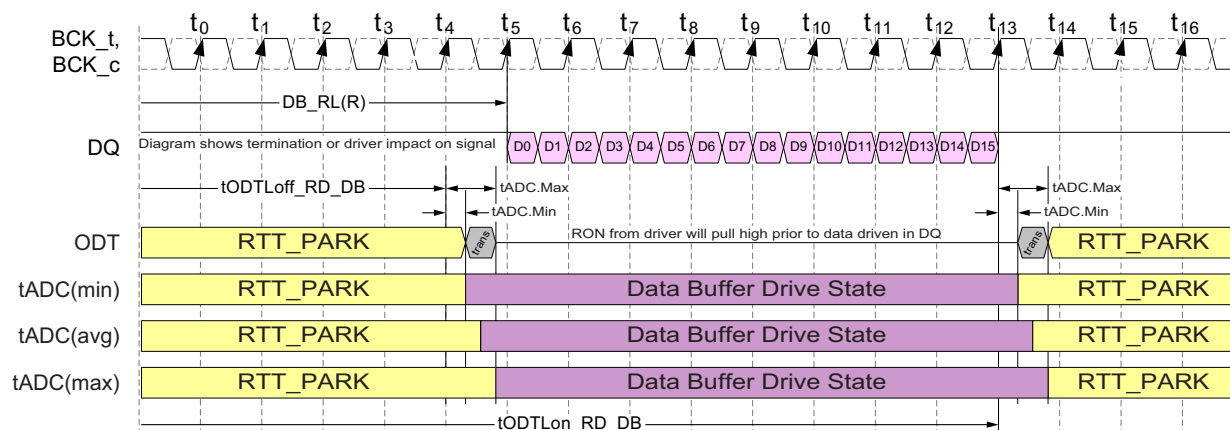


Figure 49 — Example of  $t_{ADC}$

Table 13 — Latencies and Timing Parameters Relevant for ODT when DRAM CRC is Disabled

Symbol	Parameter	Conditions	DDR5-6400 to 12800	Unit	Note
$t_{ODTLoFF\_RD\_DB}$	Data Termination Disable	<b>From:</b> Registering BCOM bus target read command <b>To:</b> Disables the termination upon driving data	Data Termination Disable = $DB\_RL + tPDM\_RD\_RA - 1 t_{HDQS}$	ns	1,2
$t_{ODTLon\_RD\_DB}$	Data Termination Enable	<b>From:</b> Registering BCOM bus target read command <b>To:</b> Re-enables the termination after driving data	Data Termination Enable = $DB\_RL + BL/2 + tPDM\_RD\_RA$	ns	1,2
$t_{ODTLoFF\_RD\_DQS\_DB}$	Strobe Termination Disable	<b>From:</b> Registering BCOM bus target read command <b>To:</b> Disables the termination upon driving strobe	Strobe Termination Disable = $DB\_RL - tRPRE[H] + tPDM\_RD\_RA - 1 t_{HDQS} - \text{Read DQS OFFSET}$	ns	1,2
$t_{ODTLon\_RD\_DQS\_DB}$	Strobe Termination Enable	<b>From:</b> Registering BCOM bus target read command <b>To:</b> Re-enables the termination after driving strobe	Strobe Termination Enable = $DB\_RL + BL/2 + tRPST[H] - 0.5 t_{HDQS} + tPDM\_RD\_RA - \text{Read DQS OFFSET}$	ns	1,2
$t_{ADC}$	RTT change skew	<b>From:</b> Transitioning from RTT State to non-termination State or Transitioning from non-termination State to RTT termination State. <b>To:</b> RTT valid	$t_{ADC}(\min) = 0.2$ $t_{ADC}(\max) = 0.8$	$t_{HDQS}$ (avg)	3

NOTE 1 For simplicity, Reads are assigned the same type of timing parameter; however, unlike others, it is a fixed timing and does not have an offset control word to control it. To indicate this, it was named Data (or Strobe) Termination Disable and Enable.

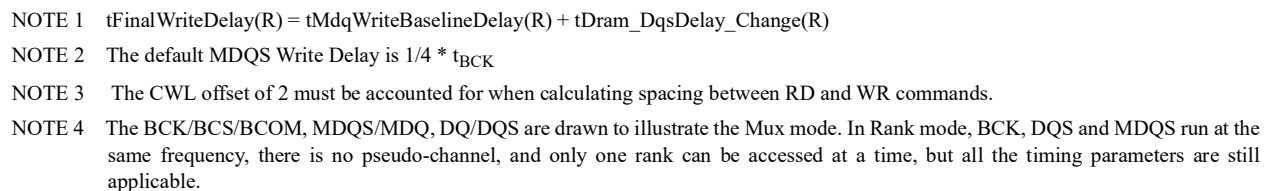
NOTE 2 In Mux mode,  $DB\_RL$  is different per pseudo-channel and per rank. In Rank mode, it is different per rank.

NOTE 3  $t_{HDQS}$  is half cycle time of BCK in Mux mode, or whole cycle time of BCK in Rank mode.



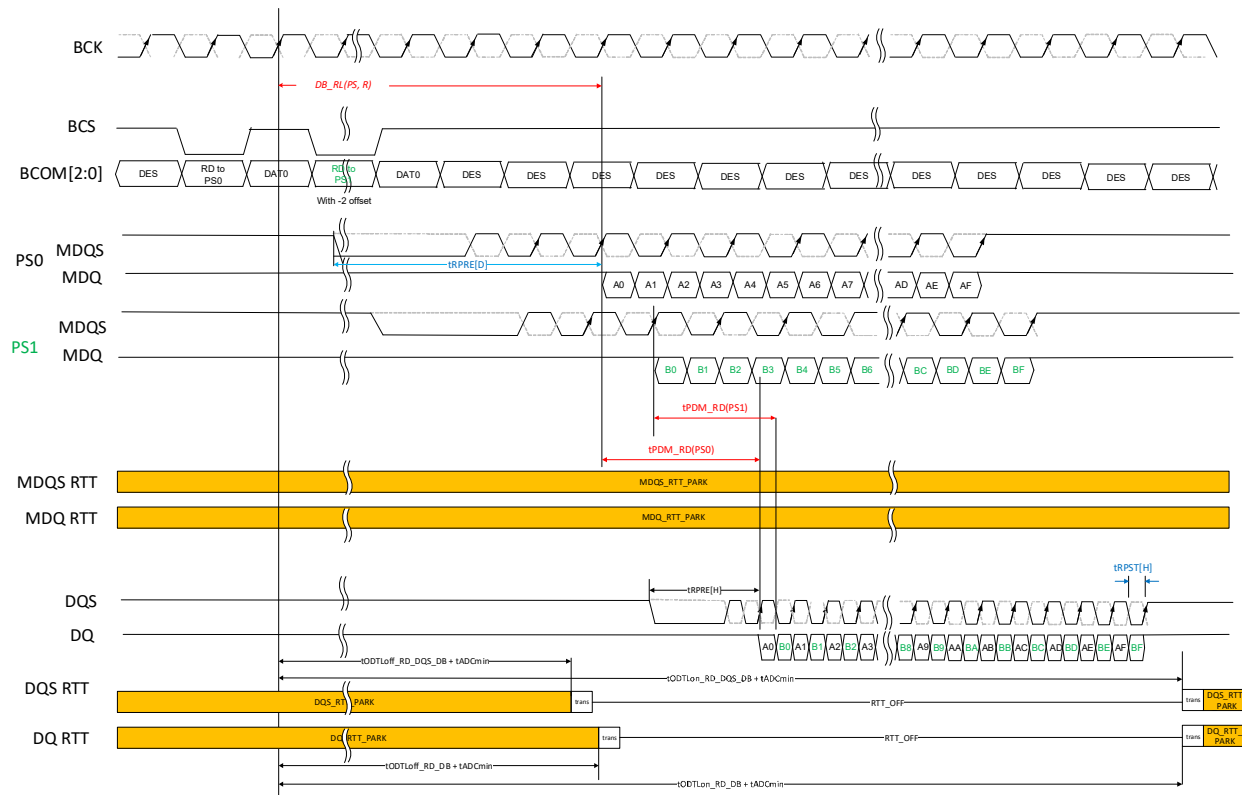
It is the controller's responsibility to manage command spacing and the programmable aspect of tODLon/off times to ensure that preambles and postambles are included in the RTT ON time.

All timings noted in Figure 50 and Figure 51 are used as reference.



**Figure 50 — Example of Burst Write Operation ODT Latencies**

### 3.18.2 ODT Timing Diagrams (cont'd)



NOTE 1 The default MDQS Read Delay is  $(1+1/4) * t_{BCK}$  for unmatched receivers case, or  $1/4 * t_{BCK}$  for matched receivers case.

NOTE 2 The CWL offset of 2 must be accounted for when calculating spacing between RD and WR commands.

NOTE 3 The BCK/BCS/BCOM, MDQS/MDQ, DQ/DQS are drawn to illustrate the Mux mode. In Rank mode, BCK, DQS and MDQS run at the same frequency, there is no pseudo-channel, and only one rank can be accessed at a time, but all the timing parameters are still applicable.

**Figure 51 — Example of Burst Read Operation ODT Latencies**

### 3.19 Host Interface Duty Cycle Adjuster (DCA)

DDR5MDB02 supports a control word adjustable DCA to allow the memory controller to adjust the MDB internally generated DQS clock tree and DQ duty cycle to compensate for systemic duty cycle error of all Host Interface DQS and DQs.

The DQS DCA is located before the DQS clock tree or equivalent place. The DCA requires a locked DLL state and will affect DQS and DQ duty cycle during the following operations:

- Read
- Read Training in HIR/HPA modes
- Mode Register Read

The controller can adjust the duty cycle through all the DCA control words and can determine the optimal control word setting for DCA in multiple different ways.

The DCA Configuration read-only register bit ([PG\[C\]RWE0\[0\]](#)) can be read by the Host to determine the vendor-specific DCA functional configuration that is supported.

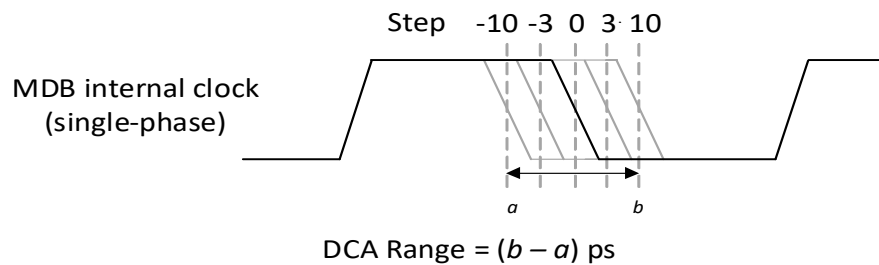
### 3.19.1 Duty Cycle Adjuster Range

When *DCA Configuration\_0* is supported (**PG[C]RWE0[0] = 0**). The per-nibble DCA step range is from -7 to +7, with an additional per-pin adjustment of -3 to +3, for a total range of -10 to +10.

When *DCA Configuration\_1* is supported (**PG[C]RWE0[0] = 1**). The per-nibble DCA step range for differential DQS\_t/c is -7 to +7, and per-pin DQS\_t and DQS\_c DCA adjustment is not supported. For DQ bits, the per-pin DCA step range is -7 to +7, and per-nibble DQ DCA adjustment is not supported.

The actual step size cannot be defined since the variation of duty cycle by changing DCA code is not linear.

The DCA Range is defined as shown in Figure 52, which uses *DCA Configuration\_0* as an example. If *a* is the location of the falling edge with the most negative step adjustment, and *b* is the falling edge with the most positive step adjustment, the DCA Range is (*b - a*), measured in ps.



**Figure 52 — Duty Cycle Adjuster Range**

The total DCA Range must be within the Max/Min in Table 14, which guarantees that the step size granularity and maximum adjustment, as a percentage of clock period, both fall within acceptable limits.

**Table 14 — DCA Range**

Parameter	Min/Max	Value	Unit	NOTE
Duty Cycle Adjuster Range	Min	7	ps	1
	Max	32		

NOTE 1 These values are guaranteed by design.

### 3.19.2 Relationship between DCA Code Change, Internal Clock(s), and DQ[S] Timing

The internal clock(s) controlled by the DCA code are those that control the timing of the DQ/DQS transmission. The rising edge is the reference edge. This corresponds to even burst data bits. The falling edge is adjusted based on the DCA code. This edge can also be considered the rising edge of a 180° clock, and corresponds to odd burst data bits. Therefore, when *DCA Configuration\_0* is supported (**PG[C]RWE0[0] = 0**), a change in the DCA code will produce a corresponding change in one or multiple of the following: the falling edge of DQS\_t, the rising edge of DQS\_c, and the launch time of odd-numbered UIs of DQ bits. When *DCA Configuration\_1* is supported (**PG[C]RWE0[0] = 1**), a change in the DCA code will produce a corresponding change in one or multiple of the following: the falling edge of the differential DQS\_t/c, and the launch time of odd-numbered UIs of DQ bits.

A positive DCA adjustment results in a larger duty cycle ratio, while a negative DCA adjustment results in a smaller duty cycle ratio.

When *DCA Configuration\_0* is supported (**PG[C]RWE0[0] = 0**), the per-nibble DCA adjustment is in the DCA control word bits **PG[C]RW[E1,E3]** for DQS\_t/c and **PG[C]RW[E2,E4]** for the DQ bits. When *DCA Configuration\_1* is supported (**PG[C]RWE0[0] = 1**), the per-nibble DCA adjustment for differential DQS\_t/c is in the DCA control word bits **PG[C]RW[E1,E3]**, and per-nibble DCA adjustment for DQ bits is not supported.

### 3.19.2 Relationship between DCA Code Change, Internal Clock(s), and DQ[S] Timing (cont'd)

When in x8 mode on the Host side with [PG\[70\]RWF0\[1\]](#) set, only the per-nibble DQS0 adjustment in [PG\[C\]RWE1](#) and the per-pin DQS0\_t/c adjustment in [PG\[C\]RW\[F0,F1\]](#) (only in *DCA Configuration\_0*) are used. [PG\[C\]RWE3](#) and [PG\[C\]RW\[F8,F9\]](#) are ignored.

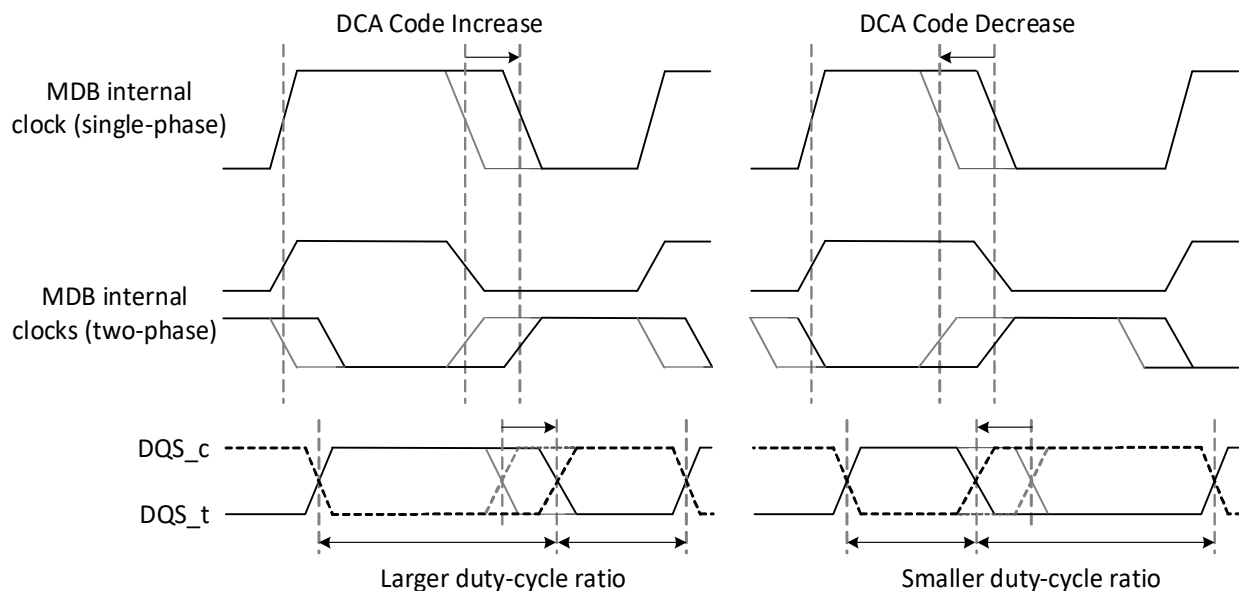
When *DCA Configuration\_0* is supported ([PG\[C\]RWE0\[0\] = 0](#)), the per-pin DCA adjustment is in the control word bits [PG\[C\]RWF0](#) to [PG\[C\]RWF5](#) and [PG\[C\]RWF8](#) to [PG\[C\]RWFD](#). The per-pin DCA adjustment is additive to the per-nibble DCA adjustment, as shown in the examples below:

**Table 15 — DCA Range Examples (not all possible combinations) when [PG\[C\]RWE0\[0\] = 0](#)**

Per-Nibble DCA Adjustment	Per-Pin DCA Adjustment	Total DCA Adjustment at Pin
DCA Step -7	DCA Step -3	DCA Step -10
DCA Step -2	DCA Step +2	DCA Step 0
DCA Step 0	DCA Step +1	DCA Step +1
DCA Step +2	DCA Step -3	DCA Step -1
DCA Step +4	DCA Step +3	DCA Step +7
DCA Step +7	DCA Step +3	DCA Step +10

When *DCA Configuration\_1* is supported ([PG\[C\]RWE0\[0\] = 1](#)), the per-pin DCA adjustment for DQ bits is in the control word bits [PG\[C\]RWF2](#) to [PG\[C\]RWF5](#) and [PG\[C\]RWF8](#) to [PG\[C\]RWFD](#), and per-pin DCA adjustment for DQS\_t and DQS\_c is not supported. As mentioned previously, per-nibble DCA adjustment for DQ bits is not supported.

Like the per-nibble DCA adjustment, the actual step size for the per-pin DCA adjustment cannot be defined since the variation of duty cycle by changing DCA code may not be linear. However, the per-pin DCA adjustment will be approximately the same as the per-nibble DCA adjustment.



**Figure 53 — Relationship between DCA Code Change and the Single/two-phase Internal Clock(s)/DQS Waveform (Example)**

### 3.20 DRAM Periodic Update Support

To track the DRAM  $t_{DQS2DQ}$  drift per rank, a tracking mechanism is required to periodically monitor this drift and update the respective MDQ-MDQS write delay settings in the MDB as required to compensate for the drift.

In the Rank mode, the interval oscillator updates are done on a per rank basis. In the Mux mode, the interval oscillator updates are done on a per rank and per pseudo-channel basis. The PS0 DQS2DQ calculation is triggered by the PS0 read of MR47. The PS1 DQS2DQ calculation is triggered by the PS1 read of MR47.

#### 3.20.1 DRAM $t_{DQS2DQ}$ Tracking Modes

- DRAM  $t_{DQS2DQ}$  tracking initialization mode
- DRAM  $t_{DQS2DQ}$  tracking mode

In the Rank mode, prior to performing DRAM  $t_{DQS2DQ}$  tracking, the MDB requires the Host to issue an MPC to start a DQS interval oscillator measurement for each DRAM rank. The MDB supports four ranks of DRAM  $t_{DQS2DQ}$  tracking per nibble. PG[A] control words are used for rank 0 and rank 1 tracking. PG[71] control words are used for rank 2 and rank 3 tracking.

In the Mux mode, prior to performing DRAM  $t_{DQS2DQ}$  tracking, the MDB requires the Host to issue an MPC to start a DQS interval oscillator measurement for each DRAM rank of each pseudo-channel. The MDB supports two ranks of DRAM  $t_{DQS2DQ}$  tracking per pseudo-channel and per nibble. PG[A] control words are used for rank 0 and rank 1 tracking of PS0. PG[71] control words are used for rank 0 and rank 1 tracking of PS1.

- The *DRAM  $t_{DQS2DQ}$  tracking initialization mode* is used to calculate the initial DQS clock tree delay value for each DRAM nibble and rank in PG[71,A]RW[EF:E0]. The MDB stores these values for later use during the DRAM  $t_{DQS2DQ}$  tracking mode. DRAM  $t_{DQS2DQ}$  tracking initialization on the MDB only needs to be done by the Host once after MDQ-MDQS Write Delay Training completes, since any delay adjustment due to drift is with respect to the trained values.
- The *DRAM  $t_{DQS2DQ}$  tracking mode* is used to calculate the current DQS clock tree delay value for each DRAM nibble and rank stored in PG[71,A]RW[FF:F0]. These are used to calculate the timing drift relative to their respective initial delay values, and then to update their respective MDQ-MDQS write delay values for drift compensation. DRAM  $t_{DQS2DQ}$  tracking is performed periodically by the Host as a function of system conditions. All operations, commands, and features are supported when tracking mode is enabled in RWB0[0] excepting during calculation window tTrkCalcCur.

#### 3.20.2 Operational Requirements

The following describes the operational requirements associated with the DRAM  $t_{DQS2DQ}$  tracking feature:

- The MDB initially enters the DRAM  $t_{DQS2DQ}$  tracking initialization mode as a result of power-on initialization. When a DRAM-space MRR read to MR47 is received, the MDB will trigger a calculation update for the tracking initialization mode. It is the Host's responsibility to issue the MPC command to start the DRAM DQS oscillator and to issue a DRAM-space MRR read to MR46 prior to issuing a DRAM-space MRR read to MR47.
- The MDB supports DB-space MRW operations to any register address while in either tracking mode except during a DQS clock tree delay calculation period. The Host must make sure that these MRW operations do not interfere with any tracking-related settings or processes.
- The MDB supports snooping of the DRAM-space MRW to the DRAM's DQS interval oscillator control register to obtain the DRAM's run-time count value needed for DQS clock tree calculations. The Host must configure the DRAM to perform automatic stop based on its run-time count. The snooped value is loaded into the MDB's DQS Interval Timer Run Time MR45 register PG[8]RWE7. In Mux mode, the run-time count snooped value is shared by both PS0 and PS1.

### 3.20.2 Operational Requirements (cont'd)

- The read data format of the DRAM-space MRR is assumed to be the same as defined for the DB-space MRR.
- The MDB supports DB-space MRR operations to any register address while in either tracking mode except during a DQS clock tree delay calculation period.
  - The initial and current DRAM DQS OSC Counter values captured by the MDB from each DRAM nibble and rank are readable by the Host via DB-space MRR.
  - The initial and current DRAM DQS clock tree delay values calculated by the MDB for each DRAM nibble and rank are readable by the Host via DB-space MRR.
- The Host must read DRAM OSC Counter LSB [MR46](#) and MSB [MR47](#) registers sequentially as an {LSB, MSB} pair from the same rank. Upon issuing a DRAM-space read to [MR47](#), the Host must block all transactions to all ranks for the duration of  $t_{TrkCalcInit}$  if in tracking initialization mode, or for the duration of  $t_{TrkCalcCur}$  if in tracking mode, to allow the MDB to complete the calculation and update of the DRAM MDQ-MDQS write delay adjustment.
- Host side read timing for rank-x is defined in the standard way as  $DB\_RL(Rx) + t_{PDM\_RD}$  after the DAT0 cycle of the DRAM-space MRR command sequence. Data is returned using DB-space MRR read format.

### 3.20.3 DRAM tDQS2DQ Tracking Initialization Mode

To initialize the reference values for subsequent DRAM tDQS2DQ tracking in the MDB, the Host performs DRAM tDQS2DQ tracking initialization only once per rank after MDQS Write Delay Training completes. After power cycle reset the MDB defaults to DRAM tDQS2DQ tracking initialization mode, or the mode can be set via a DB-space MRW to set  $RWB0[0] = 0$ . To perform the initialization the Host must first issue an MPC to start an initial DQS interval oscillator measurement for each DRAM rank (not shown).

The Host will issue two sequential DRAM-space MRR commands to [MR46](#) and [MR47](#) to read the initial values of a DRAM DQS OSC Counter LSB and MSB register pair from the same rank.

When the Host issues the first DRAM-space MRR to the DRAM DQS OSC Counter LSB register [MR46](#), the MDB captures the read data from each DRAM nibble using the read timing for the specified rank and stores the captured value for the lower nibble in  $PG[71,A]RWE0$  or  $PG[71,A]RWE2$ , and it stores the captured value for the upper nibble in  $PG[71,A]RWE4$  or  $PG[71,A]RWE6$ . The MDB will return a predefined value in [RWB1](#) to the Host.

When the Host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register [MR47](#), the MDB captures the read data from each DRAM nibble using the read timing for the specified rank and stores the captured value for the lower nibble in  $PG[71,A]RWE1$  or  $PG[71,A]RWE3$ , and it stores the captured value for the upper nibble in  $PG[71,A]RWE5$  or  $PG[71,A]RWE7$ . The MDB will return a predefined value in [RWB1](#) to the Host.

As shown in Figure 54, the Host must meet the  $t_{MRROD1}$  timing parameter between MRR operations to DRAM-space [MR46](#) and [MR47](#). In general, MRR operations to DRAM-space [MR46](#) and [MR47](#) must also be considered as DB-space MRR operations from the timing point of view since the MDB returns the contents of [RWB1](#) to the Host.

Once the DQS OSC Counter LSB and MSB values from each DRAM nibble for a particular rank are captured and stored, the MDB will then calculate the initial DQS clock tree delay for each nibble of the specified rank. The calculation starts when the capture has completed for the DRAM nibble with the latest read timing.

Once the calculation has completed, the MDB then stores the calculated value for the lower nibble in  $PG[71,A]RWE8$  and  $PG[71,A]RWE9$  or  $PG[71,A]RWEA$  and  $PG[71,A]RWEB$ , and it stores the calculated value for the upper nibble in  $PG[71,A]RWEC$  and  $PG[71,A]RWED$  or  $PG[71,A]RWEF$  and  $PG[71,A]RWEF$ . The calculate and store operations complete within  $t_{TrkCalcInit}$ .

### 3.20.3 DRAM tDQS2DQ Tracking Initialization Mode (cont'd)

From the time when the Host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register [MR47](#) to the end of the tTrkCalcInit period, only DES and NOP commands are legal. Once the period has completed for the specified rank, the MDB will remain in the tracking initialization mode as shown in Figure 54. The Host can then execute DRAM tDQS2DQ tracking initialization functions at a later time to perform the tDQS2DQ tracking initialization process to the other ranks.

At the end of DRAM tDQS2DQ Tracking Initialization, both Initial DRAM DQS Clock Tree Delay and Current DRAM DQS Clock Tree Delay share the same value. This results in tDRAM\_DqsDelay\_Change being equal to 0 which means no change to the MDQ-to-MDQS Write Delay.

As depicted in Figure 56, the tDQS2DQ Tracking Initialization Mode calculations described in the above paragraphs can also be triggered by direct MRW operations to the MSB counter values in [PG\[71,A\]RW\[E1, E3, E5, E7\]](#). In the case of direct MRW access, the tracking mode selection bit [RWB0\[0\]](#) is ignored and the Host is required to meet applicable timing parameters in Table 246.

Figure 54 shows an example in the Rank mode with the same data rate between the DRAM interface and the Host interface. In the Mux mode, the Host interface data rate is two times of the DRAM interface as described in the normal read operation.

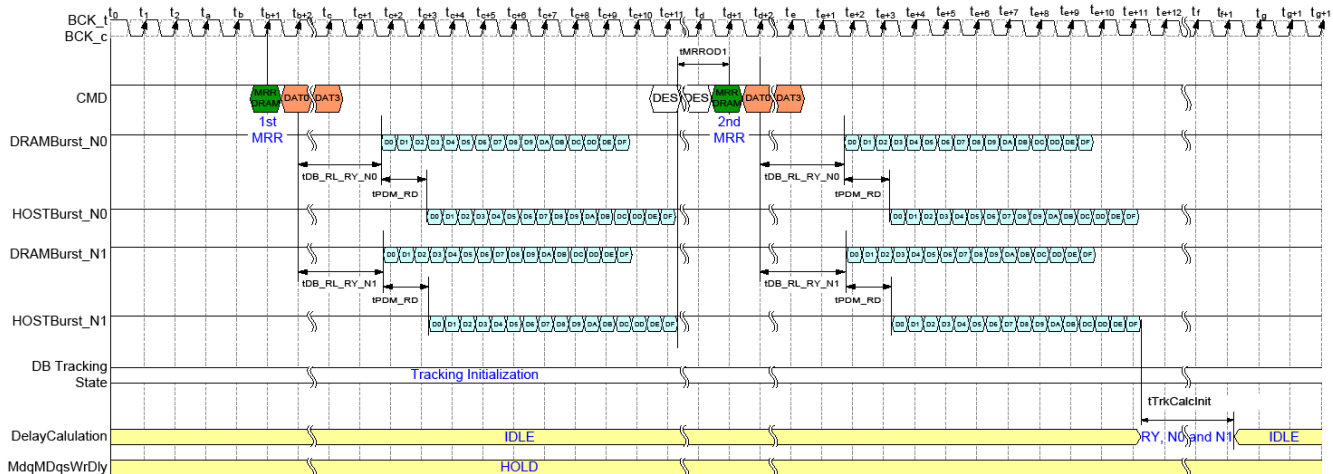


Figure 54 — DRAM tDQS2DQ Tracking Initialization Mode Flow

### 3.20.4 DRAM tDQS2DQ Tracking Mode

DRAM tDQS2DQ tracking is performed periodically by the Host as a function of system conditions. After the DRAM tDQS2DQ tracking initialization has completed, the Host must set the MDB in DRAM tDQS2DQ tracking mode via a DB-space MRW to set [RWB\[0\] = 1](#). To perform the tracking the Host shall issue an MPC to start a DQS interval oscillator measurement for each DRAM rank (not shown). After starting the DRAM DQS interval oscillator the Host will issue two sequential DRAM-space MRR commands to [MR46](#) and [MR47](#) to read the current values of a DRAM DQS OSC Counter LSB and MSB register pair from the same rank. The read process is the same as described in the Initialization mode except that different MDB registers are used for value storage.

When the Host issues the first DRAM-space MRR to the DRAM DQS OSC Counter LSB register [MR46](#), the MDB stores the captured value for the lower nibble in [PG\[71,A\]RWF0](#) or [PG\[71,A\]RWF2](#), and it stores the captured value for the upper nibble in [PG\[71,A\]RWF4](#) or [PG\[71,A\]RWF6](#). The MDB will return a predefined value in [RWB1](#).



### 3.20.4 DRAM tDQS2DQ Tracking Mode (cont'd)

As shown in Figure 55, the Host must meet the  $t_{MRROD1}$  timing parameter between MRR operations to DRAM-space [MR46](#) and [MR47](#). In general, MRR operations to DRAM-space [MR46](#) and [MR47](#) must also be considered as DB-space MRR operations from the timing point of view since the MDB returns the contents of [RWB1](#) to the Host.

When the Host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register [MR47](#), the MDB stores the captured value for the lower nibble in [PG\[71,A\]RWF1](#) or [PG\[71,A\]RWF3](#), and it stores the captured value for the upper nibble in [PG\[71,A\]RWF5](#) or [PG\[71,A\]RWF7](#). The MDB will return a predefined value in [RWB1](#).

Once the DQS OSC Counter LSB and MSB values from each DRAM nibble for a particular rank are captured and stored, the MDB will then calculate the current DQS clock tree delay for each nibble of the specified rank. The calculation starts when the capture has completed for the DRAM nibble with the latest read timing.

Once the calculation has completed, the MDB then stores the calculated value for the lower nibble in [PG\[71,A\]RWF8](#) and [PG\[71,A\]RWF9](#) or [PG\[71,A\]RWFA](#) and [PG\[71,A\]RWFB](#), and it stores the calculated value for the upper nibble in [PG\[71,A\]RWFC](#) and [PG\[71,A\]RWF7D](#) or [PG\[71,A\]RWFE](#) and [PG\[71,A\]RWFF](#). The MDB will update the applied MDQ-MDQS write delay value for each nibble of the rank based on its MDQ write baseline delay and its stored initial and current DQS clock tree delay values. The calculate, store and update operations must complete within  $t_{TrkCalcCur}$ . From the time when the Host issues the second DRAM-space MRR to the DRAM DQS OSC Counter MSB register [MR47](#) to the end of the  $t_{TrkCalcCur}$  period, only DES and NOP commands are legal.

Once the  $t_{TrkCalcCur}$  period has completed for the specified rank, the MDB will remain in tracking mode as shown in Figure 55.

As shown in Figure 57, the tDQS2DQ Tracking Mode calculations described in the above paragraphs can also be triggered by direct MRW operations to the MSB counter values in [PG\[71,A\]RW\[F1, F3, F5, F7\]](#). In the case of direct MRW access, the tracking mode selection bit [RWB0\[0\]](#) is ignored and the Host is required to meet applicable timing parameters in Table 246.

### 3.20.5 MDQ-MDQS Adjustment Calculations

The MDB is only required to support calculation for one rank at a given time, in each x4 nibble. The MDQ-MDQS write delay adjustment calculation for each nibble,  $Ny$ , of a specified rank,  $Rx$ , is as follows.

The initial count from the DRAM tDQS2DQ tracking initialization step provides the initial DRAM DQS clock tree delay in units of  $t_{BCK}/128$ :

$$t_{Dram\_DqsDelay\_Initial}(Rx, Ny) = \text{Dram\_RunTimeCount} * t_{BCK} / (2 * \text{Dram\_DQSOscCount\_Initial}(Rx, Ny)).$$

For each DRAM tDQS2DQ tracking step, the current count provides the drifted DRAM DQS clock tree delay in units of  $t_{BCK}/128$ :

$$t_{Dram\_DqsDelay\_Current}(Rx, Ny) = \text{Dram\_RunTimeCount} * t_{BCK} / (2 * \text{Dram\_DQSOscCount\_Current}(Rx, Ny))$$

The change in the DRAM DQS clock tree delay is calculated in units of  $t_{BCK}/64$ :

$$t_{Dram\_DqsDelay\_Change}(Rx, Ny) = t_{Dram\_DqsDelay\_Current}(Rx, Ny) - t_{Dram\_DqsDelay\_Initial}(Rx, Ny).$$

The MDB then updates the applied MDQ-MDQS write delay values as:

$$t_{MdqMdqWriteDelay}(Rx, Ny) = t_{MdqWriteBaselineDelay}(Rx, Ny) + t_{Dram\_DqsDelay\_Change}(Rx, Ny)$$

Each MDQ write baseline delay register is not updated from its trained value. Instead, its value is offset by its respective  $t_{Dram\_DqsDelay\_Change}$  value before being applied to the delay circuitry.



### 3.20.5 MDQ-MDQS Adjustment Calculations (cont'd)

As an example, if the current DQS clock tree delay is larger than the initial DQS clock tree delay, the DQS clock tree delay has increased by  $t_{\text{Dram\_DqsDelay\_Change}}$ , so the applied MDQ-MDQS write delay needs to be increased by this amount.

For the Final Write Delay including all offset contributors such as  $t_{\text{DRAM\_DQSDelay\_Change}}$  from Page PG[71,A] and PG[0,1,72,73]RW[EE:F1] (per-bit Write Delays), the DDR5MDB02 device is only required to support the  $-0.5 * t_{\text{BCK}}(\text{minimum})$  to  $+3.5 * t_{\text{BCK}}(\text{maximum})$  delay range defined for the Write Delay baseline control words in PG[0,1,72,73]RW[E6:E7].

In cases where control words in PG[0,1,72,73]RW[E6:E7], PG[0,1,72,73]RW[EE:F1], and Page PG[71,A] are programmed with settings that would cause any Final Write Delay value to be outside the delay range supported by the device, the MDB will saturate the effective Final Write Delay values at the maximum or minimum (as applicable) of the delay range it supports.

Figure 55 shows an example in the Rank mode with the same data rate between the DRAM interface and the Host interface. In the Mux mode, the Host interface data rate is two times of the DRAM interface as described in the normal read operation.

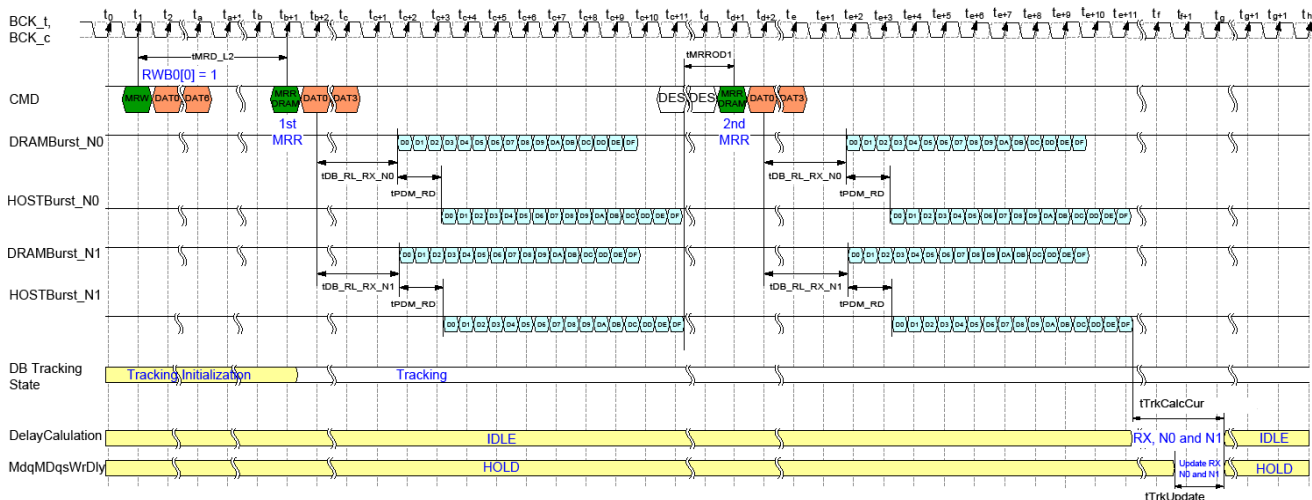


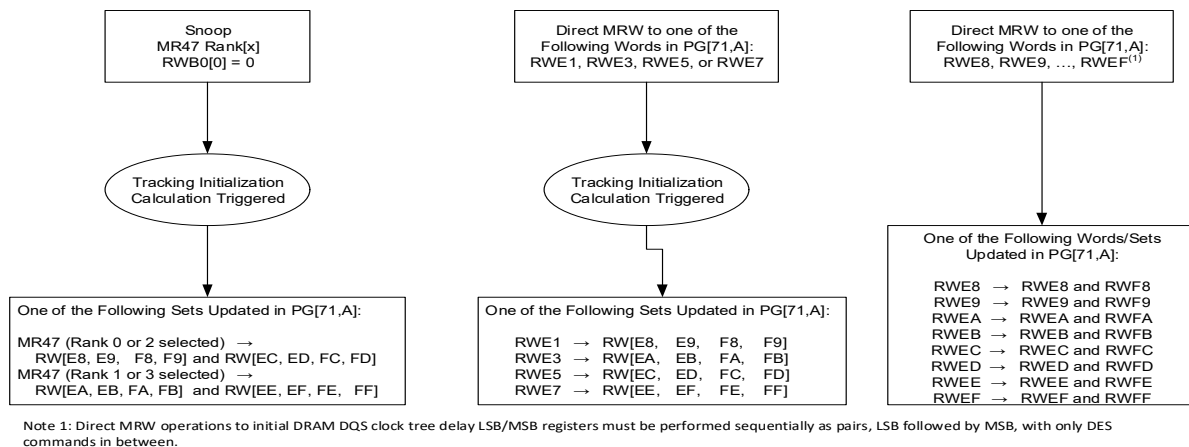
Figure 55 — DRAM  $t_{\text{DQS2DQ}}$  Tracking Mode Flow

### 3.20.6 DRAM interval Oscillator Snoop Value

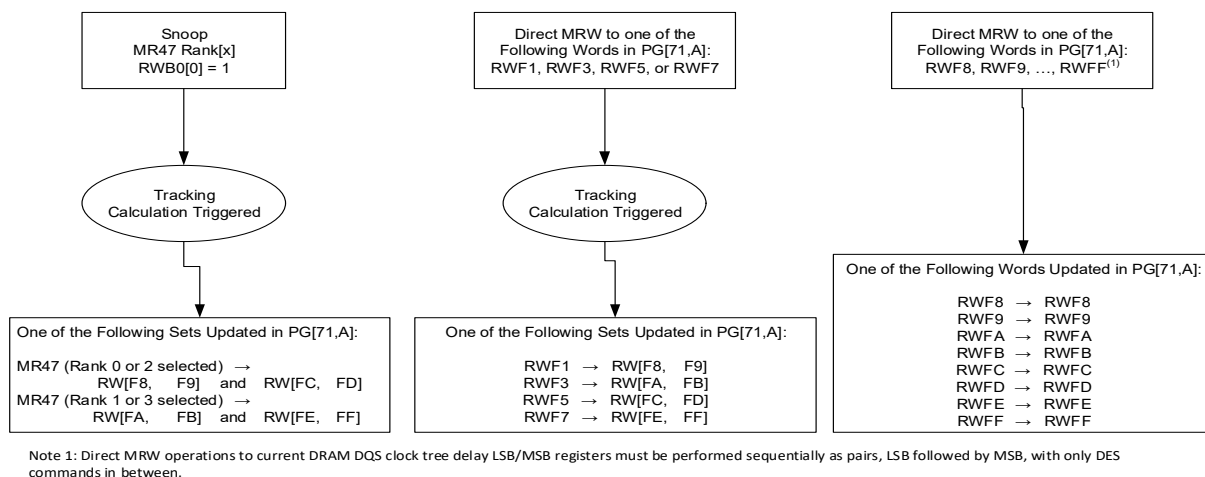
The MDB configures PG[8]RWE7 with the snooped value from a DRAM-space MRW to the DRAM's interval oscillator control register MR45. The MDB uses the snooped interval timer stop value, referred to as the run-time count value, for DRAM DQS clock tree delay calculations. The Host must make sure that the DRAM's run-time count value is configured as necessary. It must also make sure that the DRAM's interval oscillator is configured for automatic stop based on its run-time count value.

Although PG[8]RWE7 can be written directly by the Host, the intent is that it will not be written directly by the Host after it has been configured with the snooped value. Writing to this register directly is intended for debug purposes.

### 3.20.6 DRAM interval Oscillator Snoop Value (cont'd)



**Figure 56 — tDQS2DQ Tracking Initialization Sequences**



### Figure 57 — tDQS2DQ Tracking Sequences

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## 4 Self Refresh Operation

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DDR5 does not have a separate CKE signal going to the DIMM or the MDBs. Self refresh Entry is signaled via a command sequence on the BCOM interface. A BCS\_n active pulse will take the Data Buffer out of the self refresh state.

### 4.1 Self Refresh Modes

After the SRE command is received by the Data Buffer, the MDB input clock may stop as BCK\_t = BCK\_c = HIGH. When the BCK clock is running, the BCS\_n signal must remain HIGH in order for the MDB to stay in Self Refresh state. In Rank mode, there are two options for the MDB to handle the on-die terminations during Self Refresh as illustrated in Figure 60 through Figure 65. These two options are vendor specific, with no impact to the Host Controller operation.

#### 4.1.1 Self Refresh Mode with Clock Stop Entry

Self Refresh Mode is a very low power state in which the input clocks can stop and the MDB on-die terminations, including RTT\_PARK, are disabled. Self-refresh entry is signaled when the MRCD sends SRE command on the BCOM[2:0] control bus. The DDR5MDB02 uses a clock-stop detection circuit to disable the command bus BCK\_t/ BCK\_c, BCOM[2:0], and BCS\_n receivers. When the clock stops, BCK\_t and BCK\_c will be driven or pulled up HIGH, respectively, by the MRCD or by the discrete termination resistors on the module. Similarly, BCS\_n, and BCOM[2:0] signals will be pulled HIGH by the MRCD or the termination resistors. Note that the BCS\_n is NOT driven LOW when in self refresh.

The MDB will disable DQ/DQS and MDQ/MDQS on-die terminations during Self Refresh with Clock Stop. In Mux mode, the MDB rely on the clock-stop detection circuit for this purpose. In Rank mode, the MDB may disable on die terminations using the SRE command, or the MDB may also rely on the clock-stop detection circuit.

#### 4.1.2 Exit from Self Refresh Mode with Clock Stop

To exit the Clock Stop condition, the MRCD starts the BCK clocks with stable frequency and phase while keeping BCOM[2:0] and BCS\_n signals HIGH. The MDB may exit the self refresh state any time after it exits the clock stop condition and prior to tSTAB\_DB.

In Mux mode, on die terminations in the MDB get re-enabled by the exit from Clock-Stop condition directly. In Rank mode, on die terminations can get re-enabled either by the first NOP command following exit from Clock-Stop condition, or by the exit from Clock-Stop condition directly.

If the BCOM[2:0] and BCS\_n bus timings have not been trained for the current frequency of operation, after a wait of tSTAB\_DB from when the BCK clocks are toggling with stable phase and frequency, the Host is allowed to apply the “BCOMTM Entry” strap command (see Table 34) to train the BCOM[2:0] and BCS\_n signal timings.

In Rank mode, the BCS\_n signal is allowed to pulse LOW for one or more cycles (with valid timings) after a wait of tSTAB\_DB from when the BCK clocks are toggling with stable phase and frequency. In Mux mode, the single NOP never arrives, because the MRCD uses it to synchronize the clock phase. The BCK only starts after that point. A minimum of 25ns is guaranteed from the BCK re-toggling to the next multi-cycle NOP commands.

#### 4.1.3 Self Refresh Mode without Clock Stop Entry

Self Refresh without Clock Stop is similar to Self Refresh with Clock Stop mode except that the MRCD will not stop the BCK clock in this mode.

In Mux mode, the MDB device keeps on-die terminations enabled as shown in Figure 59. In Rank mode, the MDB device may disable on die terminations during Self Refresh without Clock Stop using the SRE command, or the MDB is also allowed to keep on-die terminations enabled.

4.1.4 Self Refresh Mode without Clock Stop Exit

Exiting this mode is similar to Self Refresh with Clock Stop, except that the Host will not wait  $t_{\text{STAB\_DB}}$  upon exit, as the clock circuitry in the Data Buffer stays locked.

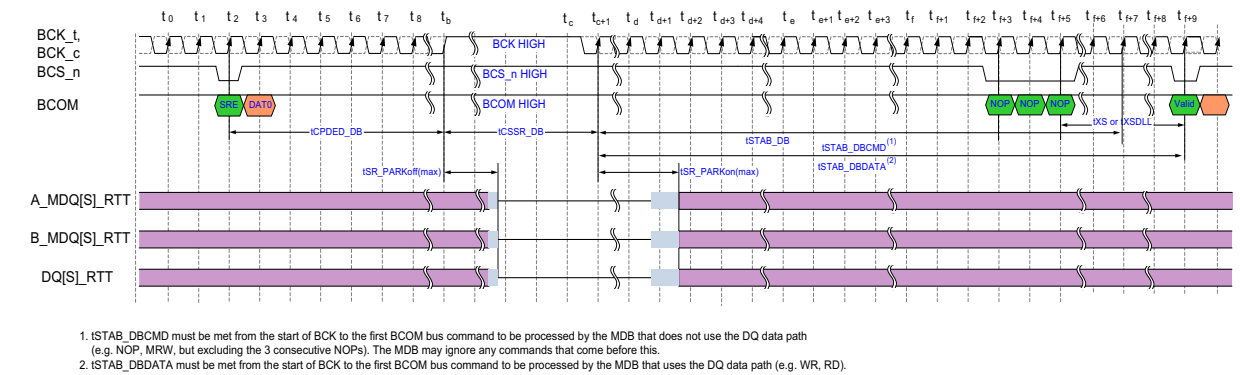


Figure 58 — Mux Mode Self Refresh Entry Exit with Clock Stop – Termination Disabled by Clock Stop Detection Circuit

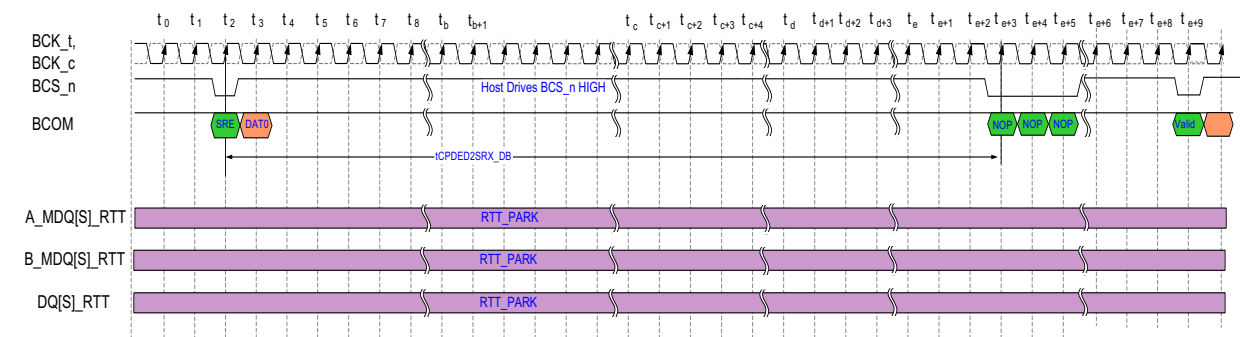
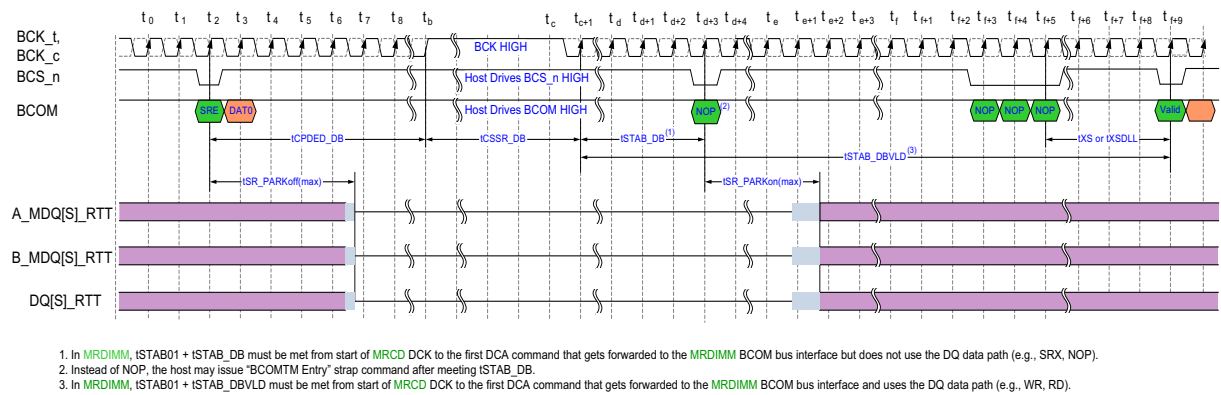
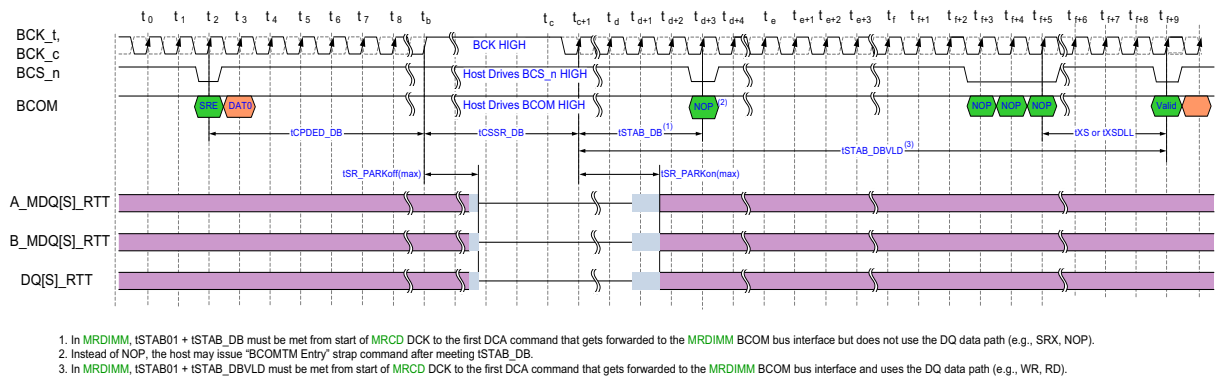


Figure 59 — Mux Mode Self Refresh Entry and Exit without Clock Stop – RTT\_PARK Remains Enabled

#### 4.1.4 Self Refresh Mode without Clock Stop Exit (cont'd)



**Figure 60 — Rank Mode Self Refresh Entry Exit with Clock Stop and Frequency Change – Termination Disabled by SRE Command**



**Figure 61 — Rank Mode Self Refresh Entry Exit with Clock Stop and Frequency Change – Termination Disabled by Clock Stop Detection Circuit**

1. In MRDIMM, ISTAB\_DBCMD must be met from start of MRCD DCK to the first DCA Command that gets forwarded to the MRDIMM BCOM bus interface but does not use the DQ data path (e.g., SRX, NOP, etc.).

2. Instead of NOP, the host may issue "BCOMTm Entry" strap command after meeting ISTAB\_DB.

3. In MRDIMM, ISTAB\_DBDATA must be met from start of MRCD DCK to the first DCA Command that gets forwarded to the MRDIMM BCOM bus interface and uses the DQ data path (e.g., WR, RD).

The diagram illustrates the timing relationships for the MRDIMM BCOM bus interface. The top section shows the BCK (clock), BCS (chip select), and BCOM (data/command) signals. The BCK signal is a periodic clock. The BCS signal is active-low, with BCS\_n going high at time t<sub>c</sub>. The BCOM signal is a multiplexed bus that carries data (green boxes) and commands (orange boxes). The data path is used for RDQ (read data) and the command path is used for MRCD (read command) and DCA (data command). The diagram shows the timing of the BCOM signal relative to the BCK and BCS signals, and the timing of the RDQ signal relative to the BCOM signal. The RDQ signal is shown as a series of purple bars, with the first bar starting at t<sub>0</sub> and the last bar starting at t<sub>H9</sub>. The RDQ signal is active-low, with the first bar going low at t<sub>0</sub> and the last bar going low at t<sub>H9</sub>. The diagram also shows the timing of the BCOM signal relative to the BCK and BCS signals, with the BCOM signal going high at t<sub>c</sub> and the BCOM signal going low at t<sub>H9</sub>. The diagram includes several timing annotations: t<sub>0</sub> to t<sub>8</sub> are marked on the BCK signal; t<sub>c</sub> is the time when BCS\_n goes high; t<sub>d</sub> to t<sub>H9</sub> are marked on the BCK signal; t<sub>0</sub> to t<sub>8</sub> are marked on the BCOM signal; t<sub>c</sub> is the time when BCS\_n goes high; t<sub>d</sub> to t<sub>H9</sub> are marked on the BCOM signal. The diagram also shows the timing of the RDQ signal relative to the BCOM signal, with the RDQ signal going low at t<sub>0</sub> and the RDQ signal going low at t<sub>H9</sub>. The diagram includes several timing annotations: t<sub>0</sub> to t<sub>8</sub> are marked on the BCK signal; t<sub>c</sub> is the time when BCS\_n goes high; t<sub>d</sub> to t<sub>H9</sub> are marked on the BCK signal; t<sub>0</sub> to t<sub>8</sub> are marked on the BCOM signal; t<sub>c</sub> is the time when BCS\_n goes high; t<sub>d</sub> to t<sub>H9</sub> are marked on the BCOM signal. The diagram also shows the timing of the RDQ signal relative to the BCOM signal, with the RDQ signal going low at t<sub>0</sub> and the RDQ signal going low at t<sub>H9</sub>. The diagram includes several timing annotations: t<sub>0</sub> to t<sub>8</sub> are marked on the BCK signal; t<sub>c</sub> is the time when BCS\_n goes high; t<sub>d</sub> to t<sub>H9</sub> are marked on the BCK signal; t<sub>0</sub> to t<sub>8</sub> are marked on the BCOM signal; t<sub>c</sub> is the time when BCS\_n goes high; t<sub>d</sub> to t<sub>H9</sub> are marked on the BCOM signal. The diagram also shows the timing of the RDQ signal relative to the BCOM signal, with the RDQ signal going low at t<sub>0</sub> and the RDQ signal going low at t<sub>H9</sub>.

1. In MRDIMM, IStAB\_DBCMD must be met from start of MRCD DCK to the first DCA Command that gets forwarded to the MRDIMM BCOM bus interface but does not use the DQ data path (e.g., SRX, NOP, etc.).

2. Instead of NOP, the host may issue "BCOMTm Entry" strap command after meeting IStAB\_DB.

3. In MRDIMM, IStAB\_DBDATA must be met from start of MRCD DCK to the first DCA Command that gets forwarded to the MRDIMM BCOM bus interface and uses the DQ data path (e.g., WR, RD).

The diagram illustrates the timing relationship between the BCS\_n and BCOM signals and the memory array read data signals. The clock signals BCK\_t and BCK\_c are shown as a series of pulses. BCS\_n is a control signal that transitions from low to high at time t<sub>b+1</sub>. BCOM is a data signal that transitions from low to high at time t<sub>c+1</sub>. The data signals A\_MDQ[S]\_RTT, B\_MDQ[S]\_RTT, and DQ[S]\_RTT are shown as a series of pulses. The timing parameters shown are ISR\_PARKoff(max), ICPOEDQSRX\_08, and ISR\_PARKon(max).

**Figure 64 — Rank Mode Self Refresh Entry and Exit without Clock Stop – Termination Disabled by SRE Command**

4.1.4 Self Refresh Mode without Clock Stop Exit (cont'd)

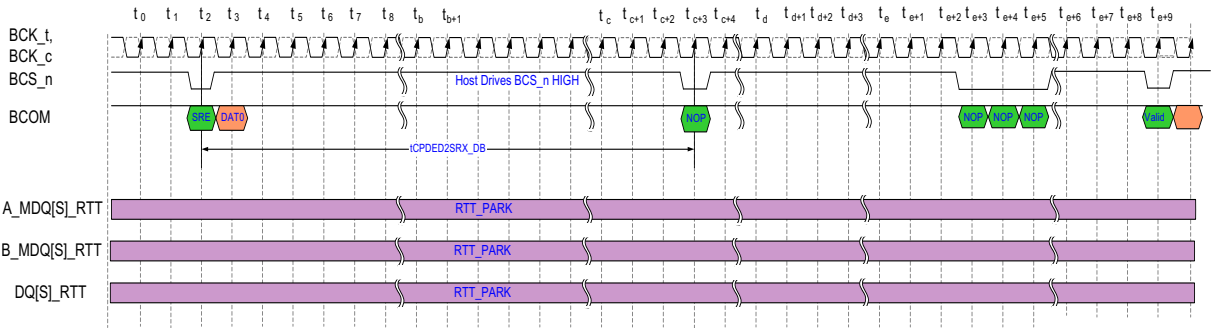


Figure 65 — Rank Mode Self Refresh Entry and Exit without Clock Stop – RTT\_PARK Remains Enabled

## 5 Data Buffer Control Bus

This section describes the Data Buffer Control Bus signals used in the DDR5 MRDIMM application. The Data Buffer interface connects the DDR5MRCD with each of the ten DDR5MDB Data Buffers.

The BCOM bus protocol is modified from the standard RCD/DB due to the two pseudo-channels in Mux mode. Read and write commands must specify which pseudo-channel(s) the command is for, and have a rank bit for each pseudo-channel.

The BCOM bus protocol also supports the Rank mode to access the four package ranks per sub-channel.

### 5.1 Control Bus Signals

Table 16 — List of Signals for Data Buffer Control Signals

Name	Description	Signal Count per channel
BCS_n	BCOM Chip Select	1
BCOM[2:0]	Data buffer command signals	3
BRST_n	BCOM Reset	1
BCK_t, BCK_c	Clock outputs for the data buffers	2
Total		7

#### 5.1.1 Control Bus Signal Termination

BCK\_t, BCK\_c, BCS\_n, and BCOM[2:0] signals are terminated to VDDQ on the DDR5 MRDIMM as shown in Figure 66.

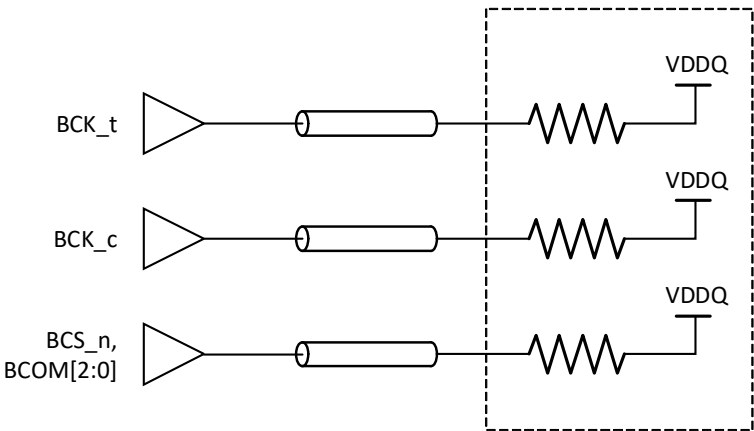


Figure 66 — Control Bus Termination



## 5.2 Restrictions

### 5.2.1 Restrictions in Mux Mode

Both pseudo-channels must be transferring data in the same direction as they are sharing strobe signals.

A minimum tCL of 28 is required for Mux 1N mode. A minimum tCL of 32 is required for Mux 2N mode.

### 5.2.2 Restrictions in Rank Mode

A minimum tCL of 24 is required for Rank 1N mode.

## 5.3 Control Bus Commands

When MDB is in Mux mode or Rank mode, Data Buffer control bus always works in 1N mode regardless of the DRAM Command/Address interface 1N/2N mode setting.

### 5.3.1 Data Buffer Control Bus Command Truth Table for both Mux and Rank Modes

Table 17 — Data Buffer Control Bus Command Truth Table<sup>1</sup>

Command	Description	BCS_n	1st Cycle BCOM[2:0] Encoding	2nd Cycle BCOM[2:0] Encoding	Total BCOM CMD Length (nBCK)
WR	Write	L	000 & 010	xxx	2
RD	Read	L	001 & 011	xxx	2
MRW	Mode Register Write	L	100	0xx	8
MRR	Mode Register Read	L	100	1xx	5
SRE	Self Refresh Entry	L	101	0xx	2
RFU	Reserved	L	101	1xx	-
MPC	Multi-purpose CMD	L	110	xxx	4
NOP	NOP	L	111	NA	1
DES	Deselect	H	xxx	NA	1

NOTE 1 However, when the MRCD detects Parity/CRC Error in the second cycle of a command, the second cycle BCSn will be pulled LOW by the MRCD to instruct the MDB to ignore the command.

### 5.3.2 Host Command to Command Timing due to the BCOM Bus Protocol

The BCOM bus puts certain restrictions on commands that would not normally be there. This is due to the number of clocks that some commands take to send across the BCOM bus.

**NOTE:** Each of the two sub channels have an independent BCOM bus. In Mux mode, the pseudo-channels share a sub channel BCOM bus, so the restrictions apply to the opposite pseudo-channel.

### 5.3.2 Host Command to Command Timing due to the BCOM Bus Protocol (cont'd)

**Table 18 — Host Command to Command Timing due to the BCOM Bus Protocol<sup>1</sup>**

Command	Total Length (nBCK)	DRAM Clocks (QCK) to Next Command Requiring BCOM Bus	Notes
WR	2	2	
RD	2	2	
MRW	8	8	
MRR	5	5	
SRE	2	2	In Mux mode, only PS0 SRE is sent to BCOM bus.
RFU	-	-	
MPC	4	4	
NOP	1	1	
DES	1	-	DES is the LACK of a command.

NOTE 1 This table does not supersede more restrictive requirements like tMRD and tCCD.

### 5.3.3 Command Sequences

Some commands require more than one clock cycle in order to send additional information needed by the Data Buffer in the execution of the command. This succession of command and its corresponding data transfers is called a command sequence.

#### 5.3.3.1 Command Sequences in Mux Mode

The WR and RD commands are sent individually per pseudo channel to allow enough payload bits to support 2 ranks per pseudo-channel and burst on the fly together. The two pseudo-channels may start their data transfers on the same clock or by any DRAM clock offset. Since two BCOM commands cannot be sent at the same time, a special format is used for the case where the pseudo-channels start their transfers 0, or 1 clocks apart. The second of the two BCOM commands will signal a transfer start offset of -1, or -2 DRAM clock cycles.

- If the two pseudo-channels start on the same clock, the PS0 BCOM command (Format 0) will be sent first, followed by the PS1 BCOM command (Format 1). The PS1 BCOM command will indicate that its transfer will start 2 DRAM clock cycles before the time where the BCOM command was sent.
- If the PS0 transfer starts one DRAM clock cycle after the PS1 transfer: The PS1 BCOM command (Format 0) will be sent first, followed by the PS0 BCOM command (Format 1). The PS0 BCOM command will indicate that its transfer will start 1 DRAM clock cycle before the time where the BCOM command was sent.
- If the pseudo-channels start 2 or more clock cycles apart the BCOM commands are sent independently and there is no need for an offset at all. These commands will be (Format 0).

There are not enough payload bits in the BCOM command to contain the Format, the WR/RD info, the pseudo-channel info, the rank info, the BL info and the clock offset info. Therefore, two formats are required.

- Format 0 is the standard format and contains the Format number, the WR/RD select, the pseudo-channel select, the rank select, and the burst length. The clock offset bit is NOT required in Format 0.

### 5.3.3.1 Command Sequences in Mux Mode (cont'd)

- Format 1 is used **ONLY** when the BCOM command must have a timing offset due to the pseudo-channels starting on the same clock or one starting one cycle after the other. It contains the Format number, the WR/RD select (which is actually redundant as it must be the same as the previous BCOM command), the rank select, the burst length, and a start offset bit. Note that the pseudo-channel select is **NOT** required, as it is always the opposite pseudo-channel from the previous Format 0 command.

### 5.3.3.2 Command Sequences in Rank Mode

In Rank mode, the command sequences are the same as Mux mode except the following:

- WR and RD commands in Format 0 are used with modified BCOM bits to support four ranks instead of pseudo-channel information. Format 1 is not used.
- MRW and MRR commands are used with modified BCOM bits to support four ranks instead of pseudo-channel information.

## 5.4 Command Sequence Descriptions

The timing diagrams in this section show only the lower nibble of the Data Buffer. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 16, preamble = 2 Cycle and postamble = 0.5 Cycle, but equivalent timing relationships exist for burst length = 8 and 18, other preamble settings, and postamble = 1.5 Cycle.

For readability reasons, the timing diagrams use the abbreviations DB\_RL and DB\_WL for the latency between second cycle of RD command and the first effective rising edge of MDQS at the Data Buffer inputs and for the latency between second cycle of WR command and the first effective rising edge of MDQS at the Data Buffer outputs respectively. Both DB\_RL and DB\_WL include full cycle and fractional cycle delays.

**Table 19 — Data Buffer PG[73:72, 1:0] Rank Training Control Word Decoding**

<b>MDB Control Word</b>	<b>Function</b>
<b>RWE0</b>	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word
<b>RWE1</b>	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word
<b>RWE2</b>	Lower Nibble DRAM Interface Receive Enable Training Control
<b>RWE3</b>	Upper Nibble DRAM Interface Receive Enable Training Control
<b>RWE8</b>	Lower Nibble DRAM Interface Write Leveling Control
<b>RWE9</b>	Upper Nibble DRAM Interface Write Leveling Control

The Data Buffer delays  $t_{PDM\_RD}$  and  $t_{PDM\_WR}$  are defined as the delay between first effective rising edge of MDQS and the first effective rising edge of DQS for a RD command and as the delay between first effective rising edge of DQS and the first effective rising edge of MDQS for a WR command respectively. By default these delays are constant per Data Buffer for all ranks and nibbles, however, the MDB may need to adjust  $t_{PDM}$  for non-default register settings in order to maintain the data path fall through time in the device.

Timing parameters that are integer multiples of tBCK are shown in **bold blue** letters while timing parameters that are analog non-integer multiples or fractions of tBCK are shown in *red italic* letters.

### 5.4.1 Equations for the Latencies in Mux Mode

xxx[PS,R].l and xxx[PS,R].u are the equations for the Lower and Upper nibbles, respectively. “PS” in the equations refers to the pseudo-channel number, and the “R” in the equations refers to the rank number.

$$BCOML = 1 \text{ nBCK}$$

$$DB\_WL(PS,R) = CWL + DWL(PS,R) - BCOML$$

$$DB\_RL(PS,R) = CL + MRE(PS,R) - BCOML$$

Fractional and cycle delay equations for DWL and MRE for PS0, PS1, Ranks 0 and 1 are listed below.

For the two ranks in pseudo-channel 0:

- $DWL[0,0].l = (PG[0]RWE1[3:0] * 64 + PG[0]RWE8[5:0]) * t_{BCK}/64.$
- $DWL[0,0].u = (PG[0]RWE1[7:4] * 64 + PG[0]RWE9[5:0]) * t_{BCK}/64.$
- $DWL[0,1].l = (PG[1]RWE1[3:0] * 64 + PG[1]RWE8[5:0]) * t_{BCK}/64.$
- $DWL[0,1].u = (PG[1]RWE1[7:4] * 64 + PG[1]RWE9[5:0]) * t_{BCK}/64.$
- $MRE[0,0].l = (PG[0]RWE0[3:0] * 64 + PG[0]RWE2[5:0]) * t_{BCK}/64.$
- $MRE[0,0].u = (PG[0]RWE0[7:4] * 64 + PG[0]RWE3[5:0]) * t_{BCK}/64.$
- $MRE[0,1].l = (PG[1]RWE0[3:0] * 64 + PG[1]RWE2[5:0]) * t_{BCK}/64.$
- $MRE[0,1].u = (PG[1]RWE0[7:4] * 64 + PG[1]RWE3[5:0]) * t_{BCK}/64.$

For the two ranks in pseudo-channel 1:

- $DWL[1,0].l = (PG[72]RWE1[3:0] * 64 + PG[72]RWE8[5:0]) * t_{BCK}/64.$
- $DWL[1,0].u = (PG[72]RWE1[7:4] * 64 + PG[72]RWE9[5:0]) * t_{BCK}/64.$
- $DWL[1,1].l = (PG[73]RWE1[3:0] * 64 + PG[73]RWE8[5:0]) * t_{BCK}/64.$
- $DWL[1,1].u = (PG[73]RWE1[7:4] * 64 + PG[73]RWE9[5:0]) * t_{BCK}/64.$
- $MRE[1,0].l = (PG[72]RWE0[3:0] * 64 + PG[72]RWE2[5:0]) * t_{BCK}/64.$
- $MRE[1,0].u = (PG[72]RWE0[7:4] * 64 + PG[72]RWE3[5:0]) * t_{BCK}/64.$
- $MRE[1,1].l = (PG[73]RWE0[3:0] * 64 + PG[73]RWE2[5:0]) * t_{BCK}/64.$
- $MRE[1,1].u = (PG[73]RWE0[7:4] * 64 + PG[73]RWE3[5:0]) * t_{BCK}/64.$

### 5.4.2 Equations for the Latencies in Rank Mode

xxx[R].l and xxx[R].u are the equations for the Lower and Upper nibbles, respectively. “R” in the equations refers to the rank number.

$$BCOML = 1 \text{ nBCK}$$

$$DB\_WL(R) = CWL + DWL(R) - BCOML$$

$$DB\_RL(R) = CL + MRE(R) - BCOML$$

Fractional and cycle delay equations for DWL for Ranks 0, 1, 2 and 3 are listed below.

- $DWL[0].l = (PG[0]RWE1[3:0] * 64 + PG[0]RWE8[5:0]) * t_{BCK}/64.$
- $DWL[0].u = (PG[0]RWE1[7:4] * 64 + PG[0]RWE9[5:0]) * t_{BCK}/64.$

### 5.4.2 Equations for the Latencies in Rank Mode (cont'd)

- $DWL[1].l = (PG[1]RWE1[3:0] * 64 + PG[1]RWE8[5:0]) * t_{BCK}/64.$
- $DWL[1].u = (PG[1]RWE1[7:4] * 64 + PG[1]RWE9[5:0]) * t_{BCK}/64.$
- $DWL[2].l = (PG[72]RWE1[3:0] * 64 + PG[72]RWE8[5:0]) * t_{BCK}/64.$
- $DWL[2].u = (PG[72]RWE1[7:4] * 64 + PG[72]RWE9[5:0]) * t_{BCK}/64.$
- $DWL[3].l = (PG[73]RWE1[3:0] * 64 + PG[73]RWE8[5:0]) * t_{BCK}/64.$
- $DWL[3].u = (PG[73]RWE1[7:4] * 64 + PG[73]RWE9[5:0]) * t_{BCK}/64.$

Fractional and cycle delay equations for MRE for Ranks 0, 1, 2 and 3 are listed below.

- $MRE[0].l = (PG[0]RWE0[3:0] * 64 + PG[0]RWE2[5:0]) * t_{BCK}/64.$
- $MRE[0].u = (PG[0]RWE0[7:4] * 64 + PG[0]RWE3[5:0]) * t_{BCK}/64.$
- $MRE[1].l = (PG[1]RWE0[3:0] * 64 + PG[1]RWE2[5:0]) * t_{BCK}/64.$
- $MRE[1].u = (PG[1]RWE0[7:4] * 64 + PG[1]RWE3[5:0]) * t_{BCK}/64.$
- $MRE[2].l = (PG[72]RWE0[3:0] * 64 + PG[72]RWE2[5:0]) * t_{BCK}/64.$
- $MRE[2].u = (PG[72]RWE0[7:4] * 64 + PG[72]RWE3[5:0]) * t_{BCK}/64.$
- $MRE[3].l = (PG[73]RWE0[3:0] * 64 + PG[73]RWE2[5:0]) * t_{BCK}/64.$
- $MRE[3].u = (PG[73]RWE0[7:4] * 64 + PG[73]RWE3[5:0]) * t_{BCK}/64.$

### 5.4.3 WR/RD Burst Length Processing

Table 20 — WR/RD Burst Length Processing

DRAM MR0 Snooped BL Type PG8RWE0[1:0] <sup>1</sup>	DRAM MR50 Snooped WR/RD CRC Enabled PG8RWE8[2:0]	WR/RD Sequence DAT0 BCOM[1]	MDB Burst Length Processing (BL)
00 = BL16 Fixed	Disabled	X	16
	Enabled	X	18
01 = BC8 OTF	Disabled	0 = BC8	8
		1 = BL16	16
	Enabled	X	18

NOTE 1 BL32 Fixed and BL32 OTF settings are not supported in MRCD and MDB in normal operation.

## 5.4.4 WR Commands

### 5.4.4.1 WR Command (Format 0) in Mux Mode

**Table 21 — Command (Format 0) in Mux Mode**

Clock	BCS_n	BCOM[2:0]	Description
1	0	000	WR command Format 0 BCOM[0]=0 Indicated WR command (vs. RD). BCOM[1]=0 Indicates Format 0 BCOM[2]=0 (RD/WR vs. other commands)
2	1	DAT0	BCOM[0]= Rank Select; 0=Rank 0, 1=Rank 1 BCOM[1]= BL; 0 = BC8, 1=BL16 BCOM[2]= Pseudo-Channel Select; 0=PS0, 1=PS1

### 5.4.4.2 WR Command (Format 0) in Rank Mode

**Table 22 — Command (Format 0) in Rank Mode**

Clock	BCS_n	BCOM[2:0]	Description
1	0	000	WR command Format 0 BCOM[0]=0 Indicated WR command (vs. RD). BCOM[1]=0 Indicates Format 0 BCOM[2]=0 (RD/WR vs. other commands)
2	1	DAT0	BCOM[0]= Rank Select <sup>1</sup> BCOM[1]= BL; 0 = BC8, 1=BL16 BCOM[2]= Rank Select <sup>1</sup>

NOTE 1 BCOM[2,0] = Rank Select; 00 = Rank 0, 01 = Rank 1, 10 = Rank 2, 11 =Rank 3

### 5.4.4.3 WR Command (Format 1) in Mux Mode

**Table 23 — WR Command (Format 1) in Mux Mode**

Clock	BCS_n	BCOM[2:0]	Description
1	0	010	WR command Format 1 BCOM[0]= 0 Indicated WR command (vs. RD). BCOM[1]= 1 Indicates Format 1 BCOM[2]= 0 (RD/WR vs. other commands)
2	1	DAT0	BCOM[0]= Rank Select; 0=Rank 0, 1=Rank 1 BCOM[1]= BL; 0 = BC8, 1=BL16 BCOM[2]= Delay Bit: 0= -2 clock delay; 1 = -1 clock delay

### 5.4.4.3 WR Command (Format 1) in Mux Mode (cont'd)

Delay Bit BCOM[2] encoding in DAT0 is as follows:

- 1 = -1 clock delay. Data will come one cycle earlier than the command timing.
- 0 = -2 clock delay. Data will come two cycles earlier than the command timing (at the same time as the other pseudo-channel).

### 5.4.4.4 WR Command Sequence Timing

Figure 67 shows the timing sequence for a Write command in Mux mode. The second WR command in format 1 for PS1 has an offset of -2 clock cycles.

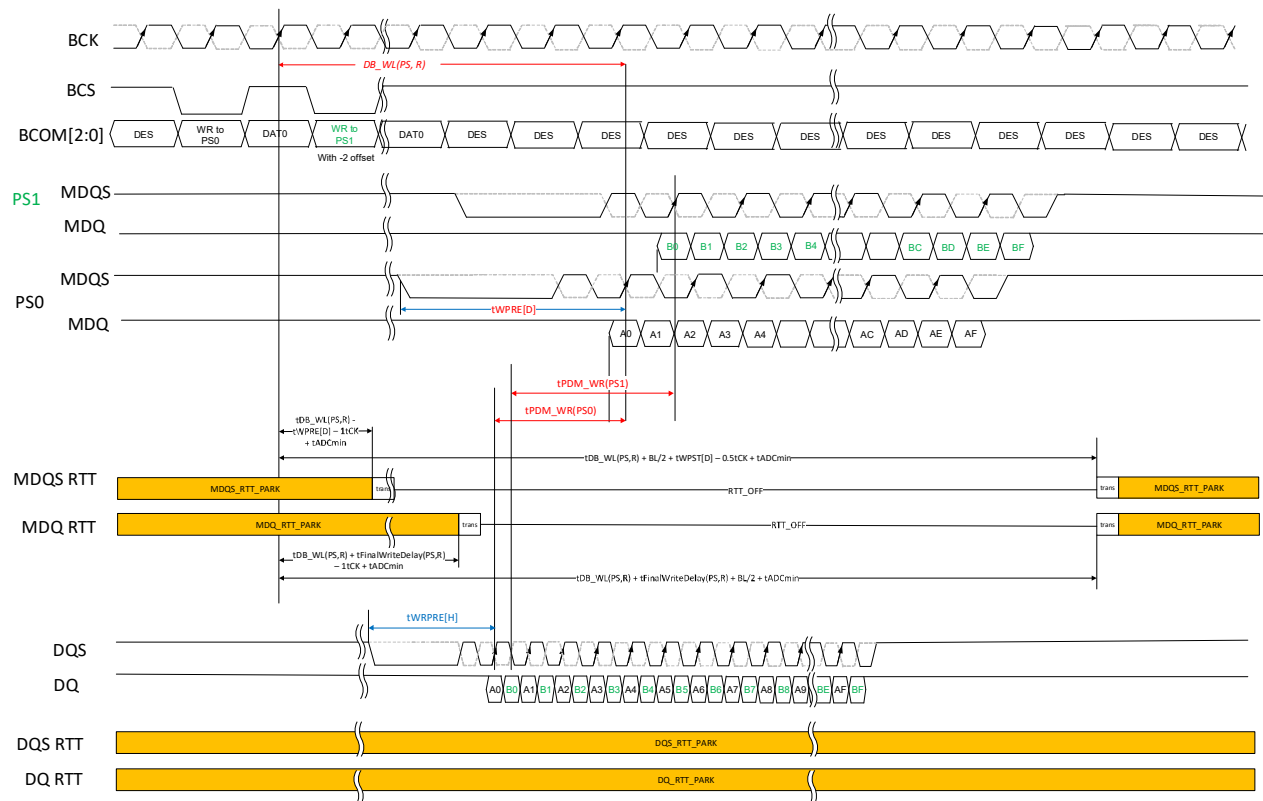


Figure 67 — Write Command Sequence in Mux Mode

#### 5.4.4.4 WR Command Sequence Timing (cont'd)

Figure 68 shows the timing sequence for a Write command in Rank mode.

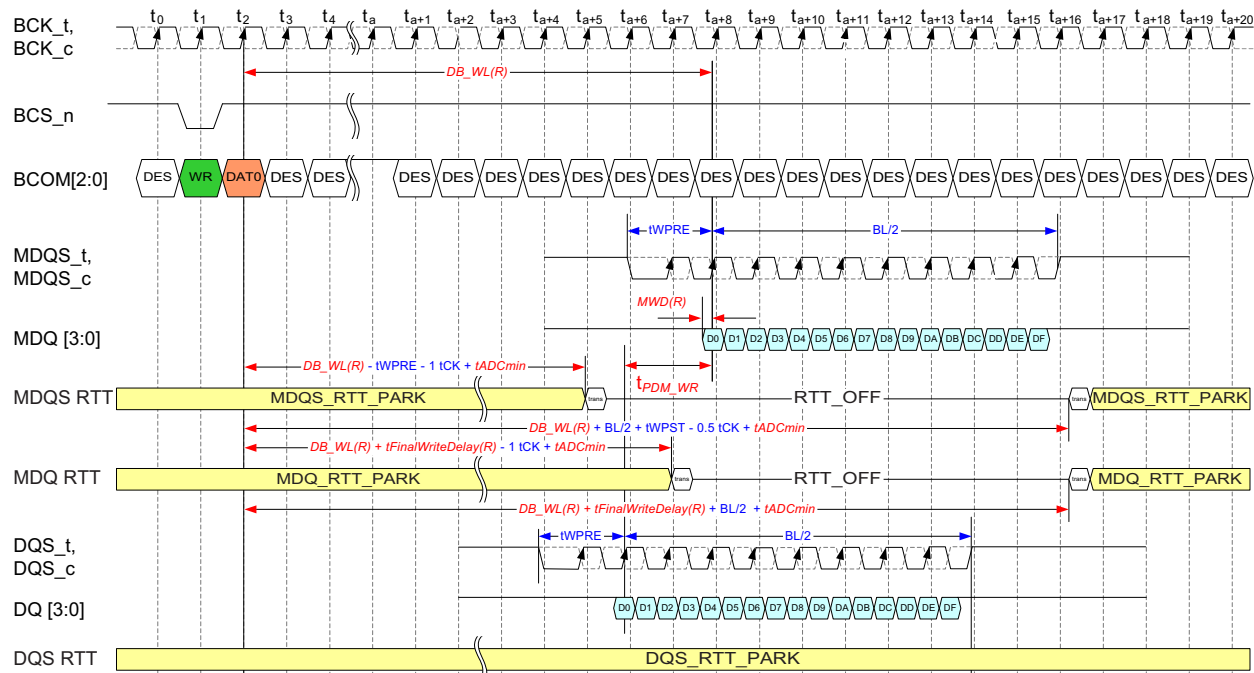


Figure 68 — Write Command Sequence in Rank Mode

### 5.4.5 RD Commands

#### 5.4.5.1 RD Command Format 0 in Mux Mode

Table 24 — RD Command (Format 0) in Mux Mode

Clock	BCS_n	BCOM[2:0]	Description
1	0	001	RD command Format 0 BCOM[0]=1 Indicated RD command (vs. WR). BCOM[1]=0 Indicates Format 0 BCOM[2]=0 (RD/WR vs. other commands)
2	1	DAT0	BCOM[0]= Rank Select; 0=Rank 0, 1=Rank 1 BCOM[1]= BL; 0 = BC8, 1=BL16 BCOM[2]= Pseudo-Channel Select; 0=PS0, 1=PS1



### 5.4.5.2 RD Command Format 0 in Rank Mode

**Table 25 — RD Command (Format 0) in Rank Mode**

Clock	BCS_n	BCOM[2:0]	Description
1	0	001	RD command Format 0 BCOM[0]=1 Indicated RD command (vs. WR). BCOM[1]=0 Indicates Format 0 BCOM[2]=0 (RD/WR vs. other commands)
2	1	DAT0	BCOM[0]= Rank Select <sup>1</sup> BCOM[1]= BL; 0 = BC8, 1=BL16 BCOM[2]= Rank Select <sup>1</sup>

NOTE 1 BCOM[2,0] = Rank Select; 00 = Rank 0, 01 = Rank 1, 10 = Rank 2, 11 =Rank 3

### 5.4.5.3 RD Command Format 1 in Mux Mode

**Table 26 — RD Command (Format 1) in Mux Mode**

Clock	BCS_n	BCOM[2:0]	Description
1	0	011	RD command Format 1 BCOM[0]= 1 Indicates RD command (vs. WR). BCOM[1]= 1 Indicates Format 1 BCOM[2]= 0 (RD/WR vs. other commands)
2	1	DAT0	BCOM[0]= Rank Select; 0=Rank 0, 1=Rank 1 BCOM[1]= BL; 0 = BC8, 1=BL16 BCOM[2]= Delay Bit: 0= -2 clock delay; 1 = -1 clock delay

Delay Bit BCOM[2] encoding in DAT0 is as follows:

1 = -1 clock cycle delay. Data will come one cycle earlier than the command timing.

0 = -2 clock cycles delay. Data will come two cycles earlier than the command timing (at the same time as the other pseudo-channel).

5.4.5.4 RD Command Sequence Timing

Figure 69 shows the timing sequence for a Read command in Mux mode. The second RD command in format 1 for PS1 has an offset of -2 clock cycles. This figure only shows the case of the unmatched receivers at the DRAM interface.

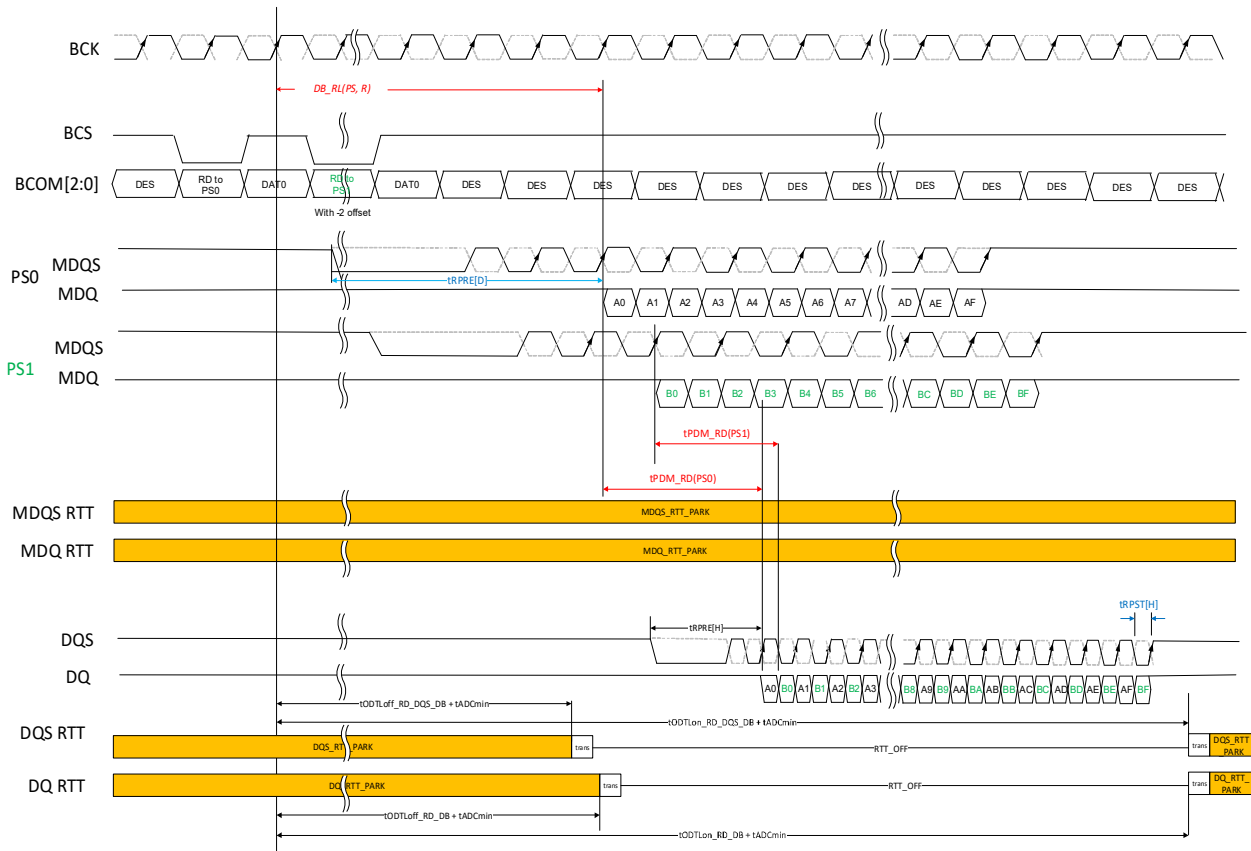


Figure 69 — Read Command Sequence in Mux Mode

#### 5.4.5.4 RD Command Sequence Timing (cont'd)

Figure 70 shows the timing sequence for a Read command in Rank mode.

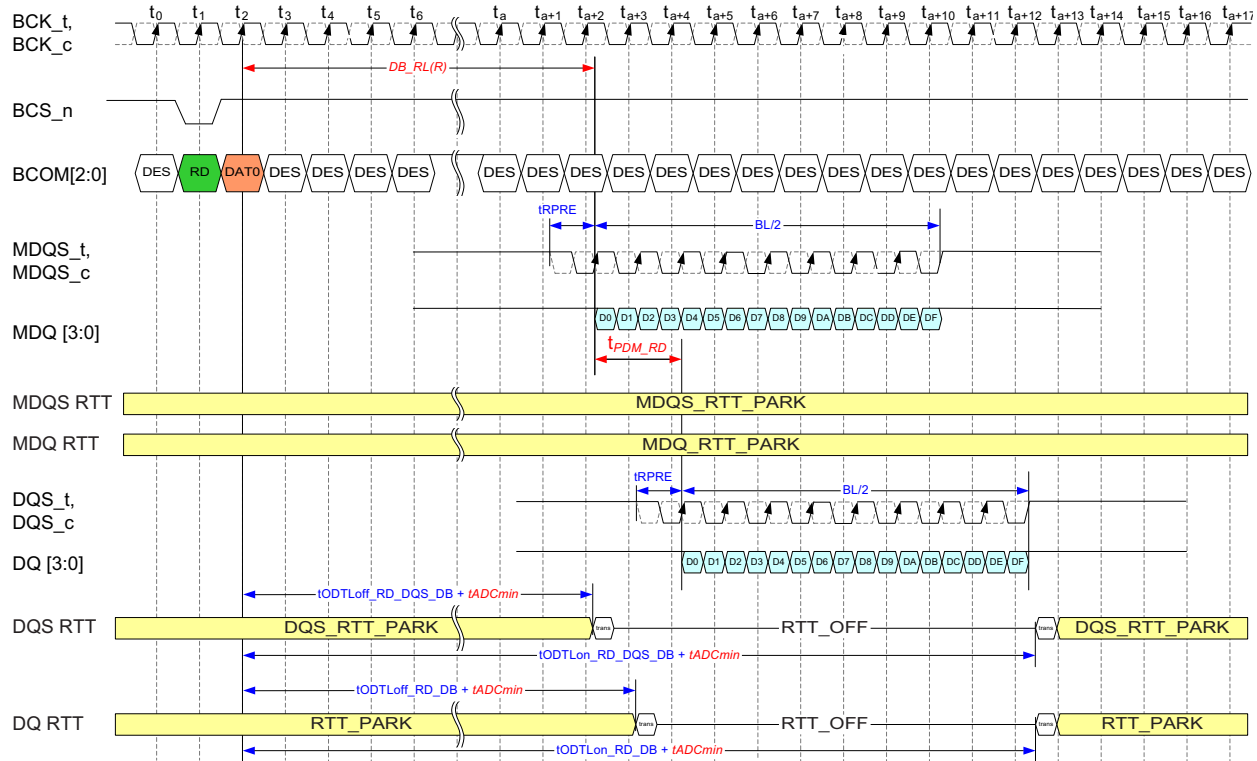


Figure 70 — Read Command Sequence in Rank Mode

### 5.4.6 MRW Commands

The MRCD generates MRW commands to the data buffers for each MR command. Table 27 shows the sequence for MRW commands.

**Table 27 — Multi-cycle Sequence for MRW Commands**

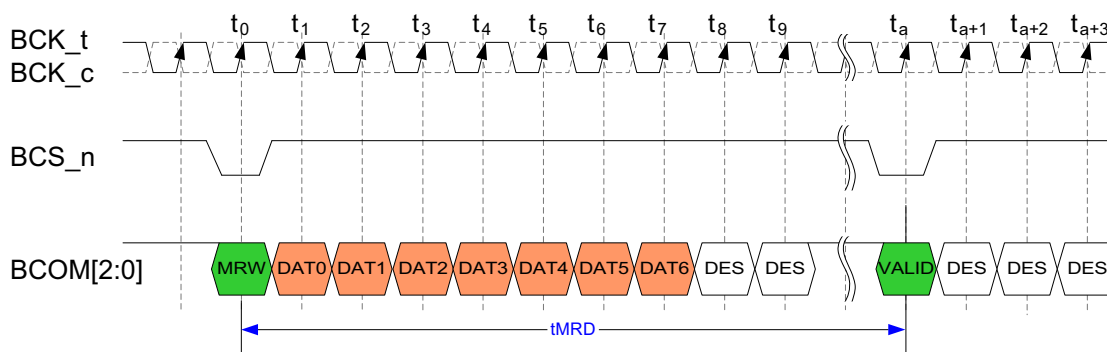
Time (Clock Cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	100	MRW Command BCOM[2:0] = 100
2	1	CMD/DAT0 0xx	BCOM[0] = CW; 0 = DRAM space, 1 = DB space BCOM[1] = Rank Select; 0 = Rank0; 1 = Rank1 <sup>1</sup> BCOM[2] = 0 (part of command encoding)
3	1	DAT1	BCOM[1:0] = MRA[7:6] BCOM[2] = RFU in Mux mode, Rank select in Rank mode. <sup>1</sup>
4	1	DAT2	BCOM[2:0] = MRA[5:3]
5	1	DAT3	BCOM[2:0] = MRA[2:0]
6	1	DAT4	BCOM[1:0] = OP[7:6] BCOM[2] = RFU
7	1	DAT5	BCOM[2:0] = OP[5:3]
8	1	DAT6	BCOM[2:0] = OP[2:0]
9		Next Cmd	Next Command

NOTE 1 In Rank mode, {DAT1[2], DAT0[1]} = Rank Select; 00 = Rank 0, 01 = Rank 1, 10 = Rank 2, 11 = Rank 3.

The sequence for an MRW command is shown in Figure 71. The timing diagrams show how the MR Write command is followed by seven data transfer cycles. Since the command sequence uses eight cycles it is necessary to include these cycles as part of the tMRD parameter that indicates the spacing from the MRW command to the following valid command (also shown in the diagrams). The number of additional transfers on the BCOM bus after the MRW command also imposes a limitation on how close consecutive MRW commands can be issued to the Data Buffer.

The Rank Select bit may be ignored by the data buffer in both the Mux mode and the Rank mode.

In Mux mode, there is no pseudo-channel information in the MRW command. Page 70 RW E4 bits 3 and 4 determine whether pseudo-channel 0 or 1 is the target for the MRW command as far as MRW snooping is concerned.



**Figure 71 — MRW Command Sequence**

## 5.4.7 MRR Commands

### 5.4.7.1 Multi-cycle Sequence for MRR Commands

Table 28 shows the sequence for MRR commands.

**Table 28 — Multi-cycle Sequence for MRR Commands**

Time (Clock Cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	100	Mode Register Read Command (MRR) BCOM[2:0] = 100
2	1	CMD/DAT0 1xx	BCOM[0] = CW; 0 = DRAM space, 1 = DB space BCOM[1] = Rank Select; 0 = Rank 0, 1 = Rank 1. <sup>1</sup> BCOM[2] = 1 (part of command encoding) Note: Burst length is fixed BL16
3	1	DAT1	BCOM[1:0] = MRA[7:6] BCOM[2] = PS select in Mux mode; 0=PS0, 1=PS1. Rank select in Rank mode. <sup>1</sup>
4	1	DAT2	BCOM[2:0] = MRA[5:3]
5	1	DAT3	BCOM[2:0] = MRA[2:0]
6		Next Cmd	Next Command

NOTE 1 In Rank mode, {DAT1[2], DAT0[1]} = Rank Select; 00 = Rank 0, 01 = Rank 1, 10 = Rank 2, 11 = Rank 3.

MRR commands read data from the MR locations in either the DRAM or the data buffer. MR locations in the MRCD must be read by first transferring their contents to a DRAM register then reading that DRAM register. If the CW bit is a 0 the read will come from the DRAMs, and the data buffer will treat this command like a read command. The case CW = 1 MRA7 = 0 is not defined. Data Buffer will treat it as invalid address and Read zeros. If the CW = 1 and MRA7 = 1, then read will come from the Data Buffer's MR location. The Data Buffer will send the same data on all DQs for the second 8 UI and drive High or Low on the first 8 UI.

**Table 29 — MRR Read Format for Data Buffer Return<sup>1,2</sup>**

Serial	UI 0-7	UI 8	UI 9	UI 10	UI 11	UI 12	UI 13	UI 14	UI 15
DQ0	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ1	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ2	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ3	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ4	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ5	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7
DQ6	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7
DQ7	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7

NOTE 1 When DQ Bus CRC mode is enabled, the DQS1 as CRC lane will be "don't care" for the Host.

NOTE 2 The UIs in the table are per pseudo-channel in Mux mode, and interleaved at Host interface based on PS value in MRR command.

### 5.4.7.1 Multi-cycle Sequence for MRR Commands (cont'd)

**Table 30 — MRR Read Format for Data Buffer Return with DRAM Read CRC Enabled<sup>1</sup>**

Serial	UI 0-7	UI 8	UI 9	UI 10	UI 11	UI 12	UI 13	UI 14	UI 15	UI 16	UI 17
<b>DQ0</b>	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
<b>DQ1</b>	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x
<b>DQ2</b>	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
<b>DQ3</b>	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x
<b>DQ4</b>	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
<b>DQ5</b>	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x
<b>DQ6</b>	0	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	x	x
<b>DQ7</b>	1	!OP0	!OP1	!OP2	!OP3	!OP4	!OP5	!OP6	!OP7	x	x

NOTE 1 This table is for Rank mode only, since DRAM CRC is not supported in Mux mode.

## 5.4.8 SRE Commands

The SRE command is sent by the MRCD when the sub-channel enters SRE.

**Table 31 — Multi-cycle Sequence for SRE Commands**

Time (Clock Cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	101	Self Refresh Entry Command (SRE) <sup>1</sup> BCOM[2:0] = 101
2	1	CMD/DAT0 0xx	BCOM [0] = Reserved BCOM [1] = Reserved BCOM [2] = 0 (part of encoding)
3		Next Cmd	Next Command

NOTE 1 Since the SRE command is a 1-Cycle command on the DRAM bus and a 2-Cycle command on the BCOM bus, the Host controller must ensure there is enough spacing between the SRE command and the following command that uses the BCOM bus.

### 5.4.9 MPC Command

Table 32 shows the sequence for MPC commands.

**Table 32 — Multi-cycle Sequence for MPC Commands**

Time (Clock Cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	110	Multi-purpose Command (MPC) BCOM[2:0] = 110
2	1	DAT0	BCOM[1:0] = OP[7:6] BCOM[2]= RFU
3	1	DAT1	BCOM[2:0] = OP[5:3]
4	1	DAT2	BCOM[2:0] = OP[2:0]
5		Next Cmd	Next Command

### 5.4.10 NOP

Table 33 shows the sequence for NOP.

**Table 33 — Multi-cycle Sequence for NOP Commands**

Time (Clock Cycle)	BCS_n	BCOM[2:0]	Description
0		Prev Cmd	Previous command or data transfer
1	0	111	NOP Command BCOM[2:0] = 111
2		Next Cmd	Next Command

When in power down, an active BCS\_n signal will return the Data Buffer to the active state. The BCOM command will indicate NOP so that no other command is executed.

## 6 BCOM Training Mode (BCOMTM) - Data Buffer Interface

BCOMTM is a method to facilitate the feedback of a logical combination of the sampled BCOM[2:0] and BCS\_n signals. In this mode, the BCK is running and the BCK samples the BCOM and BCS\_n signals every rising edge of BCK. A feedback equation that includes all the BCOM and BCS\_n signals results in an output value that is sent on the DQ signal back to the Host memory controller. The MRCD timings for BCS\_n and BCOM[2:0] signals can then be optimized for proper alignment to the BCK signal. When the Data Buffer is in this mode, no functional commands are executed. The functional command interface is restored only after exiting BCOMTM. The Data Buffer can exit BCOM TM in three ways, which requires a reset with BCOM[2:0] straps all HIGH, with straps all LOW, or with straps set for the BCOM TM exit (010), see Table 34.

### 6.1 Entry and Exit for BCOM Training Mode

BCOMTM is enabled by a static value of BCOM[2] = LOW, BCOM[1] = LOW, and BCOM[0] = HIGH on the BCOM signals when BRST\_n de-asserts. The Data Buffer captures encoding on BCOM signal pins.

BCOMTM Exit by a static value of BCOM[2] = LOW, BCOM[1] = HIGH, and BCOM[0] = LOW on the BCOM signals when BRST\_n de-asserts. The Data Buffer captures encoding on BCOM signal pins.

### 6.2 Data Buffer Training States

When the Data Buffer powers up, the command bus may need to be trained prior to normal operation. In order to set BCOM VREF and enable BCOM Training Mode, the following training states will be supported by the DDR5MDB02: BCOMTM, set 1N BCOM CMD Timing, and set BCOM VREF as shown in Table 34.

**Table 34 — BCOM Strap for Data Buffer Training States**

BCS_n Static Value <sup>1</sup>	BCOM[2:0] Static Value	Description	tStrap_Delay <sup>2</sup>
H	000	Normal operation - RESET <sup>3</sup>	tSTAB_DB (Max)
H	001	BCOMTM ENTRY <sup>4</sup>	tBCOMTM_Entry (Max)
H	010	BCOMTM EXIT <sup>5</sup>	tBCOMTM_Exit (Max)
H	011	Set 1N BCOM CMD Timing <sup>6</sup>	tBCOM_1N (Max)
H	100	Set BCOM BVref to 75% VDD <sup>7,8</sup>	tBCOM_Vref (Max)
H	101	Increase voltage of BCOM BVref by 1% <sup>7,8</sup>	Vref_time_short (Max)
H	110	Decrease voltage of BCOM BVref by 1% <sup>7,8</sup>	Vref_time_short (Max)
H	111	Normal operation - RESET <sup>3</sup>	tSTAB_DB (Max)

NOTE 1 The Host is required to drive BCS\_n HIGH and the MDB ignores BCS\_n when decoding Strap command.

NOTE 2 Minimum waiting times the Host must guarantee from Strap command being captured to the next valid command, shown in Figure 72.

NOTE 3 Normal Reset - default reset - all non-sticky control registers are restored to their default states (which is “0”, except when explicitly defined otherwise).

NOTE 4 BRST\_n sequence only sets BCOMTM enable within buffer. Retain any previous control word values, internal register and any previous Vref values

NOTE 5 BRST\_n sequence only clears BCOMTM enable within buffer. Retain any previous control word values, internal register and any previous Vref values

NOTE 6 BRST\_n sequence only sets BCOM CMD timing. Retain any previous control word values. When Host applies “Set 1N BCOM CMD Timing,” RW80[0] and RW80[7] will be updated to 1N mode.

NOTE 7 BRST\_n sequence only sets BCOM BVref within buffer. Retain any previous control word values.

NOTE 8 The Data Buffer will update the BVref control word PG[2]RWFA setting so that it reflects the voltage value resulting from executing this Strap command.



## 6.2 Data Buffer Training States (cont'd)

When BRST\_n de-asserts, the Data Buffer captures encoding on BCOM signal pins.

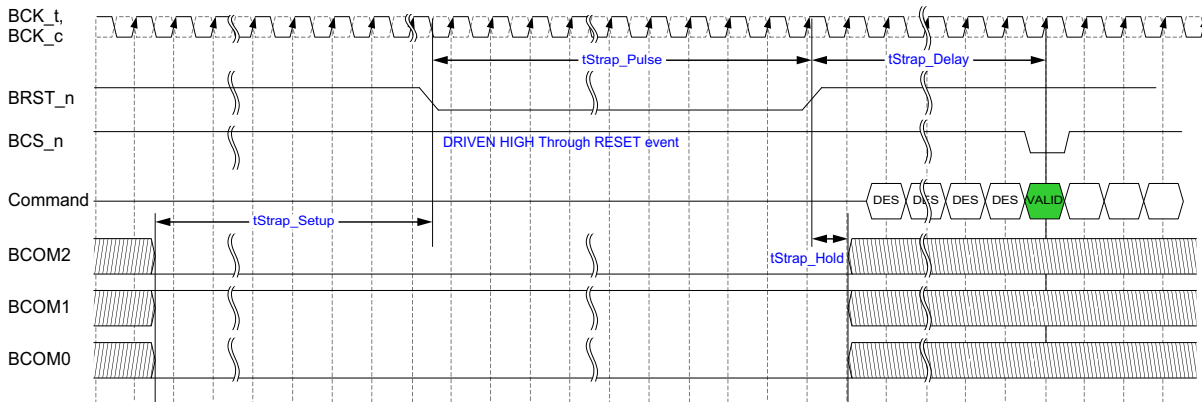


Figure 72 — Strap Example

## 6.3 BCOM Training Mode (BCOMTM) Operation

In BCOMTM, the BCOM values are sampled on every rising BCK edge. In BCOMTM the BCS\_n signal is also sampled on every rising BCK edge as an input signal and does not qualify the BCOM signals. Once the BCOM and BCS\_n signals are sampled, the values are XOR'd to produce an XOR Sample. This XOR Sample is logically combined with other XOR Samples in the sequence to produce an output value that is driven on all the DQs, as a static value.

During BCOM Training Mode, the module-level BCOM termination is enabled as for functional operation. The BCOM VREF is set according to the value programmed through the BRST\_n static BCOM settings. The timing requirements for the BCOM bus, BCK\_t, BCK\_c, and BCS\_n are the same as for functional operation.

The delay from when the BCOM and BCS\_n signals are sampled and when the output of the logical combination of XOR Samples is driven on the DQ signals is specified as  $t_{BCOMTM\_Valid}$ , as shown in the following figure. The XOR Samples should alternate between a 0 and 1 in order to produce a training pattern with consistent feedback to the Host. When there is no change on the BCOM training output, the DQ shall continue to drive the same value continuously with no switching on the bus. The pattern is generated by the Host and leverages the BCOM Pass Through mode in the MRCD. The BCOM training pattern will assert BCS\_n LOW one or more times for each BCOM/BCS\_n or BCK output delay setting change.

On the Host interface, while in BCOM training mode, the MDB continuously enables its DQ drivers, and disables its DQ receivers and DQ termination (DQ\_RTT\_PARK). Also, the Data Buffer disables its DQS drivers and receivers. It applies DQS\_RTT\_PARK continuously on DQS if enabled.

As shown in Figure 73, the Data Buffer device is required to disable the DQ outputs within  $t_{BCOMTM\_Exit}$  after executing a BCOMTM Exit strap command. Since there is no minimum value defined for  $t_{BCOMTM\_Exit}$ , the DQ outputs can be disabled any time between the BCOMTM\_Exit command and  $t_{BCOMTM\_Exit}$  (Max).

### 6.3 BCOM Training Mode (BCOMTM) Operation (cont'd)

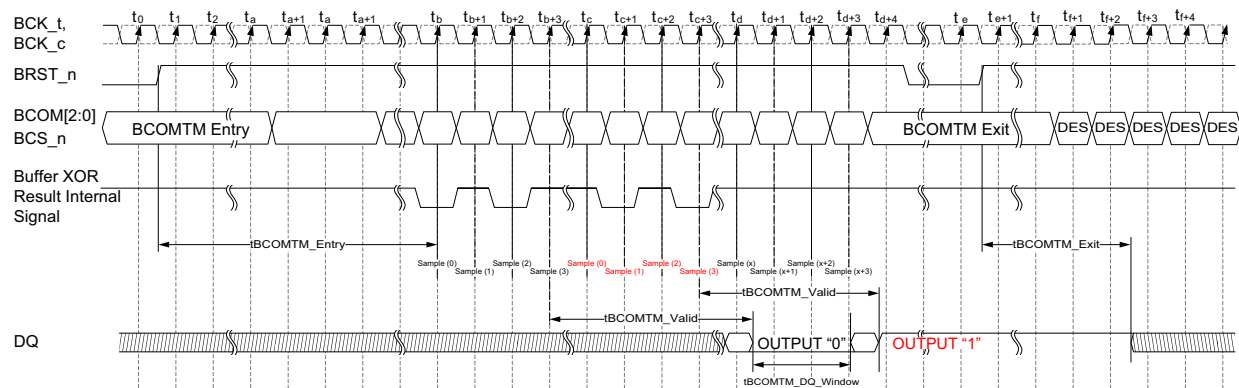


Figure 73 — Timing Diagram for BCOMTM

### 6.4 BCOM Training Feedback Equations

The BCOMTM Output is computed based on the BCS\_n assertion and the values of the BCOM inputs. Table 35 clarifies the output computation.

Table 35 — XOR Sample

BCK	BCOMTM XOR Sample
Rising Edge	XOR (BCOM[2:0], BCS_n)
Falling Edge	No Sample

In BCOMTM, the BCOM and BCS\_n values are sampled on all BCK rising edges and XOR'd. Each group of 4 consecutive XOR samples is evaluated in pairs, and then the two pairs are combined with a logical OR prior to sending to the DQ output. The evaluation of the XOR samples to determine the output is as follows:

Table 36 — Sample Evaluation for Intermediate Output[0]

Output[0]	XOR Sample[0]	XOR Sample[1]
1	0	0
0	0	1
1	1	0
1	1	1

Table 37 — Sample Evaluation for Intermediate Output[1]

Output[1]	XOR Sample[2]	XOR Sample[3]
1	0	0
0	0	1
1	1	0
1	1	1

Table 38 — Sample Evaluation for Final BCOMTM Output

BCOMTM Output <sup>1</sup>	Output[0]	Output[1]
0	0	0
1	0	1
1	1	0
1	1	1

NOTE 1 When there is no change on the BCOMTM Output from previous evaluation, DQ shall continue to drive same value continuously with no switching on the bus.

## 7 Per X Addressability Modes

### 7.1 Per DRAM Addressability (PDA) Mode

The DDR5MDB02 will need to support DQ pass through mode, details in Section 3.7.

In the Mux mode and Rank mode, PDA enumeration for the DRAMs uses DQ Pass-Through mode in the Data Buffers with the data and strobes passed from the Host to the DRAM side.

In the Mux mode, the Host interface strobes are running at 2x the speed that is expected by the DRAMs. To accommodate this, the Data Buffer has a circuit to optionally divide the strobe by two before sending to the DRAM side. Control Word [PG\[70\]RWE4\[6\]](#) is used to control this function, with a 0 bypassing the circuit and passing the strobe through unmodified, and a 1 dividing it by 2.

The circuit adds propagation delay for DQ pass through mode:

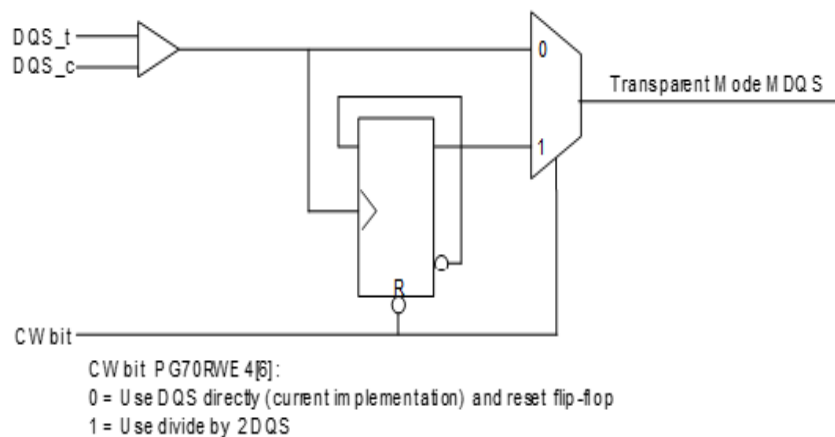


Figure 74 — DQ Pass-Through Mode Divider

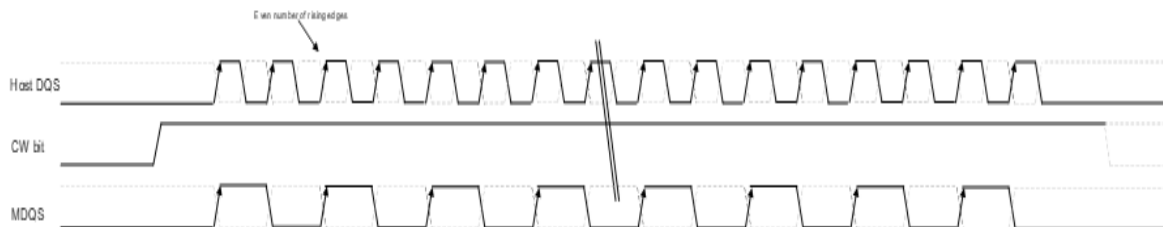


Figure 75 — PDA Enumeration Timing Example

For repeatable MDQS pattern, pass-through data flow must be configured for the Host-to-DRAM direction and a valid differential level must be applied on Host DQS before the [PG70RWE4\[6\]](#) is written from 0 to 1 and for the entire PDA enumeration event the bit is set. Also, an even number of DQS pulses, including the preamble and postamble, must be sent for each burst. This bit must be a 0 when in Transparent Mode.

## 7.2 Per Buffer Addressability (PBA) Mode

It is necessary for the data buffer to support a feature similar to per-DRAM addressability for buffer control word access transactions. This feature will be used to allow the Host controller to configure each data buffer independently from each other. This is a requirement, for example, to allow independent DFE register settings per buffer. DRAM PDA mode and MDB PBA mode shall not be enabled at the same time.

DRAM CRC and DQ Bus CRC must be disabled in the MDB when PBA enumeration is run. For PBA enumeration in Rank mode, a BL16 strobe set will be sent by the Host. For PBA enumeration in Mux mode, a BL32 strobe set will be sent by the Host. The Data Buffers will use any one of the strobe edges or set of edges — for example, the last 4 strobe edges — to sample the data bus.

DDR5 introduces a BCOM interface-only method for Per Buffer Addressability, by having a unique PBA Enumerate ID in each Data Buffer and the ability to set a PBA Select ID in all Data Buffers.

The unique PBA Enumerate ID requires the use of the DQ signals and a PBA Enumerate Programming Mode in the Data Buffer to program.

Once the PBA Enumerate ID has been programmed, subsequent commands do not use the DQ signals (Legacy PBA mode) to designate which Data Buffer is selected for the command. The PBA Enumerate ID is a 4-bit field which is different in each Data Buffer. The PBA Select ID is also a 4-bit field which is set dynamically via MRW commands and it set to the same value in all Data Buffers.

When the PBA Select ID is the same as the PBA Enumerate ID or when the PBA Select ID is set to the “All Buffers” code of 1111B, the Buffer will apply the MRW command.

During RESET procedure, the receive FIFO must be initialized with all ones in order to ensure that the PBA enumerate flow does not program an enumerate ID when the strobes are not officially toggling. This is specifically for the case where the DIMM is connected in a test environment where the strobes of some devices are not connected. Those buffers will retain the default ID of 15.

## 7.3 PBA Enumerated ID Programming

PBA Enumerate Programming Mode is enabled by setting the PBA Enumerate Mode bit to a 1. While in this mode only MRWs to the PBA Enumerate ID Control Word or the PBA Enumerate Enable Control word (to disable the mode) are permitted. There are two sequences that may be used to perform PBA Enumerated ID Programming. Sequence A involves providing a single burst of 16 strobe edges in Rank mode or 32 strobe edges in Mux mode sent in association with the PBA Enumerate ID MRW command. Sequence B involves a continuous toggling of the DQS<sub>t</sub> and DQS<sub>c</sub>.

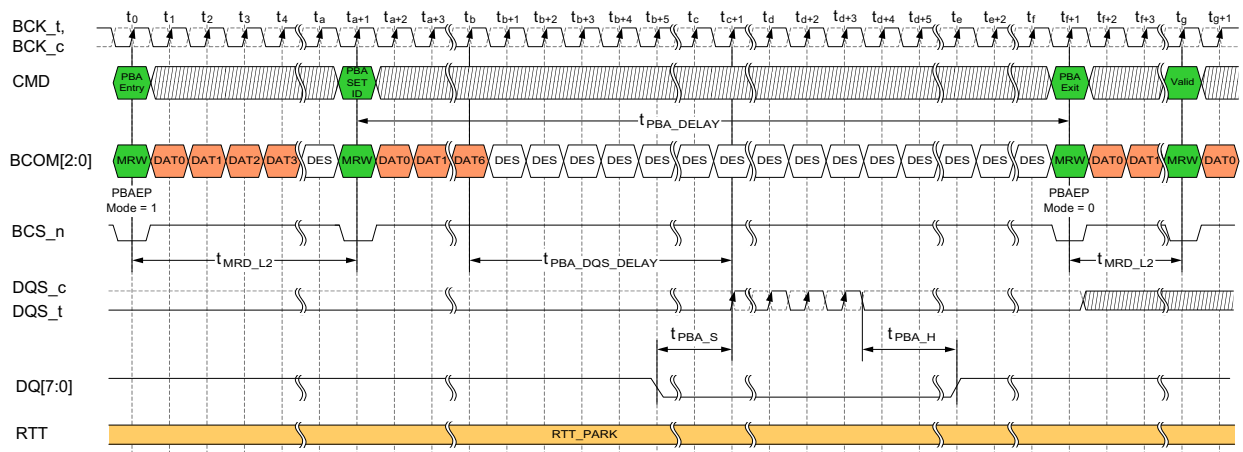
In PBA Enumerate Programming Mode, the default (or previously programmed) RTT<sub>PARK</sub> value will be applied on the DQ signals.

In PBA Enumerate Programming Mode, only PBA Set ID MRW commands and Exit PBA Enumerate Programming Mode MRW commands are allowed.

To remove the MDB from PBA Enumerate Programming Mode, send an Exit PBA Enumerate Programming MRW command. The Exit PBA Enumerate Programming Mode MRW command is never qualified by the DQ settings and is applied to all MDBs.

During the PBA Enumerate ID Programming mode, the Host is only allowed to execute one Enumerate Command in each MDB device (i.e., MRW to PBA Enumerate ID with the corresponding DQ0 or DQ4 bit LOW). Once the PBA Enumerate ID is programmed in a MDB, any change for the PBA Enumerate ID requires the Host to perform a new PBA Enumerate ID Programming sequence.

### 7.3.1 Sequence A - Single Burst of 16 or 32 Strobe Edges



NOTE 7 The PBA Set ID MRW command cycle time is defined as  $t_{PBA\_DELAY}$ . This time is longer than the normal  $t_{MRDL2}$  and must be met in order to provide the MDB time to latch the asserted DQ and complete the write operation to the PBA Enumerate ID control word prior to the next PBA Set ID command.

**Figure 76 — PBAEP Mode Entry, Programming of PBA Enumerate ID, and PBAEP Mode Exit**

Prior to enabling PBA Enumerate Programming Mode, the Host must drive  $DQS\_t$  and  $DQS\_c$  differentially LOW, other than when the burst of 16 strobe edges is sent in association with the PBA Enumerate ID MRW command. The Host must send preamble and postamble  $DQS\_t/DQS\_c$  toggles during the qualification of the PBA command.

Once PBA Enumerate Programming Mode is enabled in the Data Buffer, the Host memory controller shall wait  $t_{MRDL2}$  to the time the first PBA Enumerate ID MRW command is issued.

When a PBA Enumerate ID command is sent, only the buffer which samples its DQ0 bit LOW or its DQ4 bit LOW will enumerate itself with the ID. Data Buffers which sample both the DQ0 bit HIGH AND DQ4 HIGH will retain their previous enumeration ID.

A complete BL16 set of strobe edges in Rank mode or BL32 set of strobe edges in Mux mode (8 or 16 rising edges and 8 or 16 falling edges) must be sent by the Host within the  $t_{PBA\_DQS\_DELAY}$  min/max range from the MRW command. The MDB is allowed to use any one of the strobe edges or set of edges—for example, the last 4 strobe edges—to capture the DQ value during the valid Low duration of the target DQ. Valid Low time is defined as the time between  $t_{PBA\_S}$  and  $t_{PBA\_H}$ . If the MDB captures a 0 on DQ0 or DQ4 at any strobe edge in the strobe sequence, the PBA Enumerate ID command shall be executed by the MDB. Since the write timings for the DQ bus have not been trained, the Host must ensure a minimum of 16 strobe edges in Rank mode or 32 strobe edges in Mux mode occurs after a period of  $t_{PBA\_DQS\_DELAY(min)}$  after the associated MRW command. The BC8 control word setting in the MDB is ignored while in PBA Enumerate Programming mode. The DQS assumes preamble/postamble requirements.

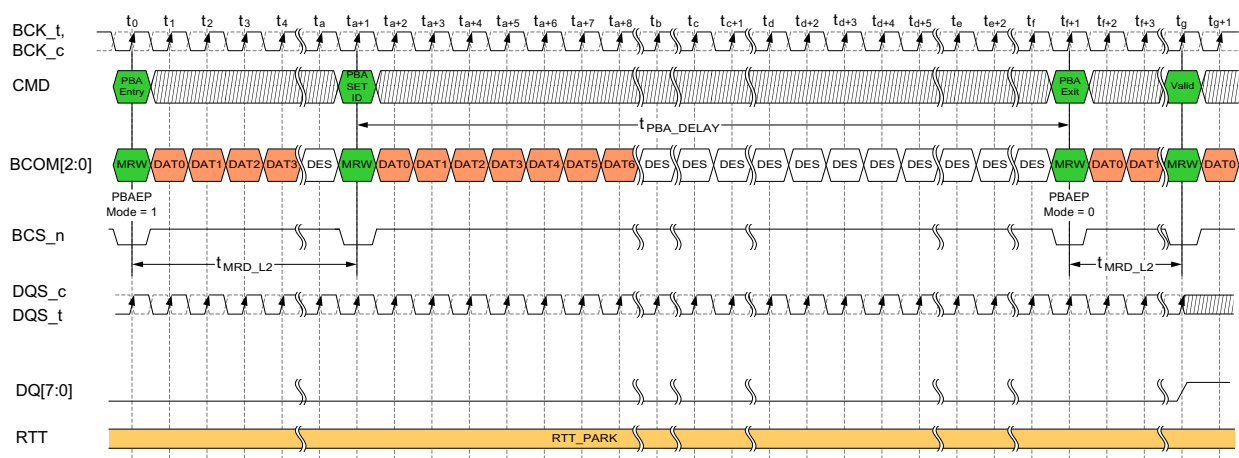
In PBA Enumerate Programming Mode, the default (or previously programmed) RTT\_PARK value will be applied on the DQ signals. An example of PBA Enumerate Sequence A is as follows:

1. All buffers default to ID=15.
2. The Host sends an MRW to the Select ID Control Word with a 15 to select all devices (if not already set that way).
3. The Host begins driving  $DQS\_t$  and  $DQS\_c$  differentially LOW.
4. The Host sends an MRW to the Enumerate Enable Control Word to enable PBA Enumerating Programming mode.

### 7.3.1 Sequence A - Single Burst of 16 or 32 Strobe Edges (cont'd)

5. The Host sends an MRW to the Enumerate ID Control Word with an ID of 0000, driving a 0 onto the DQ signals of the buffer that it desires to enumerate with an ID of 0. The strobes are toggled as described above. The Host drives 1s on all other DQ signals. The Host sends the BL32 strobe sequence on ALL strobes.
6. The Host repeats the above step with IDs of 0001 through 0100 to enumerate the remaining 4 buffers, driving their DQ signals LOW on the appropriate command.
7. The Host sends an MRW to the Enumerate Enable Control Word to Disable PBA mode.
8. All buffers are uniquely enumerated.

### 7.3.2 Sequence B - Continuous DQS Toggle



NOTE 9 The PBA Set ID MRW command cycle time is defined as  $t_{PBA\_DELAY}$ . This time is longer than the normal  $t_{MRD\_L2}$  and must be met in order to provide the MDB time to latch the asserted DQ and complete the write operation to the PBA Enumerate ID control word prior to the next PBA Set ID command.

**Figure 77 — PBA Enumerate Programming Mode with Continuous DQS Toggle Timing Diagram**

Prior to enabling PBA Enumerate Programming Mode, the Host drives the proper DQs low and begins toggling  $DQS\_t/DQS\_c$ . As shown in Figure 77, the Host continues to drive these signals in this manner through the sequence of PBA Enumerate Programming Mode Enable MRW, wait  $t_{MRD\_L2}$ , PBA Set ID MRW, wait  $t_{PBA\_DELAY}$ , Exit PBA Enumerate Programming Mode MRW and, finally, wait until  $t_{MRD\_L2}$  is satisfied. At this point, the Host may stop driving DQ and  $DQS\_t/DQS\_c$  or change the DQ value to enumerate the next buffer and begin the sequence again.

During this sequence, in the period from the PBA Set ID MRW command cycle to the end of  $t_{PBA\_DELAY}$ , the buffer will sample the DQ value. Only the buffer which samples its DQ0 bit LOW or its DQ4 bit LOW will enumerate itself with the ID. Data Buffers which sample both the DQ0 bit HIGH AND DQ4 HIGH will retain their previous enumeration ID.

An example of PBA Enumerate Sequence B is as follows:

1. All buffers default to ID=15.
2. The Host sends an MRW to the Select ID Control Word with a 15 to select all devices (if not already set that way).
3. The Host begins toggling  $DQS\_t$  and  $DQS\_c$ .

### 7.3.2 Sequence B - Continuous DQS Toggle (cont'd)

4. The Host drives a 0 onto the DQ signals of the buffer that it desires to enumerate with an ID of 0. The Host drives 1s on all other DQ signals.
5. The Host sends an MRW to the Enumerate Enable Control Word to enable PBA Enumerating Programming mode.
6. The Host sends an MRW to the Enumerate ID Control Word with an ID of 0000.
7. The Host sends an MRW to the Enumerate Enable Control Word to Disable PBA mode.
8. The Host repeats steps 4-7 with IDs of 0001 through 0100 to enumerate the remaining 4 buffers, driving their DQ signals LOW on the appropriate command.
9. The Host stops driving DQ and DQS\_t/DQS\_c.
10. All buffers are uniquely enumerated.

### 7.3.3 PBA Enumerate Cases

For the “don’t enumerate” case where the MDB ignores the PBA Enumerate ID MRW command in the PBA Enumerate Programming Mode, the DQS\_t/DQS\_c and DQ signals may be high (driven or due to RTT\_PARK termination) prior to sending the MRW command to enter PBA Enumerate Programming Mode. After entering PBA Enumerate Programming Mode, the DQS and DQ signals must remain high (driven or due to RTT\_PARK termination) until exiting PBA Enumerate Programming Mode. Holding the signals high will ensure that this Data Buffer is never set to a PBA Enumerate ID other than the default setting of 0xFh (15). Refer to Table 39 below for a complete list of notes and cases.

**Table 39 — PBA Enumerate Results**

DQS[1:0]_t/DQS[1:0]_c	DQ0/DQ4	PBA Enumerate Result	Notes
<b>Toggling</b>	Low - “0”	Enumerate	1
<b>Toggling</b>	High - “1”	Don’t Enumerate	
<b>High/High, Low/Low, Floating</b>	Low - “0”	Unknown	2
<b>High/High, Low/Low, Floating</b>	High - “1”	Don’t Enumerate	3
<b>High/Low, Low/High</b>	Valid	Don’t Enumerate	

NOTE 1 The MDB will enumerate if either DQ0 or DQ4 is sampled low.

NOTE 2 DQS\_t/DQS\_c are differential signals and small amounts of noise could appear as “toggling”, resulting in “Unknown” PBA Enumerate Results.

NOTE 3 The expected usage case where the DQS signals are High is to have the DQs held High as well. The RTT\_Park may be used to hold these signals high

### 7.4 PBA Select ID Operation

Once the PBA Enumerate ID’s have been programmed in all the Data Buffers, the execution of future MRW. commands depend on the value of the PBA Select ID. If the PBA Select ID is set to 1111B, all Data Buffers will execute the command. For all other values of the select ID, only a buffer enumerated to the same ID as the select ID will respond to the MRW command. An MRW to the PBA Buffer Select ID Control Word will always be executed in all buffers regardless of the current Select ID.

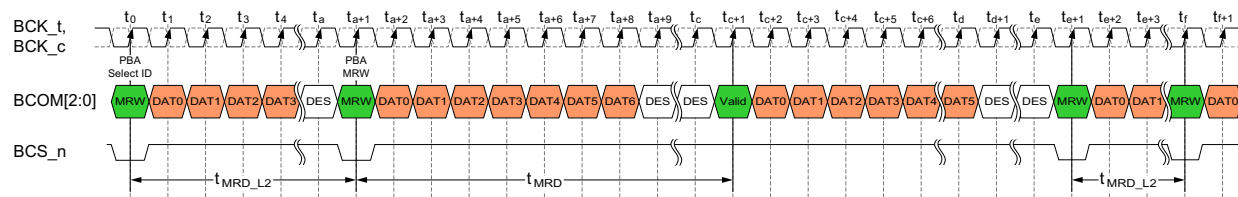
As an example, the following sequence could be used to program unique MR fields per device:

1. Send MRW with ‘PBA Select ID’ opcode, with encoding 0000 included in the opcode.
2. Send MRW’s for field settings specific to Device 0000. This can be any number of MRW’s.
3. Send MRW with ‘PBA Select ID’ opcode, with encoding 0001 included in the opcode.
4. Send MRW’s for field settings specific to Device 0001. This can be any number of MRW’s.
5. Repeat for any number of devices.

## 7.4 PBA Select ID Operation (cont'd)

6. Send MRW with 'PBA Select ID' opcode, with encoding 1111 included in the opcode to enable all Data Buffers to execute all MRW commands.

The timing diagram in Figure 78 shows an example sequencing of the programming of the PBA Select ID and MRW command.



**Figure 78 — PBA Access after ID has been Programmed**



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## 8 Strobe and Data Training Support Features

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For both Rank mode and Mux mode, the MDB shall provide matched rank timings for both read and write operations at the Host interface. The MDB shall absorb the differences in delays required by the backside interface caused by the backside training.

The Host will train to a single delay (cycle and phase) for reads and a single delay (cycle and phase) for writes across all nibbles, ranks and pseudo-channels.

Due to Host side timing alignment, the MDB must buffer Read and Write data for some ranks longer than the nominal value defined in Table 247. The actual propagation delay of these ranks is defined by the following equations:

$$tPDM\_RD\_HA = tPDM\_RD + tRD\_VAR$$

$$tPDM\_WR\_HA = tPDM\_WR + tWR\_VAR$$

The values of  $tRD\_VAR$  and  $tWR\_VAR$  are dependent on the trained timing values of each rank, across both nibbles, and both pseudo-channels (if in Mux Mode).

The baseline  $tPDM\_RD$  is assigned to the rank with the latest (Maximum) DRAM side Read Timing as defined by Receive Enable Cycles (PG[n]RWE0) + Receive Enable Phase (PG[n]RW[E2/E3]) + Read Delay (PG[n]RW[E4/E5]).  $tRD\_VAR$  is then defined as the difference between the latest trained DRAM side Read Timing and that of each rank.

The baseline  $tPDM\_WR$  is assigned to the rank with the earliest (Minimum) DRAM side Write Timing as defined by Write Leveling Cycles (PG[n]RWE1) + Write Leveling Phase (PG[n]RW[E8/E9]) + Write Delay (PG[n]RW[E6/E7]).  $tWR\_VAR$  is then defined as the difference between the earliest trained DRAM side Write Timing and that of each rank.

The maximum  $tRD\_VAR$  and  $tWR\_VAR$ , therefore, define the amount of buffering capability the MDB must support and are defined in Table 247.

The DDR5MDB02 does not contain self-sufficient training state machines for calibrating its timing control settings. It will instead depend on the Host controller to get the timing control registers programmed with the appropriate settings that will allow the MDB to work in the DDR5 MRDIMM environment. To enable the Host controller in performing the training procedure in an efficient and reliable manner, the data buffer provides various Strobe and Data training support features. The following sections describe such training support features in the MDB. The Data Path training modes in Table 40, “Summary of Training Support Features and Functions” and the DFE training are performed with a Fixed BL16.

Table 40 below provides a summary description of the various Strobe and Data training support functions and features in the MDB for the Data Bus Training.

MRCD features a new mode (in PG70RW64[4]) to convert the "MRR" commands (5-UI) into "Read" commands (2-UI) commands preserving the Pseudo-channel and Rank information. This allows the users to target training with back-to-back traffic. All MRR commands are converted to BCOM "Read" commands when PG[70]RW64[4] is set to a 1. Note that the Host controller will always set this bit for MRE, MRD, MWD, HIR, and HPA modes. The MDB is not required to decode MRR commands in MRE, MRD, MWD, HIR and HPA modes in either the Mux mode or the Rank mode. The timing registers in PG[0,1,72,73], and the internal VrefMDQ registers in PG[2]RW[F3:F0] of the register space are still independent per nibble when the DRAM interface x8 strobes are used.

## 8 Strobe and Data Training Support Features (cont'd)

**Table 40 — Summary of Training Support Features and Functions**

Interface	Training Step	Symbol	Direction	Features
DRAM Interface	MDQS Receive Enable	MRE	DRAM to MDB	Receiver enable sampling of MDQS pins Output sample driven out on Host interface DQ pins
	MDQS Read Delay	MRD <sup>1</sup>	DRAM to MDB	Phase adjustment for MDQS input delay using Read Training pattern from DRAM. Data Comparator output sample driven out on Host interface DQ pins
	DRAM Write Leveling	DWL	MDB to DRAM	Transmits MDQS according to write commands generated from Host. Receives DQ feedback from DRAM and sends to Host.
	MDQ Write Delay	MWD <sup>1</sup>	MDB to DRAM	Phase adjustment for MDQ output delay using the Data Buffer <i>Training Pattern Generator</i> for writes to the DRAM and read comparison. Data Comparator output sample driven out on Host interface DQ pins
Host Interface	Host Write Leveling	HWL	Host to MDB	The Data Buffer samples the internal WL Pulse with the Host transmitted strobe pattern and sends the sampled value back to the Host on the DQ signals.
	Host Interface Read	HIR <sup>1</sup>	MDB to Host	The Data Buffer generates the Training Pattern in response to RD's and returns to Host while DRAM interface is disabled.
	Host Preamble	HPA	MDB to Host	The Data Buffer drives Host side strobes differentially LOW other than when driving strobes in response to the RD to access the Training Pattern. In this mode, only a single toggle is supported in the preamble (similar to 1tHDQS preamble setting).
	Host Interface Write	HIW	Host to MDB	The Data Buffer compares the DQ Training Pattern in response to WR's while DRAM interface is disabled.
	Enhanced Write Training	EWTM	Host to MDB	The Data Buffer compares the CRC lane Training Pattern in response to WR's.
	Enhanced Read Training	ERTM	MDB to Host	The Data Buffer generates the CRC lane Training Pattern in response to RD's.

NOTE 1 DRAM CRC modes must be disabled.

The MDB provides separate timing control registers for the lower and upper nibbles. However, there is only one Buffer Training Mode Control Word so both nibbles are always in the same training mode. Table 41 provides an overview of the buffer control words (RW) that are involved in the timing control and timing training features of the MDB.

## 8 Strobe and Data Training Support Features (cont'd)

**Table 41 — Summary of Strobe and Data Timing and Training Control Words**

Page	RWxx	Description	Scope
Direct	RW83	[M]DQS, [M]DQ Training Modes	Select Training mode
	RW94	Internal Receive Enable Offset Coarse Status	Read only Status
	RW95	Internal Receive Enable Offset Fine Lower Nibble Status	Read only Status
	RW96	Internal Receive Enable Offset Fine Upper Nibble Status	Read only Status
	RW97	Buffer Training Configuration Control Word	
	RW98	Buffer Training Status Word for PS0 in the Mux mode, or for Rank 0 and Rank 1 in the Rank mode.	
	RW99	Buffer Training Status Word for PS1 in the Mux mode, or for Rank 2 and Rank 3 in the Rank mode.	
PG[73:72, 1:0] <sup>1</sup>	RWE0	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable	Control per rank/per nibble
	RWE1	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling	
	RWE2	Lower nibble DRAM interface receive enable training control	MRE phase and cycle control per rank
	RWE3	Upper nibble DRAM interface receive enable training control	
	RWE4	Lower nibble MDQS Read delay control	Input control per rank
	RWE5	Upper nibble MDQS Read delay control	
	RWE6	Lower nibble MDQ Write Baseline delay control	Output control per rank
	RWE7	Upper Nibble MDQ Write Baseline Delay	
	RWE8	Lower nibble DRAM interface write leveling control	Write leveling phase and cycle control per rank
	RWE9	Upper nibble DRAM interface write leveling control	
	RWEA	MDQ0/4-Read delay control	Input control per rank/per bit
	RWEB	MDQ1/5-Read delay control	
	RWEC	MDQ2/6-Read delay control	
	RWED	MDQ3/7-Read delay control	
	RWEE	MDQ0/4-MDQS Write delay control	Output control per rank/per bit
	RWEF	MDQ1/5-MDQS Write delay control	
	RWF0	MDQ2/6-MDQS Write delay control	
	RWF1	MDQ3/7-MDQS Write delay control	

NOTE 1 In the Mux mode, PG[73:72, 1:0] are used for Rank1 and Rank 0 of PS1 and PS0. In the Rank mode, PG[73:72, 1:0] are used for Rank 3, Rank 2, Rank1, and Rank 0.

### 8.1 MRE: DRAM Interface MDQS Receive Enable Training Mode

The problem is how to find the optimal settings that will allow the data buffer to work reliably in the MRDIMM environment. To help the Host controller solve this problem, the data buffer provides a DRAM interface receive enable phase training mode. In this training mode, the data buffer uses a group of programmable delay elements and sampling circuits to capture the MDQS<sub>x</sub> t/MDQS<sub>x</sub> c signals received from the DRAMs. This is accomplished by the rising edge of the MDB Receive Enable signal sampling the MDQS<sub>x</sub> t/MDQS<sub>x</sub> c signals and sending this sampled value to the Host via the DQ signals per nibble.

## 8.1 MRE: DRAM Interface MDQS Receive Enable Training Mode (cont'd)

This training mode has been defined so that it can be performed before any training has taken place between the Host controller and the MDB.

The MDB will support Per-Rank, Upper and Lower Nibble - Receive Enable cycle adjustment = -7, -6, -5, -4, -3, -2, -1, 0, 1, 2, 3, 4, 5, 6, 7 (signed magnitude) as defined in [PG\[0,1,72,73\]RWE0](#).

The MDB will support Per-Rank, Upper and Lower Nibble - Receive Enable phase adjustment (6 bits, 1/64th tBCK granularity) as defined in [PG\[0,1,72,73\]RW\[E3:E2\]](#).

The MDB will also include read-only register for the internal Receive Enable offset that is applied by the MDB after exiting the MRE training mode as defined in [RW\[96:94\]](#).

The DRAM interface receive enable timing selection is controlled in steps of  $1/64 * tBCK$  by [PG\[0,1,72,73\]RW\[E3:E2\]](#). The Host controller has the ability of setting the values for this parameter by means of MRW Write commands. When the Receive Enable training control bits [PG\[0,1,72,73\]RW\[E3, E2, E0\]](#) are all set to zero delay (default settings), the rising edge of the input-referred receive enable is aligned to a rising edge BCK that corresponds to a read latency of DB\_RL. In this training mode, the output of each MDQSx\_t/MDQSx\_c (MDQS0 in x8 DRAM case, or MDQS[1:0] in x4 DRAM case) sampling circuit is driven onto the four Host interface DQ pins corresponding to each nibble. In this training mode, the DQS\_t/DQS\_c inputs and outputs at the Host interface are disabled. To perform receive enable phase training, the Host will first enable the MDQS Receive Enable Training mode in [RW83](#). After that, if the DRAMs have already been initialized, the Host will send a sequence of MRR commands to the DRAMs to access the Read Training Pattern. This may be any number of consecutive or non-consecutive DRAM MRR commands. The DRAM will be in Preamble Training Mode, causing the MDQSx\_t/MDQSx\_c inputs of the data buffer to be differentially LOW other than when the DRAM responds with a read burst due to the MRR command. The DRAM will generate a train of pulses in the MDQSx\_t/MDQSx\_c inputs of the data buffer according to the number of MRR commands sent by the Host. The data buffer will use the RANK\_ID field in the RD Command sequences received through the BCOM[2:0] interface to select which receive enable timing control register will be used during training. The MDB will use [PG\[0,72\]RW\[E3:E2\]](#) for Rank 0 (and Rank 2 in the Rank mode), and [PG\[1,73\]RW\[E3:E2\]](#) for Rank 1 (and Rank 3 in the Rank mode). Using the output of the sampling circuits available on the DQ pins, the Host controller will be able to decide if it needs to increase or decrease the receive enable phase control settings in the data buffer by means of MRW commands. The objective is to find the end of the DRAM read preamble, i.e. first effective rising edge of MDQS\_t. At this time, the output of the sampling circuits will change from LOW to HIGH. With this method, the Host controller will be able to align the rising edge of the internal receive enable to the first effective rising edge of the incoming MDQSx\_t/MDQSx\_c signals. The Host will use combinations of cycle and phase settings to determine the first effective rising strobe edge of the read burst. The Host may send any number of back-to-back DRAM MRR commands to accomplish this step. The MDB will sample only during the rising edge of the Receive Enable signal and will hold this sample on the DQ signals to the Host until the next Receive Enable rising edge. For back-to-back RDs, there is only one read enable rising edge at the beginning of the contiguous burst. The MDB will apply an internal offset adjustment after training to account for correct centering within the programmed preamble timing. The final offset will take effect once the Host exits the MRE training mode. The Host must program the correct preamble timing prior to execution of the training sequence.

On the Host interface, while in MRE training mode, the MDB continuously enables its DQ drivers, and disables its DQ receivers and DQ termination DQ\_RTT\_PARK. Also, the Data Buffer disables its DQS drivers and receivers. It applies DQS\_RTT\_PARK continuously on DQS if enabled.

The data buffer provides a Read FIFO fall-through time for each rank and for correct operation this delay cannot change. Any potential adjustments to this data buffer Read FIFO fall-through time have to be performed prior to this training step. The Host is responsible for performing trainings between MDB and DRAM for each rank.

The DRAM interface receive enable timing established in this training step is also used by the MDB for the driver enable for the DQ/DQS outputs for Read commands (by adding an offset that corresponds to the Read FIFO flow-through time).

## 8.1 MRE: DRAM Interface MDQS Receive Enable Training Mode (cont'd)

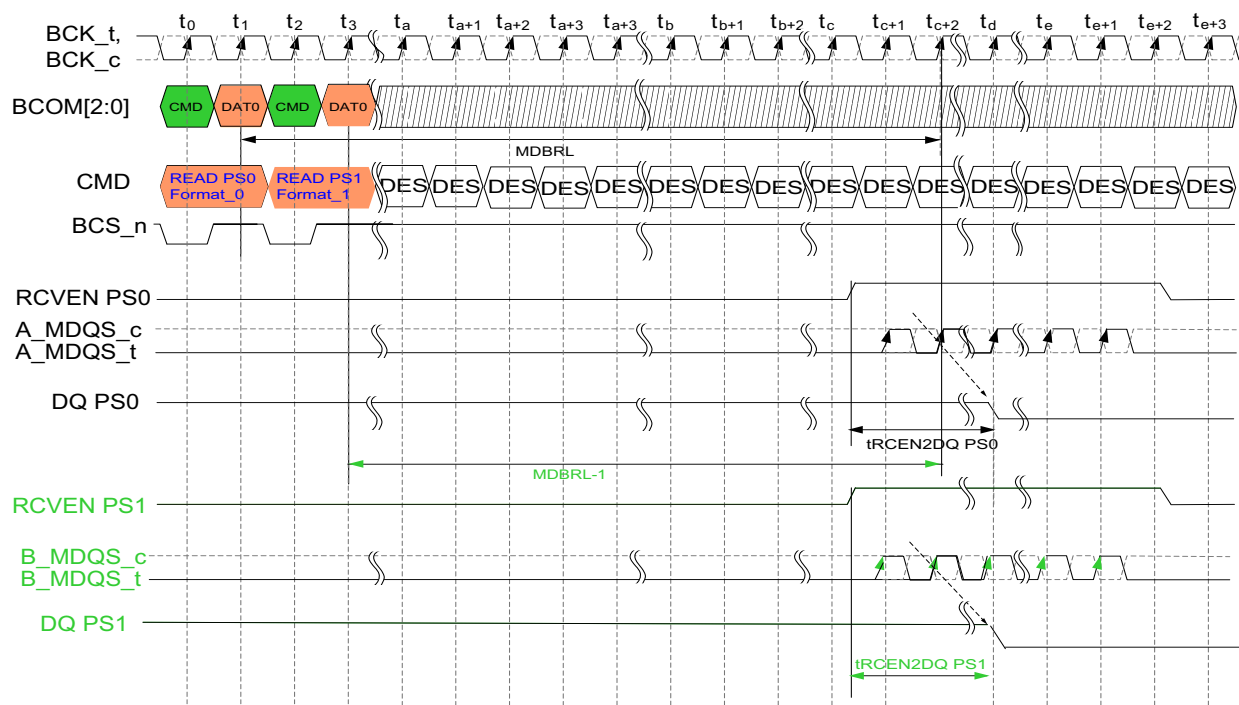
To exit this training mode, the Host controller can resume normal operation or enable other training modes with an MRW to [RW83](#).

For MRDIMM, when the MDB is in MRE Training Mode it samples the incoming MDQS strobe from the DRAM with the rising edge of its internal Receive Enable signal to generate feedback back to the Host.

In the Rank mode, the MDB has one MDQS strobe coming in at a time. In the Mux mode the MDB has two MDQS strobes coming in, one per pseudo-channel (PS). In order to be able to train both PS in parallel, the Host issues MRR reads to DRAM space MR31 to PS0 and PS1 to generate the MDQS strobe toggles. The MDB in MRE mode samples the incoming MDQS strobes with its internal Receive Enable signal upon receiving read commands. MDB will recover the PS and rank information from the read command to apply the corresponding RcvEn delays being targeted. PS0 and PS1 feedback goes out to the Host according to the configuration of MDB [PG\[70\]RWE5](#) Register. For example, if [PG\[70\]RWE5](#) = 0xCC then the MDB will output the feedback for PS0 on DQ0, DQ1 for the low nibble and DQ4, DQ5 for the high nibble and the MDB will output the feedback for PS1 on DQ2, DQ3 for the low nibble and DQ6, DQ7 for the high nibble.

Receive Enable Cycle Adjustment and Receive Enable phase adjustment registers are independent for each of the ranks on the low nibble and on the high nibble.

In Figure 79, two Read commands on BCOM are issued to train both PS in parallel during MRE training.



1. MDB RCVEN is HIGH when the MDB input receivers are enabled for sampling the MDQS\_t/MDQS\_c strobe signals from DRAM devices.

**Figure 79 — MRE Timing Diagram Read to both PS in Parallel**

Figure 79 shows an example of MRR read to both PS in parallel. MDB is in MRE mode and MRCD converts MRR to Read, MDB uses read command to generate the Receive Enable (RcvEn) pulse and sample the incoming MDQS strobes, and generates feedback for each PS back to the Host.

## 8.2 MRD: MDQS Read Delay Training Mode

In this mode, the MDB uses its Read Training Pattern generator along with data comparators to determine if the read data from the DRAM matches the expected result. The result of the comparison is used to generate the feedback that is sent back to the Host.

In the Rank mode, MDB has one source of data coming in at a time. In the Mux mode, MDB has two sources of data coming in, one for each pseudo-channel (PS). In order to be able to train both PS in parallel, the Host issues MRR reads to DRAM space MR31 to PS0 and PS1 to get patterns from DRAM Read Training Pattern. The Host can program the DRAM Read Training Pattern for each PS with the same pattern or different pattern. The Host can configure MDB to snoop DRAM Read Training Pattern registers and apply to PS0, PS1 or both (PG[8]RWE2).

The Host can also program each PS Read Training Pattern MDB registers as needed. Once the MDB is in MRD mode and the MRCD is programmed to replace MRR commands with Read commands on the BCOM interface (PG[70]RW64[4]), the MDB will perform the pattern comparisons for target PS(s) upon receiving read commands. MDB will recover the PS and rank information from the read command to apply the corresponding MDQS Read Delay and MDQ Phase control being targeted. PS0 and PS1 feedback resulting from the pattern comparisons goes out to the Host according to the configuration of MDB PG[70]RWE5.

The delay registers used for MDQS Read Delay and the per MDQ Phase control are independent for each of the ranks on the low nibble and on the high nibble.

For the DRAM-to-DB read training, the MDQS delay adjustments are performed in the data buffer so that it can correctly sample the data driven by the DRAM. The data buffer provides data pattern control words that are programmed with the expected read data pattern from the DRAM and the results of the comparison are provided on the data buffer Host interface.

To perform DRAM-to-MDB read training, the Host will first enable the MDQS read delay (MRD) training mode in the Training Mode Control Word RW83.

The delay of the DRAM interface data strobe signals (MDQSx\_t/MDQSx\_c) during read transactions is selected by buffer control word PG[0,1,72,73]RW[E5:E4] for upper and lower nibble respectively. The nominal setting for PG[0,1,72,73]RW[E5:E4] is  $(1+1/4)*tBCK$  in the unmatched receivers mode, or  $(1/4)*tBCK$  in the matched receivers mode. The Host controller may need to perform additional iterations of the training procedures, including Host Interface Read Training, when non-default settings are written into PG[0,1,72,73]RW[E5:E4].

In this training mode, the data buffer uses a data pattern comparator to determine if the read data from the DRAMs matches an expected result. In the Mux mode, each PS has an independent LFSR pattern generator so the two PS can be trained in parallel. The expected data pattern values are stored in Read Pattern 0 and Read Pattern 1 the control words PG[8]RW[E4,E3] and PG[8]RW[EA,E9], or the expected data pattern is generated by LFSR pattern generators. There are two data comparators per data buffer, with a selected per-MDQ comparison results. One data comparator is for PS0 in the Mux mode or Rank 0 and Rank 1 in the Rank mode. The other data comparator is for PS1 in the Mux mode or Rank 2 and Rank 3 in the Rank mode. The output of the data comparator is driven onto the Host connector interface on DQ pins.

- If the data pattern is matched, the DQ pins drive HIGH until the next comparison takes place or until the training mode is disabled.
- If the data pattern is not matched, the DQ pins drive LOW until the next comparison takes place or until the training mode is disabled. RW97[3] selects whether all four DQ bits within a nibble are driven LOW see Table 42 for functional description. The control words PG[8]RW[E6:E2] and PG[8]RW[EC:E9] are used to configure these pattern generators. When the LFSR pattern generators are enabled, the Host may send a long sequence of MRR commands for continuous comparison to the read training pattern. The DQ feedback to the Host must indicate a match '1' or a mis-compare '0' after each read burst of each Read command has completed. See Table 42. The comparison can also be configured to look at specific UI's within the read burst. RW97 is used to configure the UI filtering for the comparison.

## 8.2 MRD: MDQS Read Delay Training Mode (cont'd)

When using a Serial pattern, [PG\[8\]RW\[E9,E3\]](#) will contain the expected first 8 UI for all MDQ signals. [PG\[8\]RW\[EA,E4\]](#) will contain the expected last 8 UI for all MDQ signal. The Serial pattern can also be inverted per MDQ lane, [PG\[8\]RW\[EB,E5\]](#) indicates which DQ signals are inverted. These settings should match the DRAM configuration for the Read Training Pattern. The MDB shall support snooping of the DRAM MR settings for the Read Training Pattern configuration.

In addition to driving the DQ pins, status for the pattern comparison is also provided in the Buffer Training Status word [RW98](#) and [RW99](#). In the Mux mode, [RW98](#) is for PS0 and [RW99](#) is for PS1. In the Rank mode, [RW98](#) is for Rank 0 and Rank 1, and [RW99](#) is for Rank 2 and Rank 3. The status provided in [RW98](#) and [RW99](#) can be modified by the Buffer Training Configuration control word [RW97](#), to provide status of a mis-compare with or without UI filtering applied. The status in [RW98](#) and [RW99](#) is always per DQ lane.

On the Host interface, while in MRD training mode, the MDB continuously enables its DQ drivers, and disables its DQ receivers and DQ termination [DQ\\_RTT\\_PARK](#). Also, the Data Buffer disables its DQS drivers and receivers. It applies [DQS\\_RTT\\_PARK](#) continuously on DQS if enabled.

The MDB is required to support fine adjustment of the phase of individual bit lanes relative to the baseline MDQS. For this purpose, the Host controller can utilize the per lane MDQS-MDQ read delay control words [PG\[0\]RWEA](#) controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, [PG\[0\]RWEB](#) controls the phase bits MDQ1 and MDQ5 for Rank 0, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of +/- 3/64 tBCK is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQS delay in [PG\[0,1,72,73\]RW\[E5:E4\]](#) for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQS delay in [PG\[0,1,72,73\]RW\[E5:E4\]](#) for the entire nibble.

To exit this training mode, the Host controller can resume normal operation or enable other training modes with an MRW to [RW83](#).



## 8.2.1 UI filtering and Sticky Status Summary Table

Table 42 — UI filtering and Sticky Status Summary Table

Long-RD Pattern Sticky Status	Status Format <sup>1</sup>	UI Filtering	DQ Output (HIGH = No Error, LOW= Error)
Disabled	Per Transaction	Disabled (default)	For each BL16 RD command, an error during the burst on any UI of any bit lane of a nibble for x4 DRAM or byte for x8 DRAM will set all DQ bits of the nibble/byte LOW. When set LOW, this level is held until the next BL16 RD command or until the Clear Feedback Status bit in <a href="#">RW97[0]</a> is asserted or MDB reset.
		Enabled	For each BL16 RD command, an error during the burst on the selected UI of any bit lane of a nibble for x4 DRAM or byte for x8 DRAM will set all DQ bits of the nibble/byte LOW. When set LOW, this level is held until the next BL16 RD command or until the Clear Feedback Status bit in <a href="#">RW97[0]</a> is asserted or MDB reset.
	Per Bit Lane (default)	Disabled (default)	For each BL16 RD command, an error on any UI of bit lane-x of the burst will set DQ[x] LOW. When set LOW, this level is held until the next BL16 RD command or until the Clear Feedback Status bit in <a href="#">RW97[0]</a> is asserted or MDB reset.
		Enabled	For each BL16 RD command, an error on the selected UI of bit Lane-x of the burst will set DQ[x] LOW. When set LOW, this level is held until the next BL16 RD command or until the Clear Feedback Status bit in <a href="#">RW97[0]</a> is asserted or MDB reset.
Enabled <sup>2</sup> (default)	Per Transaction	Disabled (default)	For each BL16 RD command, an error during the burst on any UI of any bit lane of a nibble for x4 DRAM or byte for x8 DRAM will set all DQ bits of the nibble/byte LOW. When set LOW, this level is held until the Clear Feedback Status bit in <a href="#">RW97[0]</a> is asserted or MDB reset.
		Enabled	For each BL16 RD command, an error during the burst on the selected UI of any bit lane of a nibble for x4 DRAM or byte for x8 DRAM will set all DQ bits of the nibble/byte LOW. When set LOW, this level is held until the Clear Feedback Status bit in <a href="#">RW97[0]</a> is asserted or MDB reset.
	Per Bit Lane (default)	Disabled (default)	For each BL16 RD command, an error on any UI of bit lane-x of the burst will set DQ[x] LOW. When set LOW, this level is held until the Clear Feedback Status bit in <a href="#">RW97[0]</a> is asserted or MDB reset.
		Enabled	For each BL16 RD command, an error on the selected UI of bit Lane-x of the burst will set DQ[x] LOW. When set LOW, this level is held until the Clear Feedback Status bit in <a href="#">RW97[0]</a> is asserted or MDB reset.

NOTE 1 In the Per Transaction mode, MDB will provide per-nibble comparison result for x4 DRAM configuration, or per-byte comparison result for x8 DRAM configuration.

NOTE 2 After exiting the training mode (i.e., MRD or MWD), the feedback status will be removed from the DQ pins to support Read/Write normal operation. The MDB hardware may clear the sticky status, but the Host is required to set the Clear Feedback Status bit in [RW97\[0\]](#) to guarantee that the sticky status will not be carried over into a new (MRD or MWD) training mode entry.



### 8.3 MWD: MDB-to-DRAM Write Delay Training Mode

For the MDB-to-DRAM write delay training, the MDQ-MDQS delay adjustments are performed in the data buffer so that the DRAM receives the MDQ and MDQS signals with the optimal phase relationship. The Host-to-MDB data path has not been trained at this time so the data that is written to the DRAM comes from a pattern generator that is configured with MDB MRW commands through the DDR5 register via the BCOM bus. Since the MDB to DRAM write training requires reading back the data for correctness it is performed after the DRAM to MDB read training has already been finished.

The Host will ensure that MWD training is only performed with delay values in [PG\[A,71\]](#) cleared to zero.

To perform MDB-to-DRAM write training, the Host will first enable the MDQ-MDQS write delay (MWD) training mode in the Training Mode Control Word ([RW83](#)). In the Mux mode, each PS has an independent LFSR pattern generator so the two PS can be trained in parallel. The MDB will use the pattern generation capability for MWD training. The configuration state for the patterns is the same for the read comparison pattern and the write pattern. Therefore, there is no need to duplicate these configuration registers. The logic to generate the patterns must enable independent state transitions for write pattern versus read comparison pattern, due to the timing difference for when these patterns are used.

When the LFSR pattern is enabled, the current state for each LFSR can be read from WRITE LFSR registers [RW\[9F:9E\]](#) and [PG\[70\]RW\[EF:EE\]](#), and READ LFSR registers [RW\[9D:9C\]](#) and [PG\[70\]RW\[ED:EC\]](#). MWD mode must first be exited to read these registers. While the MDB is in the MWD training mode, the Host sends write commands to an arbitrary DRAM location. The Host must not drive DQ during MWD training since the MDB will be continuously driving training result status. The data for these Write commands come from the MDB write pattern generators.

The Host issues write commands to one selected rank in the Rank mode, or one or both PS in the Mux mode. The MDB generates the write pattern for the target rank or PS (one or both) based on the configuration of its Read Training Pattern registers and based on the PS and rank information from the write command. The MDB has two Pattern Generators. One Pattern Generator is for PS0 in the Mux mode or Rank 0 and Rank 1 in the Rank mode. The other Pattern Generator is for PS1 in the Mux mode or Rank 2 and Rank 3 in the Rank mode. MDB will recover the PS and rank information to apply the proper MDQ-MDQS delay when outputting the data. The Host then performs a read to the selected rank (on one or both PS in Mux mode), and the MDB compares the received pattern against the “previously sent” pattern. The Host can program the DRAM Read Training Pattern for each PS with the same pattern or different pattern. The Host can configure MDB to snoop DRAM Read Training Pattern registers and apply to PS0, PS1 or both defined in [PG\[70\]RWE4](#). The Host can also program each PS Read Training Pattern MDB registers as needed. The results for the write vs. read comparisons produced by the MDB for each PS is asynchronously sent back to the Host through the DQ pins. Feedback for each PS is sent out is independent of the other PS. When the MDB is configured per-transaction in [RW97\[3\]](#), PS0 and PS1 feedback resulting from the pattern comparison per transaction goes out to the Host according to the configuration of MDB [PG\[70\]RWE5](#). When the MDB is configured per-bit, the Host will only be able to see the per-DQ feedback for the PS that was selected in [PG\[70\]RWE5](#). In this case, the Host requires two passes to see the per-DQ feedback of both PS, doing one PS at a time.

The MDQ-MDQS delay adjustment registers are independent for each rank in the Rank mode, or for each of the Pseudo-Channels in the Mux mode on the low nibble and on the high nibble.

To check whether the writes were successful, the Host reads the data back from the same DRAM location and the data buffer performs a bit wise comparison with the read comparison pattern. The feedback on the DQ pins to the Host will indicate a mis-compare in the same way as defined for the MRD training mode. All configuration settings for per-bit sticky error status or per transaction error events are the same as for the MRD training mode. The UI filtering and Training Status word are also the same. The phase relationship between the DRAM interface data strobe signals (MDQSx\_t/MDQSx\_c) and their corresponding data signals (MDQx) during write transactions is selected by buffer control words [PG\[73,72,1,0\]RWE6](#) and [PG\[73,72,1,0\]RWE7](#) for lower and upper nibble respectively. The MDB uses the RANK ID fields in the BCOM Write Command and Read Command sequences to select the correct DRAM interface write leveling and DRAM interface receive enable timings for Writes and Reads respectively. The MDB also uses this rank information to exercise the appropriate MDQ-MDQS settings.

### 8.3 MWD: MDB-to-DRAM Write Delay Training Mode (cont'd)

Due to the unmatched receiver in the DRAM, the range of the MDQ signal timings must account for the unmatched range.

On the Host interface, while in MWD training mode, the MDB continuously enables its DQ drivers, and disables its DQ receivers and DQ termination  $DQ\_RTT\_PARK$ . Also, the Data Buffer disables its DQS drivers and receivers. It applies  $DQS\_RTT\_PARK$  continuously on DQS if enabled. CRC modes must be disabled.

For DDR5 data rates, fine adjustment of the phase of individual MDQ bit lanes relative to MDQS are required. For this purpose, the Host controller can utilize the per lane MDQ-MDQS write delay control words through [PG\[73,72,1,0\]RWE](#) controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively, [PG\[73,72,1,0\]RWEF](#) controls the phase bits MDQ1 and MDQ5, and so on. Since all bits within a nibble are generally aligned by routing, only a small range of  $\pm 3/64$  tBCK is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQ delay in [PG\[73,72,1,0\]RW\[E7:E6\]](#) for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQ delay in [PG\[73,72,1,0\]RW\[E7:E6\]](#) for the entire nibble.

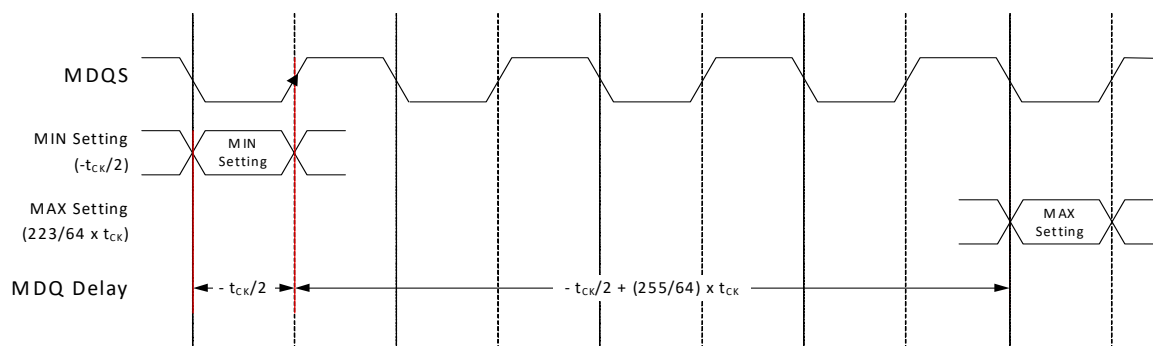


Figure 80 — MDQ Write Baseline Delay

To exit this training mode, the Host controller can go back to resume normal operation or enable other training modes with an MRW to [RW83](#).

### 8.4 DWL: DRAM Write Leveling Training Mode

In DWL mode, the MDB will drive MDQS differentially low and only toggle upon receiving a write command in the BCOM interface.

In the Rank mode, the MDB drives MDQS strobes to one selected rank upon receiving a write command. In the Mux mode, the data buffer now drives MDQS strobes for two pseudo-channels (PS). Upon receiving a write command, the MDB will toggle MDQS for one rank, one PS or both, depending on the rank and PS selection received in the BCOM write command. To train both devices in parallel the Host might issue the write commands to PS0 and PS1 in parallel, or it may issue a write command to PS0 followed by a write command to PS1. The MDQS toggle is referenced to the DAT0 of the BCOM write command. This is to align with the functional behavior when a bubble is created in the BCOM due PS0 and PS1 commands overlap. The strobe toggles generated by the MDB for one rank or each PS will reach the DRAM devices and feedback from DRAM devices will come back to the MDB. The MDB forwards the DRAM's WL response asynchronously from its respective MDQ input pins to their corresponding DQ output pins based on the configuration of MDB [PG\[70\]RWE5](#) so that the Host can read the response.

8.4 DWL: DRAM Write Leveling Training Mode (cont'd)

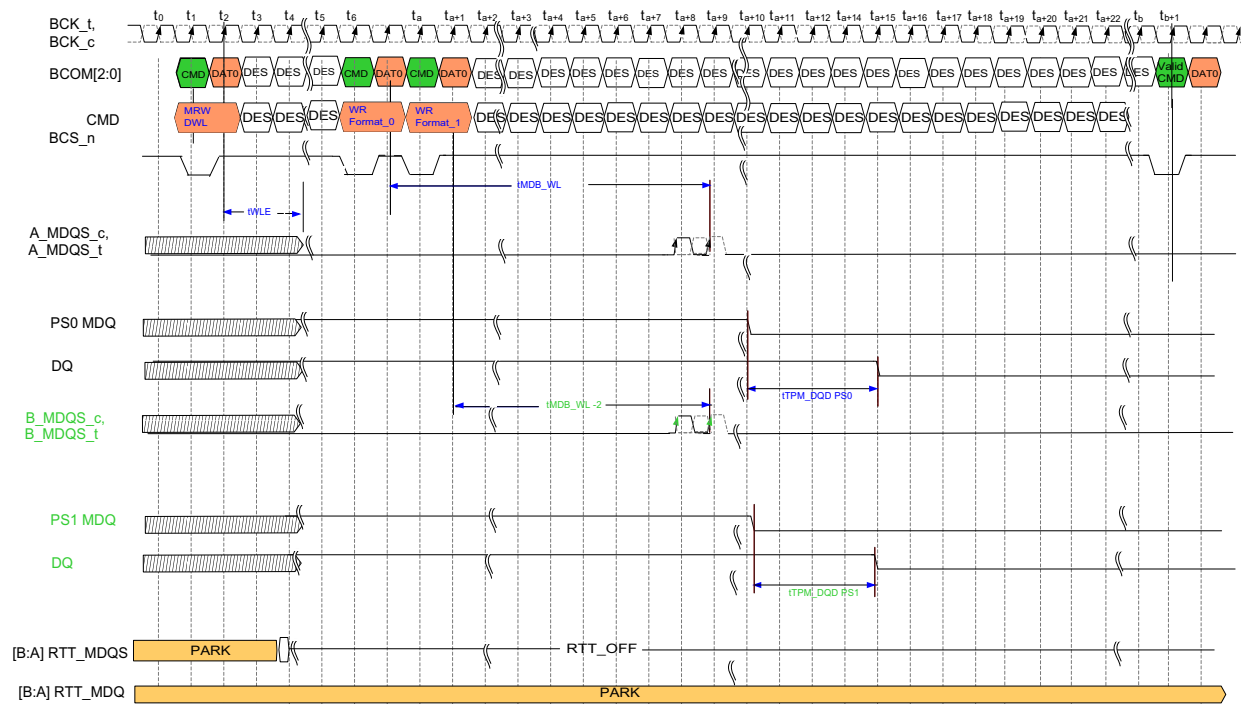
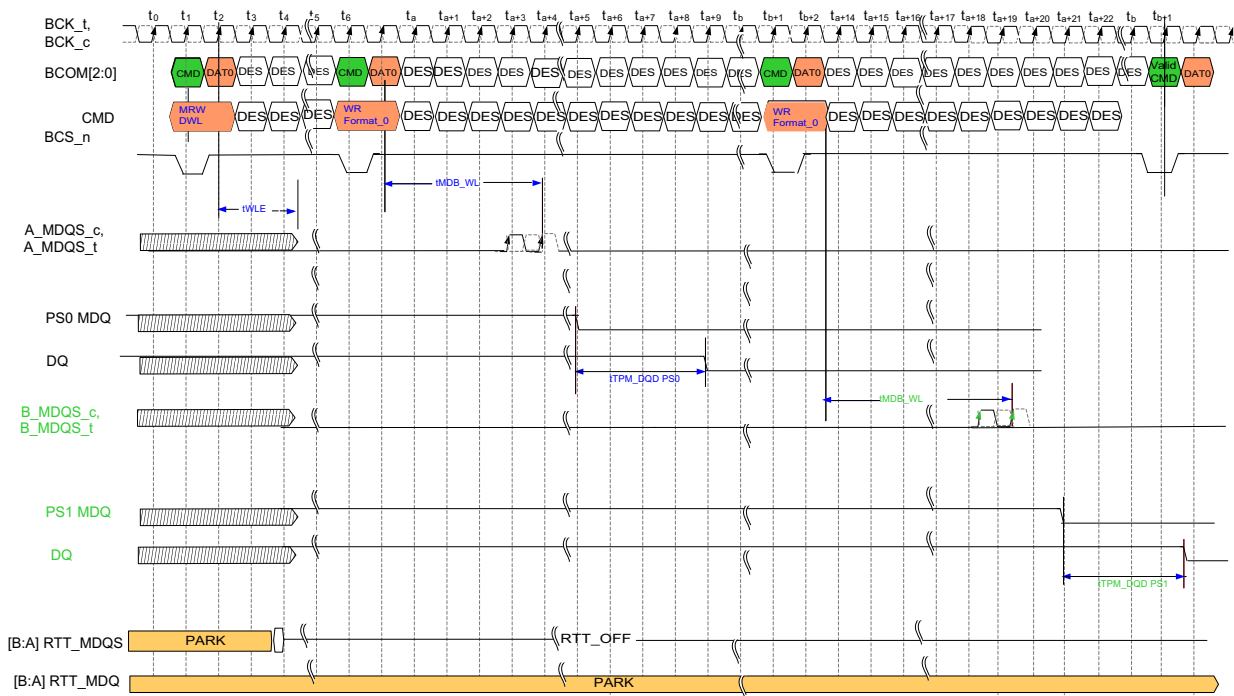


Figure 81 — DWL Write Command to both PS in Parallel

The Figure above shows an example of sending the write command to both PS in parallel. The MDB generates the MDQS strobe toggles at DB\_WL which is referenced to the second cycle of the BCOM command.

## 8.4 DWL: DRAM Write Leveling Training Mode (cont'd)



**Figure 82 — DWL Write Command to PS0 First, followed by a Write Command to PS1**

Figure 82 shows an example of sending the write command to PS0 first, followed by a write command to PS1. The MDB generates the strobe toggles at  $DB\_WL$  which is referenced to the second cycle of the BCOM command.

The MDB supports both DRAM write leveling (WL) training modes: external WL training and internal WL training with the same DRAM-interface write leveling (DWL) training mode selected via [RW83](#).

For each nibble, the Data Buffer must have an adjustable delay setting per rank to align the first effective rising edge of its differential MDQS with the timing at the DRAM receiver. This adjustable delay in the data buffer is programmed using [PG\[73,72,1,0\]RWE1](#) and [PG\[73,72,1,0\]RW\[E9:E8\]](#) control words.

When the Data Buffer enters DWL training mode, it drives both MDQS differentially LOW ( $MDQSy\_t = \text{LOW}$ ,  $MDQSy\_c = \text{HIGH}$ ) at all times except when it is generating a training pattern. When a target WRITE command is received, the Data Buffer generates the training pattern which is the preamble and the first functional MDQS pulse. The pre-amble format is snooped by the Data Buffer and stored in [PG\[8\]RWE1](#). The minimum  $t_{CCD}$  (Command to Command Delay time) between write commands is  $8t_{BCK}$ .

The rising edge of the first functional MDQS pulse occurs  $DB\_WL(Rx, Ny)$  after the DAT0 cycle of a WRITE command sequence, where  $Rx$  represents rank  $x$  and  $Ny$  represents nibble  $y$ . Rank  $x$  is the rank being trained and is selected by the Rank\_ID field in the DAT0 cycle of the write command sequence.

In DWL for each nibble, the Data Buffer forwards the DRAM's WL response asynchronously from its respective MDQ input pins to their corresponding DQ output pins so that the Host can read the response.

On the Host interface, while in DWL training mode, the Data Buffer continuously enables its DQ drivers, and disable its DQ receivers and DQ termination  $DQ\_RTT\_PARK$ . Also, the Data Buffer disables its DQS drivers and receivers. It applies  $DQS\_RTT\_PARK$  continuously on DQS if enabled.

## 8.4 DWL: DRAM Write Leveling Training Mode (cont'd)

On the DRAM Interface, while in DWL training mode, the Data Buffer disables its MDQ drivers, and it continuously enables its MDQ receivers. It continuously applies MDQ\_RTT\_PARK if enabled. The MDB operates its MDQS drivers as described above. It may disable its MDQS receivers. It disables MDQS\_RTT\_PARK.

The Data Buffer must continue to process MRWs normally in DWL mode to allow the Host to adjust its related delay registers. The Host will only send target write commands to the MDB, and non-target write commands are illegal.

Figure 82 shows the sequence of events for Data Buffer DWL training. The DRAM requires MDQS to be driven differentially LOW before it enters WL training mode. Therefore, the Data Buffer must be placed in DWL training mode prior to placing the DRAM in either of the WL training modes. Upon entering DWL mode the MDB will begin driving MDQS differentially LOW, and it will apply all of its other IO states mentioned previously. When the Data Buffer receives a WRITE command, it generates the pre-amble and the first functional MDQS pulse. When the rising edge of the first functional MDQS pulse samples the DRAM's internal WL pulse, the DRAM returns the sampled result after  $t_{WLO}$  on all of its DQ outputs. Once the MDB receives the sample result it propagates this information to its respective DQ outputs  $t_{TPM\_DQD}$  later.

The Data Buffer's output mismatch uncertainty between its DQ while in DWL training mode is  $D_{TPM\_DQ}$ . Therefore, the Host must expect an accumulative mismatch uncertainty of DRAM and Data Buffer.

## 8.5 HWL: Host Interface Write Leveling Training Mode

The Data Buffer supports a Host-interface write leveling (HWL) training mode that is similar to the DRAM's external WL training mode. For each nibble-y, prior to placing the MDB in HWL training mode the Host is required drive DQS differentially LOW ( $DQSy\_t = \text{LOW}$ ,  $DQSy\_c = \text{HIGH}$ ).

Once the Host places the Data Buffer in HWL training mode, the Host is required to drive DQS differentially LOW except when it generates a training pattern. For each write command, the Host generates only the preamble and the first functional pulse on DQS. The preamble pattern depends on the selected preamble mode.

When the Data Buffer is in HWL training mode, for each target write command the Data Buffer always generates a one-cycle wide pulse on each of its per-nibble internal WL pulse signals. The rising edge of each WL pulse is aligned with the internal WL timing point that is  $DB\_WL(Rx, Ny) - t_{PDM\_WR}$  after the DAT0 cycle of the write command, where Rx represents rank x and Ny represents nibble y. Rank x is the rank being trained and is selected by the Rank\_ID field in the DAT0 cycle of the write command sequence. At all other times, each per-nibble WL pulse signal is LOW.

For nibble-y, the WL pulse signal is sampled by each rising edge of its respective DQS, including any rising edges within the preamble. The DQS burst can arrive any time after the write command. Figure 83 shows the case where the rising edge of the DQS preamble samples the LOW level prior to the WL pulse, and the rising edge of the first functional DQS pulse samples the HIGH level of the WL pulse. The MDB asynchronously outputs each sample on the nibble's four DQ outputs after  $t_{TPM\_DQD}$ . The MDB's output mismatch uncertainty between its per-nibble DQ outputs is  $D_{TPM\_DQ}$ .

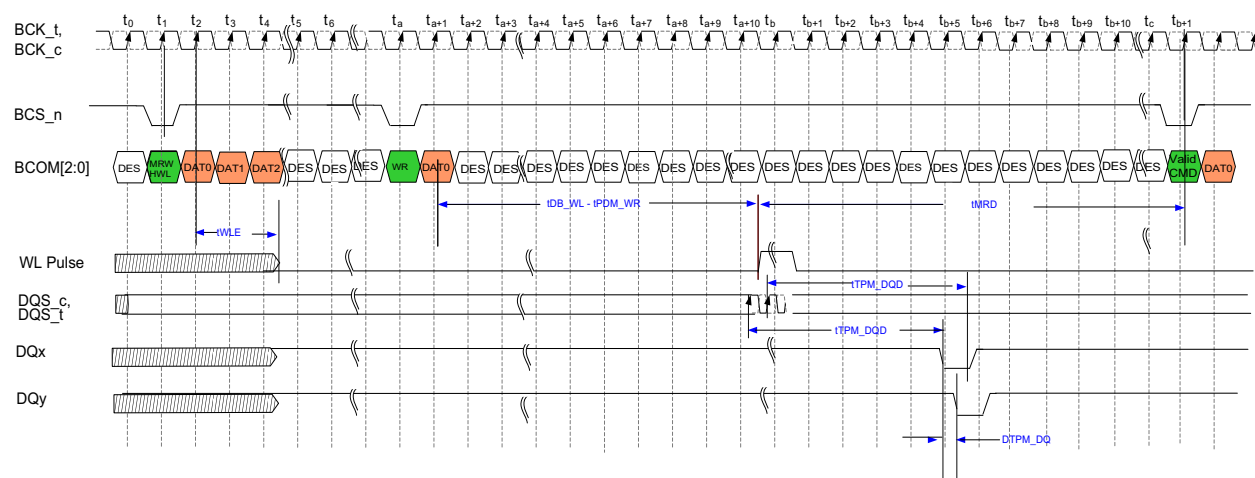
While in HWL training mode, the Data Buffer continuously enables its DQ drivers, and it may disable its DQ receivers. It disables DQ termination DQ\_RTT\_PARK. The Data Buffer disables its DQS drivers, and it must continuously enable its DQS receivers. It applies DQS\_RTT\_PARK continuously on DQS if enabled. The Data Buffer disables its MDQ drivers and receivers, and applies MDQ\_RTT\_PARK if enabled. The Data Buffer disables its MDQS drivers and receivers and applies MDQS\_RTT\_PARK if enabled.

While in HWL training mode, the Data Buffer must continue to process DB-space MRWs normally.

While in HWL training mode, the Host will only send targeted Write commands to the MDB.

When HWL training has been completed, the Host must continue to drive DQS differentially LOW until the MDB has completed HWL mode exit.

In the Mux mode, the Host interface features a single DQS strobe for both PS. The Host DQS delay is the same delay regardless of which PS (PS0, PS1, or both) or rank (rank 0 or rank 1) is being targeted. Data is time multiplexed (even UI for PS0, odd UI for PS1). The MDB in HWL mode will generate an internal WL pulse for the Host that is independent of which PS or rank is being accessed. This means that a write command coming from the Host, targeting PS0-rank0 will produce the same result that a write command targeting PS0-rank1, PS1-rank0 or PS1-rank1 would do. In other words, MDB will internally align cycle and phase for all PS and ranks in each sub-channel. The result of the MDB sampling the internal WL pulse with the Host incoming DQS strobe is used to generate feedback back to the Host on all DQ pins for the corresponding nibble independent of the PS or rank targeted by the Host during this training.



### Figure 83 — Host Write Leveling (HWL)

In HIR mode, the MDB Read Training Pattern is used to provide a data pattern back to the Host to train the read path with the patterns sourced by the MDB. When [PG\[10\]RW\[F1\[1:0\]\] = 00](#), the 8-bit pattern generators are adopted. Otherwise, the 16-bit per-pin pattern generators are adopted. 8-bit pattern mode can be selected in either Rank mode or Mux mode, in which case MDB features two sets of Read Training Pattern registers in [PG\[8\]RW\[E6:E3\]](#) and [PG\[8\]RW\[EC:E9\]](#), one per {R0, R1} or {R2, R3} group in the Rank mode, or one per PS in the Mux mode. 16-bit pattern mode is supported in the Mux mode only, in which case MDB features two sets of Read Training Pattern registers in [PG\[11\]](#) and [PG\[13\]](#), one per PS.

In the Mux mode, since the Host interface runs twice the data rate multiplexing the data for PS0 and PS1. The read pattern sent back to the Host (BL32) is time multiplexed and sourced by each of the PS Read Training Pattern generator. While in HIR mode, the MDB generates the read pattern back to the Host upon receiving read commands. MDB recovers the PS information and toggles the corresponding PS Read Training Pattern generator. If both PS are accessed at the same time, then the MDB will generate a BL32 pattern where even UI (PS0) are fed by PS0 Read

## 8.6 HIR: Host Interface Read Training Mode (cont'd)

Training Pattern generator and odd UI (PS1) are fed by PS1 Read Training Pattern generator. If the read for PS0 and PS1 come at different times, the first PS will drive the pattern from the Read Training Pattern Generator while the second PS will drive high until the second PS starts driving the Read Training Pattern Generator. The behavior is the same as in functional reads with the only difference being where the data is coming from Read Training Pattern Generator instead of DRAM. MDB will match the latency for read operations at the Host interface across PS and ranks, and the Host will see the same timing latency independent of which PS or Rank was targeted with a read command by the Host. The MDB will not receive MRR BCOM commands while in HIR mode, only RD commands on BCOM bus are allowed. Host will either send read commands directly or MRR commands if the MRCD can be set to convert MRR command to RD command on BCOM bus in MRCD [PG\[70\]RW64\[4\]](#). The MRCD will be set to block commands to the DRAM interface.

The Host performs Host-interface read (HIR) training that includes Host read enable alignment and Host read eye sample alignment. This is done in two phases, initial Host read training and final Host read training. For initial Host read training, the Host will use HIR training mode. While in HIR training mode, when MDB receives RD Commands it generates a BL32 read burst to the Host using its internal read training pattern generators. The read burst timing is Rank aligned and constant. The MDQS/MDQ receivers remain disabled during the RD and ODT will operate normally at RTT\_PARK.

For final Host training, the MDB is in its normal operating mode and the Host sends DRAM-space MRRs to the DRAM's read training pattern register. For each DRAM-space MRR, the MDB performs a normal read from the DRAM.

**Table 43 — HIR Training Mode Command Processing Summary**

Command Timing Mode	An RD is Treated as ...	An MRR is Treated as ...
1N/2N	A 1N/2N RD that causes a read from the MDB's read training pattern generator and advances the generator's LFSRs	MRR is not allowed when MDB is in the HIR training mode.

## 8.7 HPA: Host Preamble Training Mode

Host preamble training supports read leveling of the Host receiver timings. Host preamble training changes the read strobe behavior such that the strobes are always driven by the Data Buffer, and only toggle during a 1tHDQS preamble plus the actual burst of the read data. Host Preamble training mode has the same timing requirement to DQS and DQ as the normal Read operation timing when DQ Bus RD CRC is enabled or disabled. There is no toggle during post-amble time. This mode enables the Host to detect the timing of when the first data and associated strobe is returned after a read command.

The Data Buffer enters and exits Host Preamble Training Mode via MRW to [RW83](#).

### 8.7.1 Host Preamble Training Mode Operation

Once the Data Buffer is placed in Host Preamble Training Mode, the only data transactions supported are Read commands. All non-data commands, such as MRW, are still supported in this mode. Once Host Preamble Training is enabled, the device will drive DQS\_t LOW and DQS\_c HIGH within tSDOn and remain at these levels until a Read command is issued.

During Host Preamble Training Mode, the DQS preamble provided during normal operation will not be driven by the Data Buffer. Once the Read command is issued with HIR training mode enabled, the MDB device must drive the DQ pattern as per the Read Training Pattern configuration. Once the Read command is issued with HIR training mode disabled, the MDB device will forward the data from the DRAM interface to the Host interface.

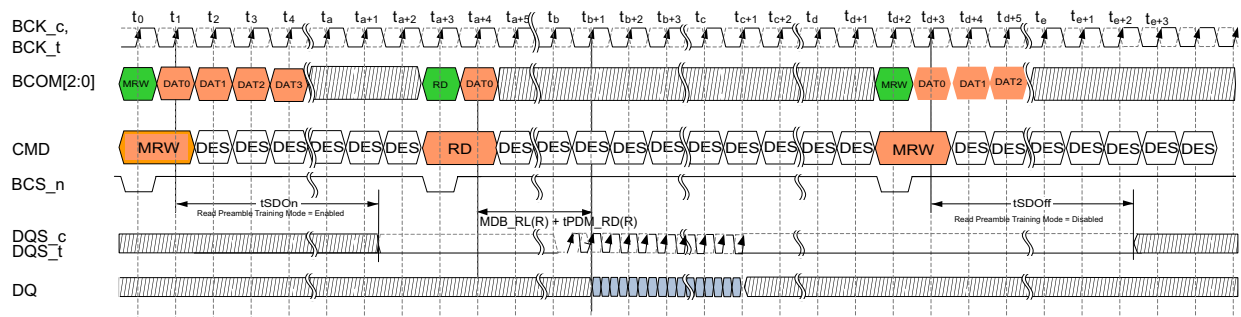


### 8.7.1 Host Preamble Training Mode Operation (cont'd)

The Read commands may be sequenced to enable back-to-back bursts on the DQ bus. While in HPA mode, the Host will not send non-target read commands, because DQS will be driven LOW during idle times.

Host Preamble Training Mode is exited within  $t_{SDOff}$  after setting [RW83](#).

Figure 84 shows the timing for the strobe driven differential LOW after Host Preamble Training Mode is enabled, and also shows the strobe timings including a 1tHDQS Preamble, after a RD command to access the read training pattern:



**Figure 84 — Timing Diagram for Host Preamble Training Mode Entry, Read Training Pattern Access, and Host Preamble Training Mode Exit**

## 8.8 Data Buffer Training Pattern Generator

The MDB contains two sets of training pattern generators to support the HIR, MRD, and MWD training modes. Each set contains two pattern generators. One set is for PS0 in the Mux mode, or Rank 0 and Rank 1 in the Rank mode. The other set is for PS1 in the Mux mode, or Rank 2 and Rank 3 in the Rank mode. Within each set, one pattern generator is used for reads and one pattern generator is used for writes. The read training pattern generator is enabled when the Data Buffer is in HIR, MRD, or MWD training mode. The write training pattern generator is only enabled when the Data Buffer is in MWD training mode. When the Data Buffer in MRD, MWD or HIR mode receives any RD command, it generates a BL16 read burst with the full BL16 data pattern sourced from its read pattern generator. Only a BL16 read burst type is supported. When in MRD or MWD training modes, the read training pattern generator is used to compare to the read data being returned from the DRAM. The write training pattern generator is used to send the write pattern to the DRAM when in MWD training mode.

### 8.8.1 Pattern Control

The read and write training pattern generators support two primary generation format modes. A Serial format and LFSR format. The LFSR format has two secondary pattern options: the LFSR pattern or a high-frequency clock pattern. The format and pattern option are selected via the [PG\[8\]RWE2](#) register as summarized in Table 44.

When a DRAM-space Mode Register Write (MRW) to MR25 occurs, the op-codes are snooped by the Data Buffer and [MR25\[2:0\]](#) are copied into the DB-space register [PG\[8\]RWE2](#). This register is reset to its default values during power-up initialization, Reset initialization with Stable Power, and MDB reset. In addition to configuring the read training pattern format for HIR training mode, this register also configures the pattern format for the pattern checker used for MRD training mode and the read phase of MWD training mode, and the pattern generator used for the write phase of MWD.

Note: In Table 44, the “PS0” and “PS1” descriptions refer to the usage in the Mux mode. In the Rank mode, the “PS0” related settings refer to Rank 0 and Rank 1, and the “PS1” related settings refer to Rank 2 and Rank 3.



## 8.8.1 Pattern Control (cont'd)

Table 44 — Read Training Mode Settings

Data Buffer RW	Operating Mode	Bit Description	Snoop Value from DRAM MRW
PG[8]RWE2[0]	PS0 Read Training Pattern Format	0 = Serial (default), 1 = LFSR	MR25[0]
PG[8]RWE2[1]	PS0 LFSR0 Pattern Option	0 = LFSR (default), 1 = Clock	MR25[1]
PG[8]RWE2[2]	PS0 LFSR1 Pattern Option	0 = LFSR (default), 1 = Clock	MR25[2]
PG[8]RWE2[3]	Reserved	Reserved	NA
PG[8]RWE2[4]	PS1 Read Training Pattern Format	0 = Serial (default), 1 = LFSR	MR25[0]
PG[8]RWE2[5]	PS1 LFSR0 Pattern Option	0 = LFSR (default), 1 = Clock	MR25[1]
PG[8]RWE2[6]	PS1 LFSR1 Pattern Option	0 = LFSR (default), 1 = Clock	MR25[2]
PG[8]RWE2[7]	Reserved	Reserved	NA
PG[8]RWE3[7:0]	PS0 Read Pattern_0 <sup>1</sup>	Serial Data_0: UI[7:0] LFSR Seed_0: UI[7:0] Default: 0x5A	MR26[7:0]
PG[8]RWE4[7:0]	PS0 Read Pattern_1 <sup>2</sup>	Serial Data_1: UI[15:8] LFSR Seed_1: UI[7:0] Default: 0x3C	MR27[7:0]
PG[8]RWE5[7:0]	PS0 Read Pattern Invert <sup>3</sup>	0= DQ[x] is not inverted 1= DQ[x] is inverted Default: 0x00	MR28[3:0] <sup>4</sup> in DRAM interface x4 configuration, or MR28[7:0] in DRAM interface x8 configuration
PG[8]RWE6[7:0]	PS0 Read LFSR Assignment <sup>3</sup>	[x] = 0, DQ[x] is sourced from LFSR0 [x] = 1, DQ[x] is sourced from LFSR1 Default: 0xEE in either DRAM interface x4 or x8 configuration	MR30[3:0] <sup>4</sup> in DRAM interface x4 configuration, or MR30[7:0] in DRAM interface x8 configuration
PG[8]RWE9[7:0]	PS1 Read Pattern_0 <sup>5</sup>	Serial Data_0: UI[7:0] LFSR Seed_0: UI[7:0] Default: 0x5A	MR26[7:0]
PG[8]RWEA[7:0]	PS1 Read Pattern_1 <sup>6</sup>	Serial Data_1: UI[15:8] LFSR Seed_1: UI[7:0] Default: 0x3C	MR27[7:0]

Table 44 — Read Training Mode Settings (cont'd)

Data Buffer RW	Operating Mode	Bit Description	Snoop Value from DRAM MRW
PG[8]RWEB[7:0]	PS1 Read Pattern Invert <sup>7</sup>	0= DQ[x] is not inverted 1= DQ[x] is inverted Default: 0x00	MR28[3:0] <sup>8</sup> in DRAM interface x4 configuration, or MR28[7:0] in DRAM interface x8 configuration
PG[8]RVEC[7:0]	PS1 Read LFSR Assignment <sup>3</sup>	[x] = 0, DQ[x] is sourced from LFSR0 [x] = 1, DQ[x] is sourced from LFSR1 Default: 0xEE in either DRAM interface x4 or x8 configuration	MR30[3:0] <sup>4</sup> in DRAM interface x4 configuration, or MR30[7:0] in DRAM interface x8 configuration
RW9C[7:0]	PS0 READ LFSR0 State Monitor (Read Only)	The current state of READ LFSR0	N/A
RW9D[7:0]	PS0 READ LFSR1 State Monitor (Read Only)	The current state of READ LFSR1	N/A
RW9E[7:0]	PS0 WRITE LFSR0 State Monitor (Read Only)	The current state of WRITE LFSR0	N/A
RW9F[7:0]	PS0 WRITE LFSR1 State Monitor (Read Only)	The current state of WRITE LFSR1	N/A
PG[70]RVEC[7:0]	PS1 READ LFSR0 State Monitor (Read Only)	The current state of READ LFSR0	N/A
PG[70]RWED[7:0]	PS1 READ LFSR1 State Monitor (Read Only)	The current state of READ LFSR1	N/A
PG[70]RWEE[7:0]	PS1 WRITE LFSR0 State Monitor (Read Only)	The current state of WRITE LFSR0	N/A
PG[70]RWEF[7:0]	PS1 WRITE LFSR1 State Monitor (Read Only)	The current state of WRITE LFSR1	N/A

NOTE 1 The WRITE LFSR0 and READ LFSR0 are initialized with the same seed value of Read Pattern\_0.

NOTE 2 The WRITE LFSR1 and READ LFSR1 are initialized with the same seed value of Read Pattern\_1.

NOTE 3 Upper/lower nibble can be written with different code only by direct MRW, and DRAMs need to be configured in PDA mode to support this case.

NOTE 4 This value gets copied to 7:4 and 3:0

NOTE 5 The WRITE LFSR0 and READ LFSR0 are initialized with the same seed value of Read Pattern\_0.

NOTE 6 The WRITE LFSR1 and READ LFSR1 are initialized with the same seed value of Read Pattern\_1.

NOTE 7 Upper/lower nibble can be written with different code only by direct MRW, and DRAMs need to be configured in PDA mode to support this case.

NOTE 8 This value gets copied to 7:4 and 3:0

There are two 8-bit pattern generation LFSRs per PS in the Mux mode or per two ranks in the Rank mode provided for LFSR pattern generation, LFSR0 and LFSR1. Associated with each LFSR is a clock pattern generator, this can be implemented as a single, shared clock-pattern generator.

### 8.8.1 Pattern Control (cont'd)

For LFSR format and the LFSR pattern selected for a particular LFSR, when an RD with the MDB in MRR, MRD or HIR occurs, the LFSR changes state. For LFSR format and the clock pattern option selected for a particular LFSR, when a RD with the MDB in MRR, MRD or HIR occurs, the LFSR holds its state and the clock pattern generator generates the clock pattern.

Two registers are provided to allow the Host to specify the 16-bit fixed pattern for serial format, or the two 8-bit seed values for LFSR format. The [PG\[8\]RW\[E3,E9\]](#) register provides UI[7:0] of the 16-bit fixed pattern for serial format, or UI[7:0] of LFSR0's 8-bit seed value for LFSR format. This register defaults to 0x5A, and can be written to any value by the Host. The [PG\[8\]RW\[E4,EA\]](#) register provides UI[15:8] of the 16-bit fixed pattern for serial format, or UI[7:0] of LFSR1's 8-bit seed value for LFSR format. This register defaults to 0x3C and can be written to any value by the Host.

These two registers are reset to their default values under the following conditions:

- Power-up initialization and Reset initialization with Stable Power
- BRST\_n assertion, when BCOM is '000' or '111'
- Self Refresh with and without Clock Stop

In addition to configuring [PG\[8\]RW\[EA:E9,E4:E3\]](#) for HIR training mode, these registers can also be configured as the pattern/seed for the pattern checker used for MRD training mode, the read phase of MWD training mode, and the pattern generator used for the write phase of MWD.

When a DRAM-space MRW to MR26 occurs, it is snooped by the MDB and [PG\[8\]RW\[E9,E3\]](#) is loaded with MR26[7:0].

When a DRAM-space MRW to MR27 occurs, it is snooped by the MDB and [PG\[8\]RW\[EA,E4\]](#) is loaded with MR27[7:0].

The [PG\[8\]RW\[EB,E5\]](#) register is provided to allow the Host to select per-DQ pattern inversion that is applied for either serial format or LFSR format. If [PG\[8\]RW\[EB,E5\]\[x\] = 0](#) the pattern applied to DQ[x] is not inverted, otherwise if [PG\[8\]RW\[EB,E5\]\[x\] = 1](#) then the pattern applied to DQ[x] is inverted. This register defaults to 0x00, and it is reset to its default value under the following conditions:

- Power-up initialization and Reset initialization with Stable Power
- BRST\_n assertion, when BCOM is '000' or '111'
- Self Refresh with and without Clock Stop

In addition to configuring the per-DQ pattern inversion for HIR training mode, this register also configures the per-DQ pattern inversion for the pattern checker used for MRD training mode and the read phase of MWD training mode, and the pattern generator used for the write phase of MWD.

When a DRAM-space MRW to MR28 occurs, it is snooped by the MDB. [PG70RWE4\[4:3\]](#) are used to select PS1/PS0. When the DRAM is a x4 device, then only MR28[3:0] is valid. All DRAM are programmed with the same value. So, when MR28 is snooped, [PG\[8\]RWE5](#) is loaded with {MR28[3:0], MR28[3:0]}. If DRAM is a x8 device then MR28[7:0] is valid. All DRAM are programmed with the same value. So, when MR28 is snooped, [PG\[8\]RWE5](#) is loaded with MR28[7:0].

## 8.8.2 LFSR Functionality and Control

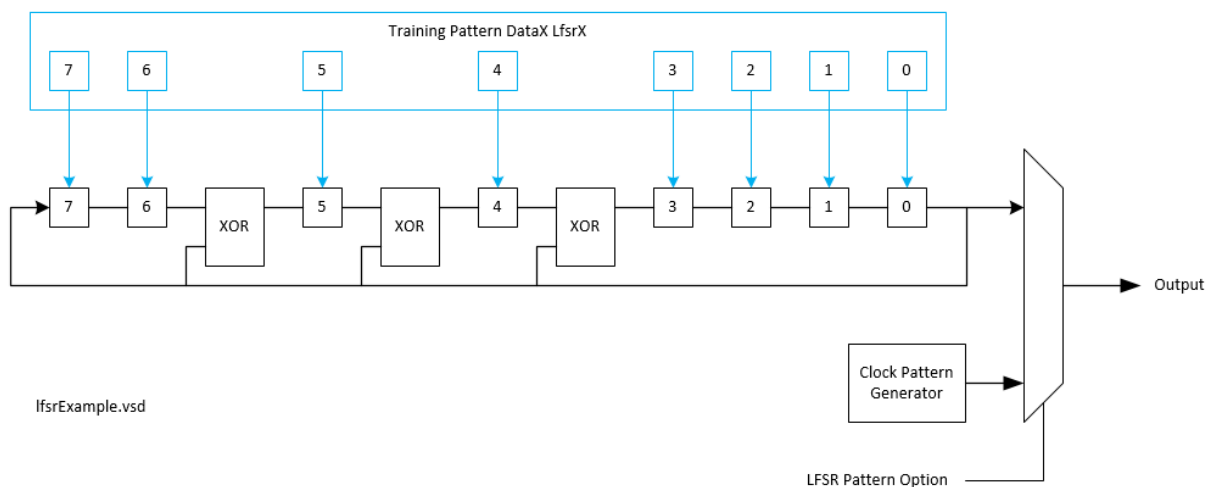
LFSR is performed on a PS basis in the Mux mode, or independently between the {R0, R1} and {R2, R3} groups in the Rank mode. The following describes PS0 or {R0, R1} group implementation.

Figure 85 shows an example LFSR topology with its associated clock pattern generator. Each LFSR is an 8-bit Galois LFSR with polynomial  $x^8 + x^6 + x^5 + x^4 + 1$ . The numbered shifter stages of each LFSR are mapped 1:1 with the bit numbers of its respective pattern/seed register. The output of each LFSR can be assigned to any number of DQ outputs. The PG[8]RWE6 register allows the Host to select the per-DQ assignment between the two LFSRs. This register defaults to 0xEE, and it is reset to its default value under the following conditions:

- Power-up initialization and Reset initialization with Stable Power
- BRST\_n assertion when BCOM is '000' or '111'
- Self Refresh with and without Clock Stop

In addition to configuring the per-DQ pattern assignment for HIR training mode, this register also configures the per-DQ assignment for the pattern checker used for MRD training mode, the read phase of MWD training mode, and the pattern generator used for the write phase of MWD.

When a DRAM-space MRW to MR30 occurs, it is snooped by the MDB. When the DRAM is a x4 device, only MR30[3:0] is valid. All DRAM are programmed with the same value. So, when MR30 is snooped, PG[8]RWE6[7:0] is loaded with {MR30[3:0], MR30[3:0]}. When the DRAM is a x8 device, MR30[7:0] is valid. All DRAM are programmed with the same value. So, when MR30 is snooped, PG[8]RWE6[7:0] is loaded with MR30[7:0].



**Figure 85 — Example LFSR Topology**

Each LFSR is enabled for pattern generation (i.e. next-state computation) only when LFSR format is selected and its LFSR pattern option is selected. Each LFSR is seeded to a new state whenever its respective pattern/seed register PG[8]RW[E4:E3] is written via a DB-space MRW. It is also seeded with the default value of its respective pattern/seed register whenever the reset condition for its respective pattern/seed register occurs (i.e. during power-up initialization, reset initialization with stable power, MDB reset, and Self-Refresh).

Each LFSR operates at the UI rate and produces a new output value each UI. Each LFSR only changes state when generating a data burst for a RD with MDB in MRD, MWR or HIR mode. During idle times, each LFSR retains its state from the end of the data burst of the previous RD with MDB in MRD, MWR or HIR mode.

### 8.8.2 LFSR Functionality and Control (cont'd)

Since the data burst for each RD with MDB in MRD, MWR, or HIR mode is 16-bits, each LFSR will complete its full sequence after 16 consecutive RDs with MDB in MRD, MWR or HIR mode. When an LFSR is seeded with 0x00 the LFSR will produce a constant zero pattern.

The state of LFSR0 will not change when a RD with MDB in MRD, MWR, or HIR mode occurs if its respective clock pattern option is selected. Instead, the clock-pattern generator changes state. The clock pattern is sent only to the DQ signals whose corresponding assignment bit is set to zero. The first UI of the clock pattern will have a value of zero, the second UI will have a value of one, and this toggle pattern will continue for each subsequent UI of the burst.

The state of LFSR1 will not change when a RD with MDB in MRD, MWR, or HIR mode occurs if its respective clock pattern option is selected. Instead, the clock-pattern generator changes state. The clock pattern is sent only to the DQ signals whose corresponding assignment bit is set to one. The first UI of the clock pattern will have a value of zero, the second UI will have a value of one, and this toggle pattern will continue for subsequent UI of the burst.

An LFSR changes state for each RD with MDB in MRD, MWR, or HIR mode received only when LFSR format is selected and its respective LFSR pattern option is selected. The assignment settings have no impact on whether an LFSR state changes for each RD with MDB in MRD, MWR or HIR mode received.

In addition to pattern generation during HIR training mode, LFSR0 and LFSR1 are used for pattern checking during MRD training mode and the read phase of MWD training mode.

The state of LFSR0 can be monitored via a DB-space MRR to read-only register [RW9E](#) and [RW9C](#), and the state of LFSR1 can be monitored via a DB-space MRR to read-only register [RW9F](#) and [RW9D](#). HIR training mode must be exited prior to reading these registers. HIR training mode exit and re-entry does not change the state of LFSR0 and LFSR1.

In addition to providing monitoring of LFSR0 and LFSR1 for HIR training mode, these registers also provide monitoring of LFSR0 and LFSR1 when used for the pattern checking during MRD training mode and the read phase of MWD training mode.

### 8.8.3 Pattern Generation Examples

The following examples cover various read training pattern generator use cases. Table 45 shows an example of serial format usage, Table 48 shows an example of LFSR format usage and Table 51 shows an example of LFSR format with 0x00 seed and clock usage.

#### 8.8.3.1 Serial Format Example

**Table 45 — PS0 or {R0, R1} Group Serial Format Example Settings**

Data Buffer RW	Operating Mode	Setting
<a href="#">PG[8]RWE2[0]</a>	Read Training Pattern Format	0
<a href="#">PG[8]RWE2[1]</a>	LFSR0 Pattern Option	0
<a href="#">PG[8]RWE2[2]</a>	LFSR1 Pattern Option	0
<a href="#">PG[8]RWE3[7:0]</a>	Read Pattern_0	0x1C
<a href="#">PG[8]RWE4[7:0]</a>	Read Pattern_1	0x59
<a href="#">PG[8]RWE5[7:0]</a>	Read Pattern Invert	0x55

## 8.8.3.1 Serial Format Example (cont'd)

Table 46 — Base Pattern

Base Pattern															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

Table 47 — Serial Format Pattern Example

DQ	Invert	UI															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
1	0	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
2	1	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
3	0	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
4	1	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
5	0	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0
6	1	1	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1
7	0	0	1	0	1	1	0	0	1	0	0	0	1	1	1	0	0

## 8.8.3.2 LFSR Format with LFSR Pattern Example

Table 48 — PS0 or {R0, R1} Group LFSR Format with LRSR Pattern Example Settings

Data Buffer RW	Operating Mode	Setting
PG[8]RWE2[0]	Read Training Pattern Format	1
PG[8]RWE2[1]	LFSR0 Pattern Option	0
PG[8]RWE2[2]	LFSR1 Pattern Option	0
PG[8]RWE3[7:0]	Read Pattern_0	0x5A
PG[8]RWE4[7:0]	Read Pattern_1	0x3C
PG[8]RWE5[7:0]	Read Pattern Invert	0xF0
PG[8]RWE6[7:0]	Read LFSR Assignment	0xFE

Table 49 — Seed Pattern

Seed Pattern															
LFSR1								LFSR0							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	1	1	0	0	0	1	0	1	1	0	1	0



8.8.3.3 LFSR Format with Clock Pattern Example (cont'd)

Table 53 — LFSR Format with Clock Pattern Example

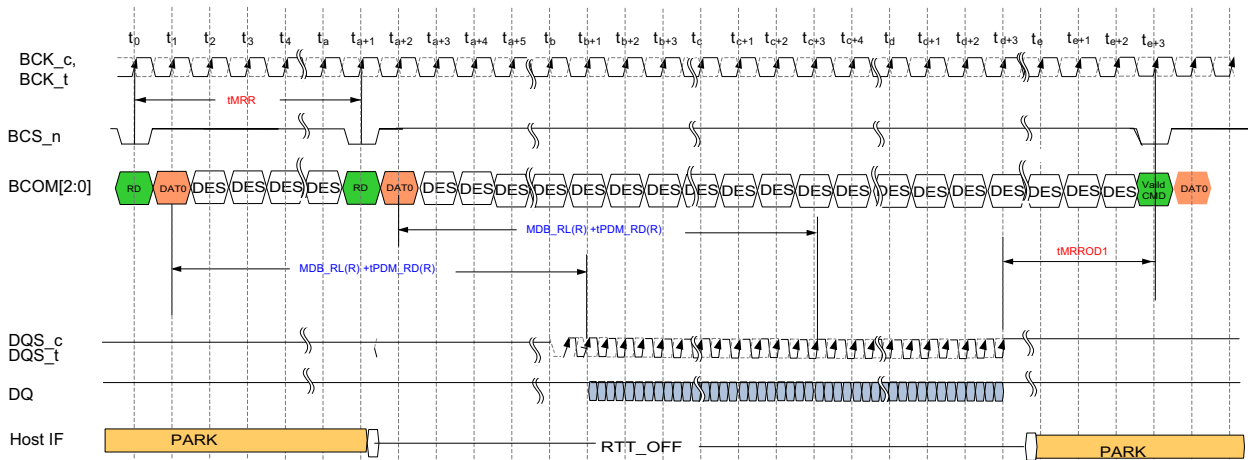
DQ	Invert	LFSR	UI															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
3	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
4	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
7	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.8.4 Timing

Figure 86 shows an example of two back-to-back Read commands in the Mux mode that are separated by  $t_{MRR} = 8$  BCK cycles.

While in HIR mode, when a MDB receives any Read Command with a 1tBCK BCS\_n assertion (target) it generates a BL32 read burst with the full BL16 data pattern sourced from its read pattern generator and the other BL16 of “1”. The read burst timing is aligned for any PS or Rank access in the RD sequence. The read latency for rank-x and nibble-y is  $DB\_RL(Rx, Ny) + t_{PDM\_RD}$  after the DAT0 cycle of the RD sequence.

In the Rank mode, as described in the normal operating section, the DQS/DQ data rate will be half of the signals shown in the figure. The MDB will generate a BL16 read burst for each RD command, but the read burst timing is also aligned for any Rank access.





## 8.9 MDQ Read Error Counter

The Data Buffer supports an error counter per bit that provides per UI to support error counting during MRD training and read phase of MWD training. The error counters are enabled when MRD mode or MWD mode is entered. Both PS0 and PS1 error counters in Mux mode, or all ranks error counters in Rank mode can be reset through [PG\[7\]RWF0\[0\]](#).

Each Error counter register is restored to the default value under the following conditions:

- Power-up initialization and Reset initialization with Stable Power
- Normal Reset during normal operation. BRST\_n assertion and BCOM[2:0]= 000 or BCOM[2:0]= 111
- Self Refresh with and without Clock Stop
- Reset event through [PG\[7\]RWF0\[0\]](#).

However, it is not reset as a result of MRD/MWD mode entry and exit.

When enabled, each error counter counts bit errors for its respective bit lane during each read burst that is a result of a RD during MRD or MWD training mode. Each error counter holds its value during idle periods. If an error counter reaches its maximum error counter at any time, it will hold its maximum value until reset.

Each error counter is 16 bits wide. Its current error count value can be read at any time via DB-space MRRs to its lower- and upper-byte registers that contain the lower and upper bytes, respectively, of its 16-bit value (MRD/MWD mode would first need to be exited). The error count value registers are [PG\[74,7\]RW\[EF:E0\]](#). [PG\[7\]RW\[EF:E0\]](#) are used for PS0 error counters in the Mux mode, or Rank 0 and Rank 1 error counters in the Rank mode. [PG\[74\]RW\[EF:E0\]](#) are used for PS1 error counters in the Mux mode, or Rank 2 and Rank 3 error counters in the Rank mode.

## 8.10 Back-Side Receiver Matching

DDR5MDB02 can be designed with unmatched back-side receivers, where the internal MDQS delay is longer than that of MDQ, or matched receivers, where the delays are approximately the same. The DRAM Interface Receiver Type read-only register bit ([PG\[70\]RWE1](#)) can be read by the Host to determine the vendor specific configuration that is supported.

The Read Delay control words ([PG\[00,01,72,73\]RW\[E5:E4\]](#)) are used to adjust the internal MDQS delay during MRD training such that MDQ is captured by MDQS in the middle of the UI. At the default setting, 7'h00, these control words will delay MDQS by the typical amount corresponding to the receiver type. For matched receivers, this is  $\frac{1}{4}t_{BCK}$ . For unmatched receivers, this is  $(1 + \frac{1}{4})t_{BCK}$ . For matched receivers, only the lower 5 bits of the Read Delay control words are used, for a total adjustment range of  $\sim\frac{1}{2}t_{BCK}$ . For unmatched receivers, a wider variation of internal MDQS delay is possible, so 7 bits of adjustment are available, for a total adjustment range of  $\sim(1 + \frac{1}{4})t_{BCK}$ . In the unmatched case, the Host may adjust the MR40 Read DQS Offset in the DRAMs to pre-launch MDQS in order to facilitate MRD training convergence.

## 8.11 CRC Pin Training Mode

The CRC pin training mode, as defined in [PG\[70\]RWE0\[5\]](#), enables the DQS1\_t/c pins functioning as the CRC pin to be trained in a similar way as the DQ pins. During training of the Host interface DQ pins, data can be written and read to/from the DRAM via the corresponding MDQ pins. The DQS1\_t/c pins do not have a mapped path to the DRAM for storage of data. In the case where DQS1\_t/c is being used for CRC functionality, the CRC pin training mode will map a path between the DQS1\_t/c pins to a DRAM DQ via the corresponding MDQ4 pin.

The CRC pin training mode applies to both sub-channels and pseudo-channels within a sub-channel. During CRC pin training mode, there is no CRC calculation for both WR and RD directions. WR CRC must be disabled in [PG\[70\]RWE0\[3\]](#) while in this training mode. RD CRC can be either enabled or disabled by setting [PG\[70\]RWE0\[2\]](#) properly based on the application need.

## 8.11 CRC Pin Training Mode (cont'd)

When RD CRC is enabled, the extra read latency including  $t_{Calc\_CRC\_RD}$  is included to the DQ and DQS1 lanes when RD is issued and data is sent back to the Host. When RD CRC is disabled, there is no extra read latency to the DQ and DQS1 lanes when RD is issued and data is sent back to the Host.

When the CRC pin training mode is enabled, all logical functionality between MDQ4 and DQ4 will be mapped to the DQS1\_t/c pins instead of DQ4. All timing, voltage and equalization control capabilities of the DQS1\_t/c pair are the same as a DQ pin and will remain independent of DQ4.

Write operation:

- DQS1\_t/c Rx will transfer data to MDQ4 Tx
- DQ4 Rx is active but does not transfer data to MDQ4 Tx

Read operation:

- MDQ4 Rx will transfer data to DQS1\_t/c Tx
- DQ4 Tx data will be a duplicate of DQ6 Tx data

## 8.12 Enhanced Training Modes

In Mux mode only with higher speed bins and additional CRC data lanes, the DDR5MDB supports Enhanced Read Training Mode (ERTM) [RW83\[6\]](#) and Enhanced Write Training Mode (EWTM) [RW83\[5\]](#). These two training modes are independent and will support write or read training for the DQs and CRC lanes when CRC is enabled.

- **Enhanced Read Training Mode (ERTM)** - This training mode allows Host pattern comparison between internal LFSR and MDB generated LFSR.
- **Enhanced Write Training Mode (EWTM)** - This training mode allows MDB pattern comparison between internal LFSR and Host generated LFSR and update the Error log control words within  $t_{MRD\_L}$ .

In addition to ERTM and EWTM modes, the DDR5MDB supports a Host Interface Write training mode (HIW) located in [RW83\[3:0\]](#) in Mux mode only, not in Rank mode, to enable periodic training and margining of the Host interface without disturbing the contents in the DRAM. These training modes can be combined with other legacy Host Interface training modes to train the DQs and CRC lanes.

Note: HPA is intended for DQS Read leveling training, which is independent of DQ or CRC lane calibration. Therefore, HPA can be enabled or disabled for any of the DQS as CRC Read Direction configurations. HPA only applies to the non-CRC strobe.

### 8.12.1 Training Pattern Generation

To support higher frequency operation, each DQ lane and the CRC lane will have the option to support unique pattern configuration. The pattern options will be 16-bit serial repeating pattern or a 16-bit LFSR seeded pattern per DQ lane and for the CRC lane with [PG\[10\]RWF1\[1:0\]](#) configured to 01 or 10 values. These programmable patterns in [PG\[11\]](#) and [PG\[13\]](#) are to be used for either the comparison during HIW and EWTM or will be used to generate the patterns during HIR and ERTM. The polynomial for the 16-bit LFSR is shown in Figure 87.

These LFSR Seed and Status registers in [PG\[14:11\]](#) are reset to their default values under the following conditions:

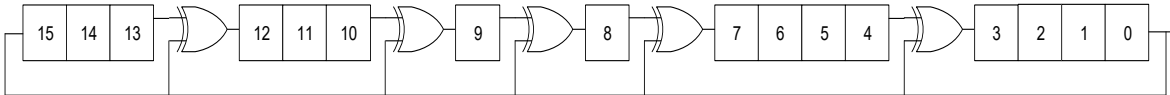
- Power-up initialization and Reset initialization with Stable Power
- BRST\_n assertion, when BCOM is '000' or '111'

Each LFSR is seeded to a new state whenever its respective pattern/seed register is written via MDB-space MRW.

### 8.12.1.1 Galois LFSR

Figure 87 shows the 16-bit LFSR topology to be used by the Memory Controller and MDB hardware for all Host Interface Training requiring a pattern including DFE.

Note: The legacy 8-bit LFSR will only be used for DRAM interface training and HIR training.



**Figure 87 — Galois LFSR:  $X^{16} + X^{13} + X^{10} + X^9 + X^8 + X^4 + 1$**

Note: The diagram in Figure 87 is the ordering of the bits that are used for Training Pattern Comparison and Error Counting.

### 8.12.2 Enhanced Read Training

Enhanced Read Training allows the Host controller to train the Read direction path, MDB to Host Interface with or without CRC enabled. Any other configuration not included in Table 54 is not supported.

### 8.12.2.1 Read Direction Configurations

**Table 54 — Supported Read Direction Configurations**

Interface	Active Lanes	HIR	ERTM	RD CRC in PG[70]RWE0[2]	DQ Source	CRC Lane Source	Pattern Compare	Notes
Host Interface ( <i>Dram Interface Not involved</i> )	DQ[7:0] and CRC lane	Enabled	Enabled	Enabled with extra tCRC_Calc_RD latency	MDB Pattern Gen	MDB Pattern Gen	Host	1,4
	DQ[7:0] and CRC lane	Enabled	Enabled	Disabled without extra tCRC_Calc_RD latency	MDB Pattern Gen	MDB Pattern Gen	Host	1,4
	DQ[7:0] only	Enabled	Disabled	Disabled without extra tCRC_Calc_RD latency	MDB Pattern Gen	CRC (DQS_t/c) Disabled	Host	2, 3,4
Host and DRAM Interfaces ( <i>MDB forwards Read Data from DRAM</i> )	DQ[7:0] and CRC lane	Disabled	Enabled	Enabled with extra tCRC_Calc_RD latency	DRAM	MDB Pattern Gen	Host	4, 5, 6, 8
	DQ[7:0] and CRC lane	Disabled	Enabled	Disabled without extra tCRC_Calc_RD latency	DRAM	MDB Pattern Gen	Host	4, 5, 6, 8
	DQ[7:0] and CRC lane	Disabled	Disabled	Extra tCRC_Calc_RD latency if Enabled	DRAM	MDB CRC Calculated (if CRC lane enabled)	N/A, CRC calculated by Host	4,7,8

NOTE 1 The MDB will generate DQ[7:0] and CRC Read data based on the Read pattern configuration LFSR or simple fixed pattern.

NOTE 2 The MDB will generate DQ[7:0] based on the Read pattern configuration LFSR or simple fixed pattern.

NOTE 3 No read data expected on CRC Lane.

NOTE 4 DQ[7:0] READ patterns are compared within the Host.

NOTE 5 The Host writes to DRAM or DRAM generates DQ[7:0] based on the Read pattern configuration LFSR or simple fixed pattern.

NOTE 6 MDB generates CRC lane.

NOTE 7 Normal Operation with or without CRC enabled.

NOTE 8 DRAM DQ source data can come from DRAM Array or DRAM pattern generator.

When in HIR and/or ERTM training modes are enabled, the MDB or DRAM will generate Read data on all DQ[7:0] and CRC lane if enabled. The Host will be responsible for pattern comparison and error tracking.

### 8.12.3 Enhanced Write Training

Enhanced Write Training allows the Host controller to train the Write direction path, Host to MDB Interface with or without CRC enabled. Any other configuration not included in Table 55 is not supported.

### 8.12.3.1 Write Direction Configurations

**Table 55 — Supported Write Direction Configurations**

Intrface	Active Lanes	HIW	EWTM	RD CRC in PG[70]RWE0[2]	DQ Source	CRC Lane Source	Pattern Compare	Notes
Host Interface (MDB does not forward Write Data to DRAM)	DQ[7:0] and CRC lane	Enabled	Enabled	Enabled with extra tCRC_Calc_RD latency	Host Pattern Gen	Host Pattern Gen	MDB	1, 2, 3, 6, 8, 11
	DQ[7:0] and CRC lane	Enabled	Enabled	Disabled without extra tCRC_Calc_RD latency	Host Pattern Gen	Host Pattern Gen	MDB	1, 2, 3, 6, 8, 11
	DQ[7:0]	Enabled	Disabled	Disabled without extra tCRC_Calc_RD latency	Host Pattern Gen	Disabled	MDB	1, 3, 4, 6, 12
	DQ[7:0]	Enabled	Disabled	Enabled with extra tCRC_Calc_RD latency	Host Pattern Gen	Disabled	MDB	1, 3, 4, 6, 12
Host and DRAM Interfaces (MDB forwards Write Data to DRAM)	DQ[7:0] and CRC lane	Disabled	Enabled	Enabled with extra tCRC_Calc_RD latency	Host	Host Pattern Gen	MDB Compared CRC lane data only	1, 2, 5, 6, 7, 8
	DQ[7:0] and CRC lane	Disabled	Enabled	Disabled without extra tCRC_Calc_RD latency	Host	Host Pattern Gen	MDB Compared CRC lane data only	1, 2, 5, 6, 7, 8
	DQ[7:0] and CRC lane	Disabled	Disabled	Refer to the Read Direction Table 54 for any read operations	Host	Host Calculated (if CRC lane is enabled)	N/A, CRC calculated by MDB	5, 7, 9, 10

NOTE 1 MRRs to PG[10]RW[E3:E0] will return the content of MDB Error Counter Status.

NOTE 2 The Host will generate LFSR or Simple fixed pattern on DQ[7:0] and the CRC lane write data based on write pattern configuration.

NOTE 3 DQ[7:0] Write patterns are compared within the MDB.

NOTE 4 The Host will generate LFSR or Simple fixed pattern on DQ[7:0] write data based on write pattern configuration.

NOTE 5 A BCOM Read command will return DQ[7:0] data from DRAM to the Host.

NOTE 6 MRRs to PG[10]RW[EE:EA] with return MDB DQ and CRC UI Phase Error Status registers.

NOTE 7 DQ[7:0] data is written to DRAM.

NOTE 8 CRC lane Write patterns are compared within the MDB. When a BCOM Read command is received, the MDB will send back the UI phase error status on the CRC lane.

NOTE 9 The Host will generate DQ[7:0] Write data and calculated CRC for Write data.

NOTE 10 CRC Write data is compared against calculated CRC within the MDB during Writes.

NOTE 11 When a BCOM Read command is received with HIW enabled, each DQ will send back its own UI phase error status using format in Table 57.

NOTE 12 When a BCOM Read command is received with HIW enabled, each DQ lane will send back its own UI phase error status using format in Table 57. The CRC lane output will be disabled in x8 mode or the CRC lane output will be normal DQS strobe in x4 mode.

8.12.3.1 Write Direction Configurations (cont'd)

When in HIW and/or EWTM training modes are enabled, the Host will send Write data on all DQ[7:0] and CRC lane if enabled. The MDB will compare the Write data to each expected pattern for each DQ lane and CRC lane if enabled. The errors will be counted per lane and per UI. The error counter support up to 32 bits and counts the total UI errors across all DQ and CRC lanes. Any of the DQs or the CRC lane can be masked during training and is done by the Host setting the appropriated bits in PG[10]RWF4 for DQ lanes and/or PG[10]RWF5 for the CRC lane. The Error Detect Threshold in PG[10]RWF3 can be set by the Host prior to training to set the criteria for the UI Phase Error Status registers PG[10]RW[EE:EA]. The Host can read the 32 bits error counter values by issuing MRRs to Host Interface Error Counter Status Registers located in PG[10]RW[E3:E0]. The Host can clear the status registers by setting PG[10]RWF0[0] =1.

To allow the Host to isolate failing pins or UIs, the MDB allows the Host to mask off selected DQ and/or CRC lane from the Error Counter Registers in PG[10]RW[E3:E0]. The MDB also allows the Host to mask off selected UI per PS channel from the UI Phase Error Status registers PG[10]RW[EE:EA] and Error Counter Registers PG[10]RW[E3:E0] with the settings in PG[10]RW[FB:F8].

The MDB will error track the UI errors on a per group basis. The groups are divided up into four phases which contain 32 UI total. A Phase Error is an error in one of 4 rotating phases shown in Figure 88 and the status can be read from MRR to PG[10]RW[EE:EA] or on the DQ bus with Read Command. The Host can clear the status registers by setting PG[10]RWF0[1] =1.

Table 56 — Phase Error

Phase	Tracked UIs
Phase 0	UI0  UI4  UI8  UI12  UI16  UI20  UI24  UI28
Phase 1	UI1  UI5  UI9  UI13  UI17  UI21  UI25  UI29
Phase 2	UI2  UI6  UI10  UI14  UI18  UI22  UI26  UI30
Phase 3	UI3  UI7  UI11  UI15  UI19  UI23  UI27  UI31

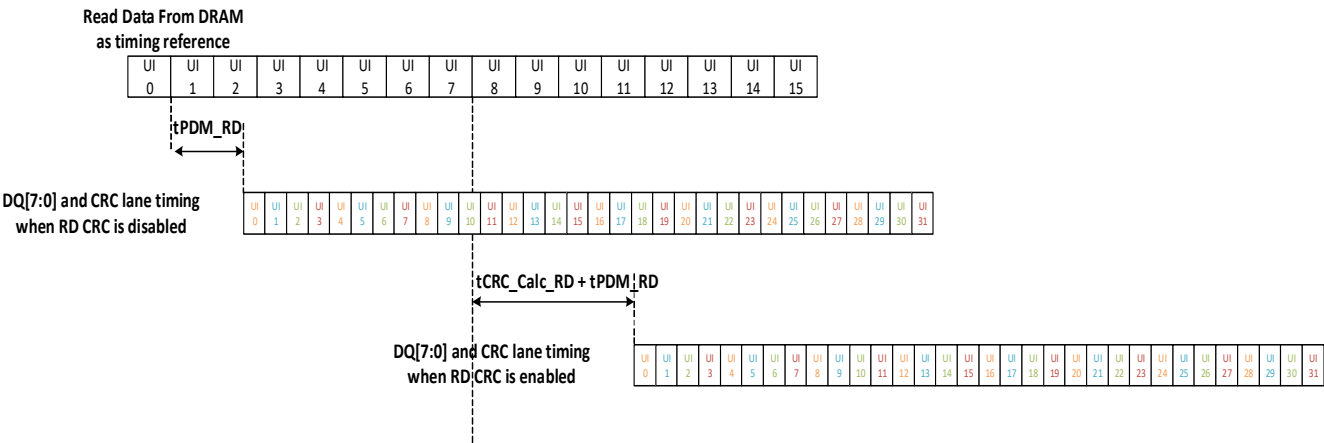


Figure 88 — 4 Phase Example

### 8.12.3.1 Write Direction Configurations (cont'd)

**Table 57 — READ Command Format for DQ and CRC Lane Phase Return<sup>1</sup>**

Serial	UI 0-7	UI 8	UI 9	UI 10	UI 11	UI 12 - 15
DQ0	0	Phase 0 PG[10]RW EB[0]	Phase 1 PG[10]RW EB[1]	Phase 2 PG[10]RW EB[2]	Phase 3 PG[10]RW EB[3]	0
DQ1	1	Phase 0 !PG[10]RW EB[4]	Phase 1 !PG[10]RW EB[5]	Phase 2 !PG[10]RW EB[6]	Phase 3 !PG[10]RW EB[7]	1
DQ2	0	Phase 0 PG[10]RW EC[0]	Phase 1 PG[10]RW EC[1]	Phase 2 PG[10]RW EC[2]	Phase 3 PG[10]RW EC[3]	0
DQ3	1	Phase 0 !PG[10]RW EC[4]	Phase 1 !PG[10]RW EC[5]	Phase 2 !PG[10]RW EC[6]	Phase 3 !PG[10]RW EC[7]	1
DQ4	0	Phase 0 PG[10]RW ED[0]	Phase 1 PG[10]RW ED[1]	Phase 2 PG[10]RW ED[2]	Phase 3 PG[10]RW ED[3]	0
DQ5	1	Phase 0 !PG[10]RW ED[4]	Phase 1 !PG[10]RW ED[5]	Phase 2 !PG[10]RW ED[6]	Phase 3 !PG[10]RW ED[7]	1
DQ6	0	Phase 0 PG[10]RW EE[0]	Phase 1 PG[10]RW EE[1]	Phase 2 PG[10]RW EE[2]	Phase 3 PG[10]RW EE[3]	0
DQ7	1	Phase 0 !PG[10]RW EE[4]	Phase 1 !PG[10]RW EE[5]	Phase 2 !PG[10]RW EE[6]	Phase 3 !PG[10]RW EE[7]	1
DQS1	0	Phase 0 PG[10]RW EA[0]	Phase 1 PG[10]RW EA[1]	Phase 2 PG[10]RW EA[2]	Phase 3 PG[10]RW EA[3]	0

NOTE 1 The UIs are per pseudo-channel in Mux mode, and interleaved at Host interface based on PS value in READ command.

## 8.13 Host Interface Training during Self-Refresh Mode (HIT-SR)

HIT-SR is supported during Self-Refresh without Clock Stop mode only. HIT-SR will allow the Host controller to put DRAMs into self-refresh, and enable any of the Host interface training modes including HWL, HIW, HIR, ERTM, EWTM, and HPA. Only functional commands that can be used while in this mode are RD, WR, MRR and MRW.

The operation sequence of MDB HIT-SR is the following:

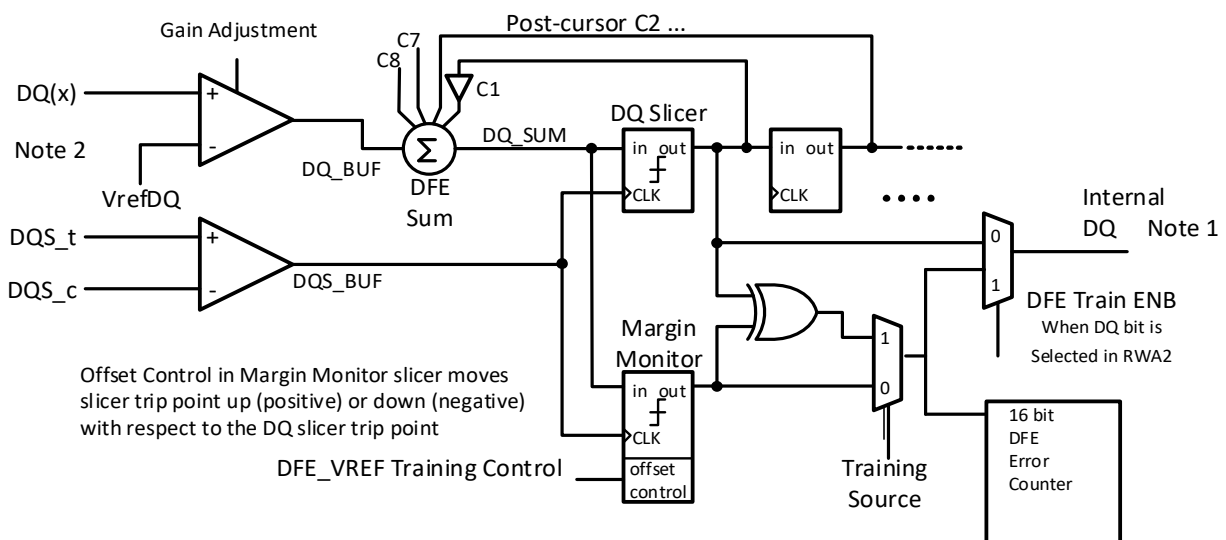
1. To enable the HIT-SR in MDB, the Host controller will configure [RW83\[7\]](#) to 1.
2. The MDB will ignore the following SRE command on the BCOM bus.
3. After the Host interface training is finished, the Host controller will configure [RW83\[7\]](#) to 0 to disable the feature.

## 9 Decision Feedback Equalization (DFE)

The DDR5MDB02 device will support an 8 Tap decision feedback equalization (DFE) on its Host-interface receivers. The Host can enable 1, 2, 3, 4, 5, 6, 7, or 8 taps in a consecutive order always starting with Tap 1 as shown in Table 58, “DFE Tap Configurations”. The DFE Tap Coefficients and Gain adjustments are set by control words [PG\[5:4\]RWE0- RWFF](#), [PG\[7B\]RW\[E0, E1, E4, E5, E8, E9, EC, ED\]](#), and [PG\[F\]RW\[F0:F8\]](#). These DFE control words allow programming of each parameter on a DQ I/O-specific basis, and they are intended to be trained by the Host. The DDR5MDB02 device does not support adaptive DFE. In order to allow Data Buffer hardware to correctly preset DFE post-cursor bit values before the start of Write data bursts, all DQ pins must be at or above VDD(min) during DQS preamble and interamble. There is no DQ preamble requirement. MDB RTT if enabled will pull up the bus on DQ pins at or above VDD(min) during DQS preamble and interamble.

The Host guarantees that the time corresponding to the number of DFE taps is less than or equal to the preamble period. When the DQS1\_t/c signals are used as CRC lane:

- For the Read direction, MDB needs to drive DQS1 differential HIGH for the number of DFE taps enabled during DQ preamble period with the assumption that Host Rx has the same number of DFE taps as the MDB DQS1, i.e., [PG\[F\]RWFD](#).
- For the Write direction, Host needs to drive DQS1 differential HIGH for the number of DFE taps enabled, as defined in [PG\[F\]RWFD](#), during DQ preamble period.



NOTE 1 This signal propagates through the Data Buffer device and supports regular DDR5MDB02 features such as DRAM Data Writes

NOTE 2 When used as a CRC lane, DQS1\_t/c as a differential input pair also has DFE support.

**Figure 89 — DFE Training Circuitry per Pin**



## 9.1 DFE Tap Configurations

**Table 58 — DFE Tap Configurations**

RWA0 OP4	RWA0 OP5	RWA0 OP6	RWA0 OP7	PG [70] RWE8 OP0	PG [70] RWE8 OP1	PG [70] RWE8 OP2	PG [70] RWE8 OP3	Tap 1	Tap 2	Tap 3	Tap 4	Tap 5	Tap 6	Tap 7	Tap 8
0	x	x	x	x	x	x	x	Dis- abled	Dis- abled <sup>1</sup>	Dis- abled <sup>1</sup>	Dis- abled <sup>1</sup>	Dis- abled <sup>1</sup>	Dis- abled <sup>1</sup>	Dis- abled <sup>1</sup>	Dis- abled <sup>1</sup>
1	0	x	x	x	x	x	x	Enabled	Dis- abled	Dis- abled <sup>2</sup>	Dis- abled <sup>2</sup>	Dis- abled <sup>2</sup>	Dis- abled <sup>2</sup>	Dis- abled <sup>2</sup>	Dis- abled <sup>2</sup>
1	1	0	x	x	x	x	x	Enabled	Enabled	Dis- abled	Dis- abled <sup>3</sup>	Dis- abled <sup>3</sup>	Dis- abled <sup>3</sup>	Dis- abled <sup>3</sup>	Dis- abled <sup>3</sup>
1	1	1	0	x	x	x	x	Enabled	Enabled	Enabled	Dis- abled	Dis- abled <sup>4</sup>	Dis- abled <sup>4</sup>	Dis- abled <sup>4</sup>	Dis- abled <sup>4</sup>
1	1	1	1	0	x	x	x	Enabled	Enabled	Enabled	Enabled	Dis- abled	Dis- abled <sup>5</sup>	Dis- abled <sup>5</sup>	Dis- abled <sup>5</sup>
1	1	1	1	1	0	x	x	Enabled	Enabled	Enabled	Enabled	Enabled	Dis- abled	Dis- abled <sup>6</sup>	Dis- abled <sup>6</sup>
1	1	1	1	1	1	0	x	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Dis- abled	Dis- abled <sup>7</sup>
1	1	1	1	1	1	1	0	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Dis- abled
1	1	1	1	1	1	1	1	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled

NOTE 1 MDB Hardware disabled when RWA0[4] = 0, and RWA0[7:5] & PG[70]RWE8[3:0] are don't care and ignored by the MDB.

NOTE 2 MDB Hardware disabled when RWA0[5] = 0, and RWA0[7:6] & PG[70]RWE8[3:0] are don't care and ignored by the MDB.

NOTE 3 MDB Hardware disabled when RWA0[6] = 0, and RWA0[7] & PG[70]RWE8[3:0] are don't care and ignored by the MDB.

NOTE 4 MDB Hardware disabled when RWA0[7] = 0, and PG[70]RWE8[3:0] are don't care and ignored by the MDB.

NOTE 5 MDB Hardware disabled when PG[70]RWE8[0] = 0, and PG[70]RWE8[3:1] are don't care and ignored by the MDB.

NOTE 6 MDB Hardware disabled when PG[70]RWE8[1] = 0, and PG[70]RWE8[3:2] are don't care and ignored by the MDB.

NOTE 7 MDB Hardware disabled when PG[70]RWE8[2] = 0, and PG[70]RWE8[3] is a don't care and ignored by the MDB.

## 9.2 DFE Gain and Tap Range

**Table 59 — DFE Gain and Tap Total Control Word Range**

DFE Parameter	Min	Max	Unites
Gain	-6	6	dB
Tap 1	- 150	150	mV
Tap 2	- 60	60	mV
Tap 3	- 45	45	mV
Tap 4	- 45	45	mV
Tap 5	- 45	45	mV
Tap 6	- 45	45	mV
Tap 7	- 45	45	mV
Tap 8	- 45	45	mV

**Table 60 — DFE Gain and Tap Coefficient Step Parameters**

DFE Parameter	DDR5-3200 - 12800			Unit
	Min	Typ	Max	
DFE Gain Bias Step Size <sup>1,2</sup>	1.7	2	2.3	dB
DFE Gain Bias Tolerance (INL) <sup>1,2</sup>	- 0.5	-	0.5	dB
DFE Gain Bias Step Size Tolerance (DNL) <sup>1,2</sup>	- 0.3	-	0.3	dB
DFE Gain Bias Step Time <sup>1</sup>	-	-	300	ns
DFE Tap Bias Step Size <sup>1,2</sup>	0.5	1.5	2.5	mV
DFE Tap Bias Tolerance (INL) (-150 mV to 0 mV) <sup>1,2</sup>	Min (V <sub>ideal</sub> x 115%, V <sub>ideal</sub> - 6 * LSB) <sup>3,4</sup>	-	Max (V <sub>ideal</sub> x 85%, V <sub>ideal</sub> + 6 * LSB) <sup>3,4</sup>	mV
DFE Tap Bias Tolerance (INL) (0 mV to 150 mV) <sup>1,2</sup>	Min(V <sub>ideal</sub> x 85%, V <sub>ideal</sub> - 6 * LSB) <sup>3,4</sup>	-	Max(V <sub>ideal</sub> x 115%, V <sub>ideal</sub> + 6 * LSB) <sup>3,4</sup>	mV
DFE Tap Bias Step Size Tolerance (DNL) <sup>2</sup>	- 66.67	-	66.67	% of Step Size
DFE Tap Bias Step Time	-	-	96	tBCK

NOTE 1 Host Vref fixed at 0.75 x V<sub>DD</sub>, typical Voltage-Temperature condition (i.e., V<sub>DD</sub> = 1.1 V, 25 °C), and default gain setting.

NOTE 2 These parameters are neither subject to silicon validation nor production testing.

NOTE 3 V<sub>ideal</sub> refers to the ideal DFE Tap value based on the setting.

NOTE 4 LSB = 1.5 mV.

## 9.3 Training Accelerator for Decision Feedback Equalization (DFE)

If the MDB is in Mux mode, when the MDB is in DFE training mode, write commands to the two pseudo-channels will occur such that the data is continuous. The write commands between the pseudo-channels may be offset, such that one pseudo-channel starts before the other and one pseudo-channel ends before the other, but once started, the write commands will cause continuous data. The MDB Accelerator Write Limit for MRDIMM is based on the total number of writes regardless which PS was targeted. If both pseudo-channels are targeted at on the same clock, both will be counted toward the Write Limit.

If the MDB is in Rank mode, when the MDB is in DFE training mode, the MDB Accelerator Write Limit for MRDIMM is based on the total number of writes regardless which Rank was targeted.

The Data Buffer will support the ability to accelerate DFE training sweeps of critical DFE training parameters for each DQ bit that is enabled for DFE training. This functionality is provided by the DFE training accelerator (DFETA). Figure 90 shows a top-level block diagram for the DFETA and Figure 91 shows the DFETA Flow. There is a single DFETA mode that is global to all DQ pins.

To perform DFE training acceleration, the Host first makes sure that the monitor path is selected in [RWA1](#), to directly drive its internal DQ path, and that DQ[x] has DFE training mode enabled.

When enabled, the DFETA has the ability to override VrefDQ, DFE Tap coefficients, and DFE\_Vref. VrefDQ, DFE Tap coefficient biases, and DFE\_Vref become DFETA loop parameters. DQ's and DQS1 that are not enabled for training in [RWA2](#) and [RWA1\[7\]](#) shall maintain their per-pin values in [PG\[6:4\]](#) and [PG2](#). This processing flow implements inner and outer loop levels as shown in Figure 91. The loop parameter values applied by the DFETA depend on how the Host has configured its inner and outer loop parameter selection and control.

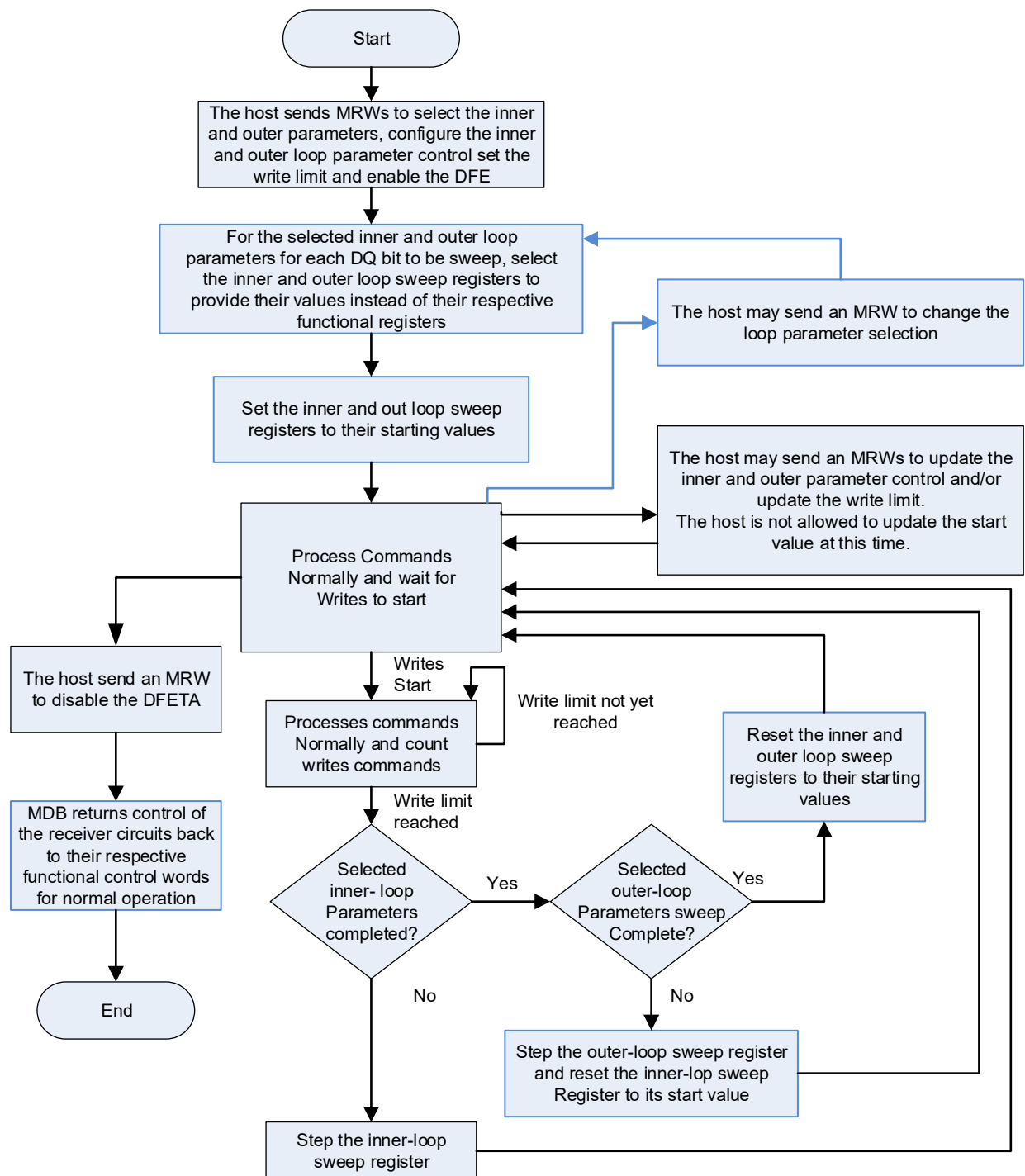
For each DFETA iteration, the Host performs a series of Writes to the DRAM followed by a complimentary series of reads from the DRAM, and the Host performs the necessary pattern comparison.

The diagram illustrates the DFE Training Accelerator architecture. It shows the flow of data and control signals between various components:

- Command Processor** sends a **Write** signal to the **DFE Training Accelerator**.
- Control Registers** send a signal to the **DFE Training Accelerator**.
- Gain Adjustment** block receives **PG[5:4]RW[F8, F0, E8, F0]** and **DQ** as inputs. It outputs **DQ** to the **DFE Sum** block and **VrefDQ** to the **DFE\_VREF Training Control** block.
- DFE Sum** block receives **DQ** and **DQSUM** (from **Post-cursor C2 ...**) as inputs. It outputs **DQ SUM** to the **DQ Slicer** block.
- DQ Slicer** block receives **DQ SUM** and **DQ** as inputs. It outputs **DQ SUM** to the **Margin Monitor** block.
- Margin Monitor** block receives **DQ SUM** and **DQ** as inputs. It outputs **DQ SUM** to the **DFE\_VREF Training Control** block.
- DFE\_VREF Training Control** block receives **VrefDQ** and **DQ SUM** as inputs. It outputs **offset control** to the **Margin Monitor** block.
- Offset Control** block receives **offset control** and **DQ SUM** as inputs. It outputs **DQ SUM** to the **DFE\_VREF Training Control** block.
- DFE Train ENB** block receives **DQ SUM** and **DQ** as inputs. It outputs **DFE Train ENB** to the **16 bit Error Counter**.
- 16 bit Error Counter** block receives **DFE Train ENB** and **Training Source** as inputs. It outputs **DFE Train ENB** to the **DFE\_VREF Training Control** block.

**Figure 90 — DFE Training Accelerator**

### 9.3 Training Accelerator for Decision Feedback Equalization (DFE) (cont'd)



**Figure 91 — DFE Training Accelerator Flow**

Note: When Host reads current loop parameter value MDB shall provide the value for upcoming or next write command.

### 9.3 Training Accelerator for Decision Feedback Equalization (DFE) (cont'd)

The DFETA partitions the loop parameters into inner and outer loop parameter sets. These are shown in Table 61. The Host selects one parameter out of each set for a particular training scenario. When the NULL parameter is selected for a particular loop level, each pass of the loop does not modify a loop parameter.

**Table 61 — Loop Parameter Partitioning**

Inter-Loop Parameters	Outer-Loop Parameters
VrefDQ	DFE Tap-1 Coefficient
DFE_Vref	DFE Tap-2 Coefficient
NULL	DFE Tap-3 Coefficient
	DFE Tap-4 Coefficient
	DFE Tap-5 Coefficient
	DFE Tap-6 Coefficient
	DFE Tap-7 Coefficient
	DFE Tap-8 Coefficient
	NULL

In addition to selecting the inner and outer loop parameters, the Host must also configure the inner and output loop controls, each consisting of starting value, step size and number of increments. This is summarized in Table 62. It is the Host's responsibility to make sure that loop parameter ranges are not exceeded depending on the starting value, step size and number of increments specified.

The Tap-x coefficient biases (in the outer loop) and DFE\_Vref registers (in the inner loop) are defined as signed-magnitude numbers, whereas the inner loop and outer-loop start values are defined as a two's complement number to simplify the logic in the accelerator state machine for incrementing from negative to positive values. The Data Buffer must convert the inner/outer-loop sweep register value from two's complement to signed-magnitude for the corresponding parameter.

**Table 62 — DFETA Loop Control**

Loop Level	Loop Control	Register
Inner	Start Value	PG[9]RW[E2:E1] Inner Loop Start Value
	Step Size	PG[9]RWE7[3:0] Inner Loop Step Size
	Number of increments	PG[9]RWE[9:8] Inner Loop Number of Increments
Outer	Start Value	PG[9]RW[E3] Outer Loop Start Value
	Step Size	PG[9]RWE7[7:4] Outer Loop Step Size
	Number of increments	PG[9]RWEA Outer Loop Number of Increments

Example use cases and respective configurations are shown in Table 63.

**Table 63 — DFETA Example Use Cases and Configurations**

Use Case	Inner-Loop Parameter	Outer-Loop Parameter
Pulse Response measurement	DFE_Vref	NULL with the number of outer loop increments set to one
Eye height margin measurement	DFE_Vref	Tap-x Coefficient Bias
2D eye measurements	DFE_Vref	NULL with the number of outer loop increments set to the number of Host increments

### 9.3 Training Accelerator for Decision Feedback Equalization (DFE) (cont'd)

As shown in Figure 91, after the Host configures and enables the DFETA, the DFETA enters a wait state and waits for writes to start. While in the wait state, the MDB processes commands normally.

Once writes start, the DFETA moves to the write state and begins counting write commands. The number of writes in the series of writes can vary depending on the training scenario. A series of writes can be composed of non-contiguous or back-to-back write commands. The DFETA provides a programmable 16-bit write-limit counter to detect the end of each series of writes. The write-limit is configured using [PG\[9\]RW\[EF:EE\]](#). The write limit counter is re-initialized for the next full count period each time the wait state is entered. It is the responsibility of the Host to make sure that the number of writes sent matches the write limit. The write-limit counter state can be read via MRRs to read-only registers, [PG\[9\]RW\[F1:F0\]](#).

While in the write state, the MDB processes writes normally until the write limit is reached. The MDB processes other commands normally as well. If an MRR or a Read command occurs, the DFETA will maintain its state. If a MDB-space MRW command occurs, it is the Host's responsibility to make sure that it does not alter any registers that will perturb the current DFETA iteration. If an MPC command occurs, the DFETA will maintain its state.

While in the wait state, the Host may send an MRW to change the loop parameter selection.

For example, if the Tap-1 coefficient bias is currently the selected outer-loop parameter, the actual  $t_{\text{Tap-1}}$  coefficient bias value is determined by the outer-loop sweep register instead of the functional Tap-1 coefficient bias register.

If the Tap-2 coefficient bias is then selected as the outer-loop parameter, the actual Tap-2 coefficient bias value is then determined by the outer-loop sweep register, and the actual Tap-1 coefficient bias value returns to being determined by its functional Tap-1 coefficient bias register. Since the wait state allows for normal command processing, the Host can send MRWs to change the settings of any of the functional VrefDQ, DFE tap coefficient bias, and DFE\_Vref registers while in the wait state.

While in the wait state, the Host may send MRWs to update the inner and outer loop parameter control and/or update the write limit.

When the write limit is reached, the Host must stop write traffic and must wait  $t_{\text{DFETA\_LoopUpdateWait}}$  for the DFETA to update its inner and outer loop parameters for the next iteration as shown in Figure 91.

When the DFETA is disabled, the selected inner and outer loop parameters are returned to being determined by their respective functional registers.

The timing parameters associated with the DFETA are shown in Table 246.

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## 10 DDR5MDB02 Device Equalization Self-Train (DESTM)

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To improve the training time of DFE and CTLE on the DQ and DQS1 as CRC signals, an alternative training method is defined to calibrate the DFE tap coefficients and CTLE settings on DQ and DQS1 as CRC Host-interface input receivers.

The Host must configure the DESTM LFSR pattern length and select the DQ and DQS1 as CRC signals, which will be trained. The Host must also enable DFE Taps [RWA0\[7:4\]](#), [PG\[70\]RWE8\[3:0\]](#), [PG\[F\]RWFD](#), and DFE ENB/Vref [RWA0\[1:0\]](#) prior to enabling the DESTM. If the DESTM training is to include CTLE coefficients then the Host must enable CTLE [PG\[D\]RWE0\[0\]](#) as part of the configuration process.

Once the configuration is done, and prior to Start Training, the Host will start driving DQS toggles and sending the LFSR pattern to the selected DQ and DQS1 as CRC signals. The Host must continue driving the LFSR until the DESTM training is completed, as shown in Figure 92. Regardless of Mux mode or Rank mode, during DESTM two independent LFSR training patterns, with the same 8-bit or 16-bit length, are issued by the controller to each DQ or DQS1 as CRC lane. One LFSR training pattern is for PS0 in Mux mode or even UI in Rank mode at the DQS rising edge, while the other LFSR training pattern is for PS1 in Mux mode or odd UI in Rank mode at the DQS falling edge.

The DESTM training sequence is started when the Host enables the Training Start bit in [PG\[F\]RWE0\[1\]](#) through BCOM bus. The MDB drives LBTXDQ LOW during the DESTM operation. The input receivers will train their internal DFE Tap coefficients for all enabled Taps and CTLE settings automatically. Once the optimum settings are found, the device will clear [PG\[F\]RWE0\[1\]](#) and signal the Host by driving LBTXDQ back to HIGH prior to  $t_{\text{DESTM}}$ . if [PG\[F\]RWE0\[7\]=1](#).

After MDB de-asserts the LBTXDQ, the Host can either restart the training or exit the DESTM mode through BCOM bus, as shown in Figure 93. The Host may stop the training at any time through a BCOM write to [PG\[F\]RWE0\[1:0\]](#).

The Fail Status registers are read-only and indicate an error has occurred. The fail status register bits are updated when DESTM training stops, either by the Host or MDB self-clear of [PG\[F\]RWE0\[1\] = "0"](#).

If the MDB did not execute the training correctly by  $t_{\text{DESTM}}$ , the MDB will not de-assert LBTXDQ, at this point the Host will stop the training through BCOM by writing [PG\[F\]RWE0\[1\] = 0](#) and the MDB will update Fail Status Registers [PG\[F\]RWE3\[7\]](#) and [PG\[F\]RWE5\[7:0\]](#).

When the continuous training mode is enabled, the device will repeatedly run the internal training state machine on one selected signal until the Host stops the training by writing [PG\[F\]RWE0\[1\]="0"](#). Prior to the continuous training mode being enabled, the Host must disable the LBTXDQ Low Assertion feature by setting [PG\[F\]RWE0\[7\]="0"](#). The Host must repeat the entire flow for the next selected signal to be trained in continuous mode.

At the end of the training procedure, the selected DFE Tap coefficients and CTLE settings registers on the selected DQ and DQS1 as CRC bits will be updated by the MDB device with the trained results.

# 10 DDR5MDB02 Device Equalization Self-Train (DESTM) (cont'd)

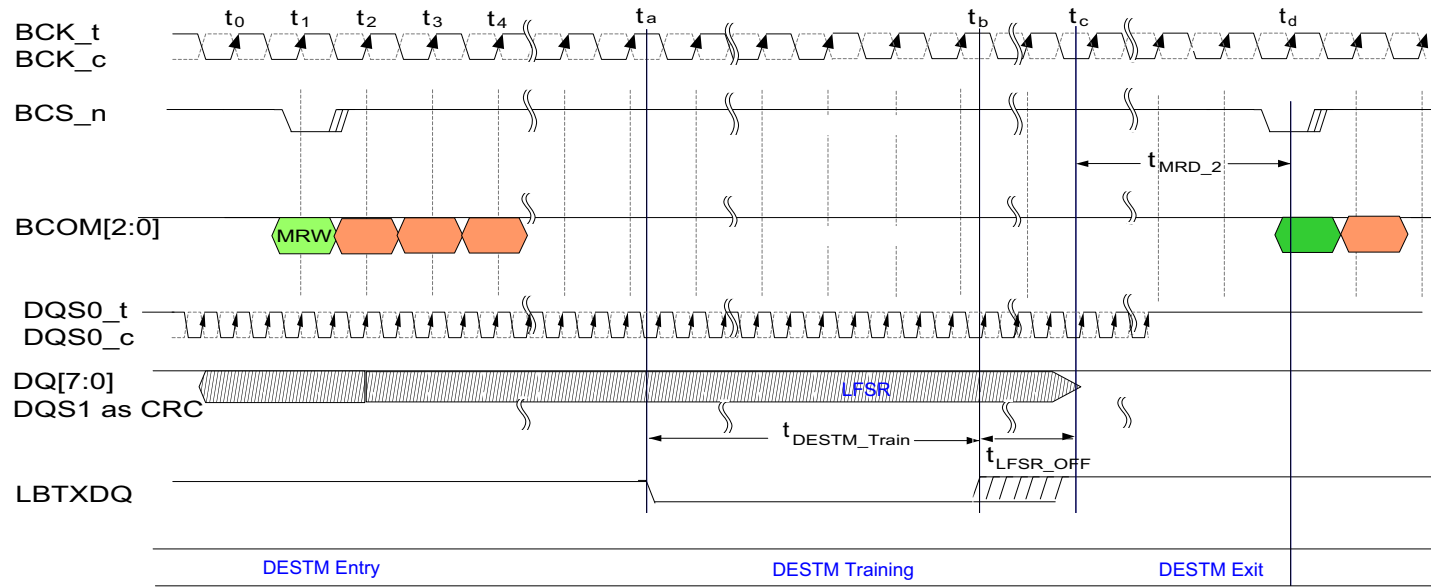


Figure 92 — DESTM Start and Stop Training Timing Diagram



## 10 DDR5MDB02 Device Equalization Self-Train (DESTM) (cont'd)

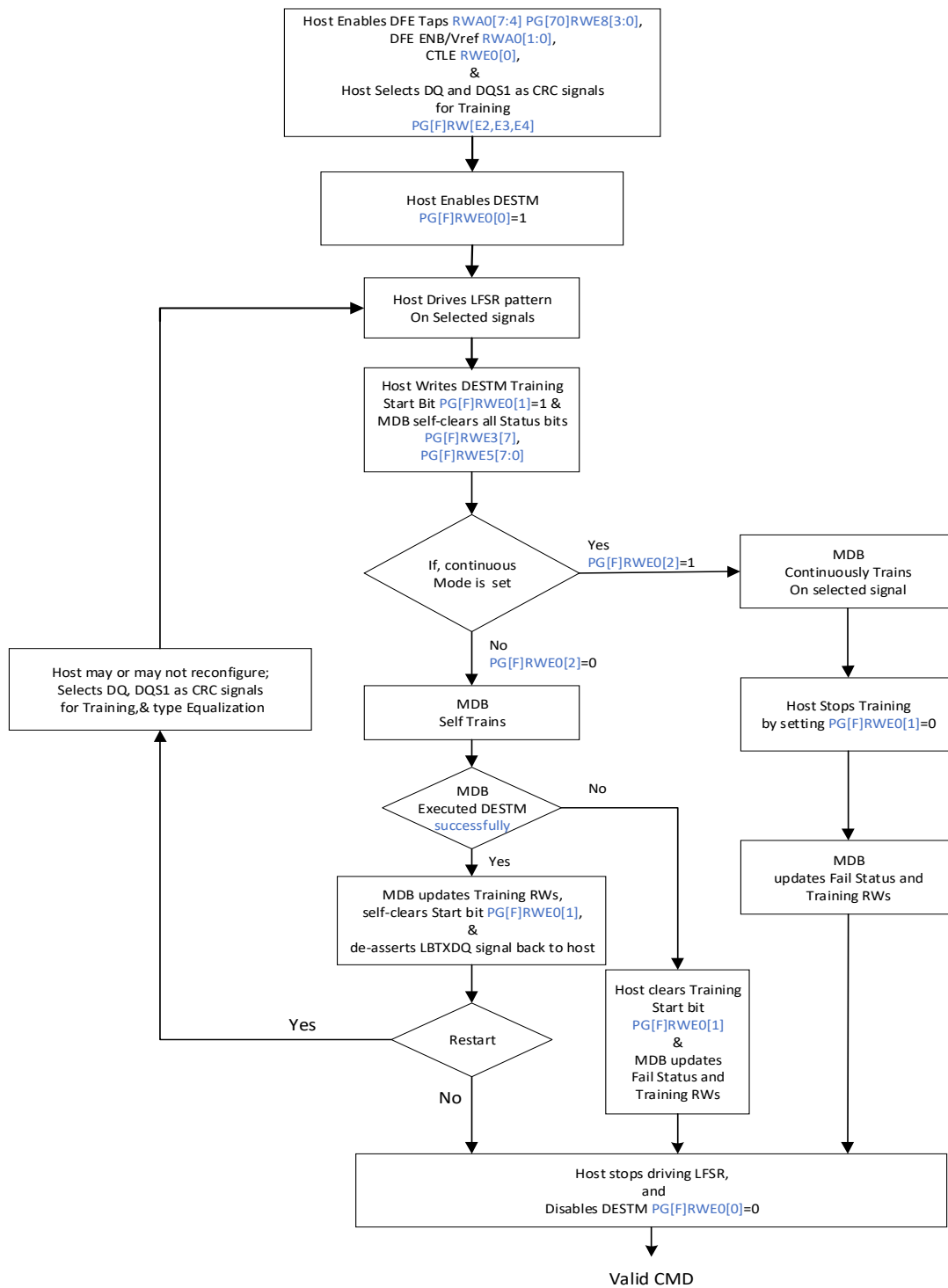


Figure 93 — Example Flow after DESTM Configuration

## 11 Control Words

The DDR5MDB02 device features a set of 8-bit control words, which allow the optimization of the device properties for different raw card designs. MRCD and DDR5MDB02 control word writes appear as MRW commands but with the CW bit HIGH. DRAMs will ignore MRW commands with the CW bit set HIGH. The different control words and settings are described below. Any change to these control words require some time for the device to settle, these times are defined in Table 246. The chip select input, BCS\_n, must be kept HIGH during that time.

The DDR5MDB02 must support control word access for any of the DDR5MDB02 specified frequency ranges.

### 11.1 Register Word Decoding

The MRW command sequence is defined in Chapter 5.4.6, “MRW Commands,”. The RW address and the settings are transmitted over the MRA bits included in the MRW command sequence in the six clock cycles immediately following the cycle when the 100b BCOM command is captured. The reset default state of all control word bits unless otherwise specified is ‘0’. Every time the device is reset, its default state is restored. Stopping the clocks (BCK\_t = BCK\_c = HIGH) to put the device in low-power mode will not alter the control word settings.

Data Buffer Control Word attributes can be:

- Reserved<sup>2</sup>
- Read Only
- Write Only
- RD/WR
- Sticky - Cleared by power cycle not Reset

The DDR5 Mode Register space is divided as follows:

**Table 64 — Control Word Addressing**

CW bit	MRA7	Description
0	x	DRAM MR space.
1	0	MRCD CW space. 128 registers decoded via MRA[6:0]
1	1	Data Buffer CW space. 128 registers decoded via MRA[6:0]

Within the MDB control word space, 96 registers are accessed directly, while 32 registers are addressed through an 8-bit paging system, providing 8192 registers. **RWDF** is the page register while addresses E0-FF are used to access the registers within each page. Pages 00-7F are for JEDEC use while pages 80-FF are vendor specific.

2. Reserved control bits may not be physically implemented and they shall be written to zero to ensure forward compatibility.

## 11.1 Register Word Decoding (cont'd)

**Table 65 — Control Word Spaces**

MRA[7:0]	Location	Page Pointer RW <sup>1</sup>	Page value	Definition	Size (bytes)	Description
00h to 5Fh	MRCD	RW5F	X	JEDEC	96	96 directly addressed registers
60h to 7Fh	MRCD	RW5F	00h-7Fh	JEDEC	4096	32 paged registers
60h to 7Fh	MRCD	RW5F	80h-FFh	Vendor	4096	32 paged registers
80h to DFh	Data Buffer	RWDF	X	JEDEC	96	96 directly addressed registers
E0h to FFh	Data Buffer	RWDF	00h-7Fh	JEDEC	4096	32 paged registers
E0h to FFh	Data Buffer	RWDF	80h-FFh	Vendor	4096	32 paged registers

NOTE 1 RW5F is the Page Pointer located in the DDR5MRCD and RWDF is the Page Pointer located in the DDR5MDB02.

All registers are 8-bits wide. If enabled in MRCD, all MRW accesses are sent across the BCOM bus to the data buffers, allowing the data buffers to snoop values sent to the DRAM or MRCD.

## 11.2 Reading Control Words from Data Buffer

MRR commands read data from the MR locations in either the DRAM or the data buffer. MR locations in the MRCD must be read by first transferring their contents to a DRAM register and then reading that DRAM register using the MRR command. If the CW bit of the MRR command is 0, the MR read data will come from the DRAM and the data buffer will treat the command like a regular Read command. If the CW bit is 1, the MR read data will come from the data buffer and all undefined or reserved bits in the selected MR location will be driven as '0' by the DDR5MDB02.

The data buffer will always drive valid data and strobe pattern sequences on its Host interface in response to an MRR command. Depending on the value of the MRR CW bit, the data may come from DRAMs or from internal registers. When the MRR command has CW = 1 and MRA7 = 0, the data buffer treats the target location as Reserved and returns all-zero bit values regardless of the address code in MRA[6:0].

### 11.3 Direct Control Word Decoding

**Table 66 — Direct Control Word Decoding**

	Register Control Word	MRA [7:0] HEX <sup>1</sup>	Meaning
Modes	RW80 <sup>2</sup>	0x80	Features
	RW81	0x81	Buffer Configuration Modes
	RW82	0x82	BCS_n BCOM Training
	RW83	0x83	[M]DQS, [M]DQ Training Modes
Timing and Voltage	RW84 <sup>2</sup>	0x84	MRDIMM Host Interface Operating Speed
	RW85 <sup>2</sup>	0x85	Host Interface Fine Granularity DIMM Operating Speed
	RW86 <sup>2</sup>	0x86	DQS Park Termination
	RW87 <sup>2</sup>	0x87	Host Interface DQ RTT Park Termination
	RW88 <sup>2</sup>	0x88	Reserved
	RW89	0x89	Reserved
	RW8A <sup>2</sup>	0x8A	Host Interface DQ Driver
	RW8B <sup>2</sup>	0x8B	DRAM Interface MDQ Driver and Termination
	RW8C <sup>2</sup>	0x8C	MDQS and MDQ PARK
	RW8D	0x8D	Loopback Control
	RW8E	0x8E	Loopback RTT and Ron
	RW8F <sup>2</sup>	0x8F	Host Interface Read DQS Offset Timing
Data Training	RW90	0x90	Continuous Burst Mode Control
	RW91	0x91	Reserved
	RW92 <sup>2</sup>	0x92	PBA Enumerate ID Control Word
	RW93 <sup>2</sup>	0x93	PBA Buffer Select ID Control Word
	RW94	0x94	Internal Receive Enable Offset Coarse Status
	RW95	0x95	Internal Receive Enable Offset Fine Lower Nibble Status
	RW96	0x96	Internal Receive Enable Offset Fine Upper Nibble Status
	RW97	0x97	Buffer Training Configuration Control Word
	RW98	0x98	PS0 Buffer Training Status Word
	RW99	0x99	PS1 Buffer Training Status Word
	RW9A	0x9A	Reserved
	RW9B	0x9B	Reserved
	RW9C	0x9C	PS0 LFSR0 State Monitor for Reads
	RW9D	0x9D	PS0 LFSR1 State Monitor for Reads
	RW9E	0x9E	PS0 LFSR0 State Monitor for Writes
	RW9F	0x9F	PS0 LFSR1 State Monitor for Writes
DFE	RWA0 <sup>2</sup>	0xA0	DFE Global Control
	RWA1	0xA1	DQ[7:0] DFE Training Mode and DQS1 DFE pin selection
	RWA2	0xA2	DQn DFE pin selection
Periodic	RWB0	0xB0	DRAM tDQS2DQ Tracking
	RWB1	0xB1	DRAM tDQS2DQ Tracking Return Value
Reserved	RWB2	0xB2	Reserved
	...	...	Reserved
	RWBF	0xBF	Reserved
Static MRR	RWC0	0xC0	Target Read Page Address
	RWC1	0xC1	Target Read Byte Address
	RWC2	0xC2	Static MRR Control
Reserved	RWC3	0xC3	Reserved
	...	...	Reserved
	...	...	Reserved
	...	...	Reserved
	RWDE	0xDE	Reserved
CW Page	RWDF	0xDF	CW MDB Page

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

NOTE 2 Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

## 11.4 Paged Control Word Decoding

### 11.4.1 PG[0,1,72,73] Training Control Word Decoding

Table 67 — PG[73:72, 1:0] Training Control Word Decoding <sup>1,2</sup>

Page	Register Control Word	MRA [7:0] HEX <sup>3</sup>	Meaning
[73:72, 1:0] <sup>4</sup>	RWE0 <sup>5</sup>	0xE0	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word
	RWE1 <sup>3</sup>	0xE1	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word
	RWE2 <sup>3</sup>	0xE2	Lower nibble DRAM interface receive enable training control
	RWE3 <sup>3</sup>	0xE3	Upper nibble DRAM interface receive enable training control
	RWE4 <sup>3</sup>	0xE4	Lower nibble MDQS read delay control
	RWE5 <sup>3</sup>	0xE5	Upper nibble MDQS read delay control
	RWE6 <sup>3</sup>	0xE6	Lower nibble MDQ Write Baseline Delay control
	RWE7 <sup>3</sup>	0xE7	Upper nibble MDQ Write Baseline Delay control
	RWE8 <sup>3</sup>	0xE8	Lower nibble DRAM interface write leveling control
	RWE9 <sup>3</sup>	0xE9	Upper nibble DRAM interface write leveling control
	RWEA <sup>3</sup>	0xEA	MDQ0/4-Read delay control
	RWEB <sup>3</sup>	0xEB	MDQ1/5-Read delay control
	RWEC <sup>3</sup>	0xEC	MDQ2/6-Read delay control
	RWED <sup>3</sup>	0xED	MDQ3/7-Read delay control
	RWEE <sup>3</sup>	0xEE	MDQ0/4-MDQS write delay control
	RWEF <sup>3</sup>	0xEF	MDQ1/5-MDQS write delay control
	RWF0 <sup>3</sup>	0xF0	MDQ2/6-MDQS write delay control
	RWF1 <sup>3</sup>	0xF1	MDQ3/7-MDQS write delay control
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 The Data Path Training modes are performed with Fixed BL16.

NOTE 2 The timing registers in PG[73:72, 1:0] of the register space are still independent per nibble when the x8 strobes are used.

NOTE 3 [MRA7](#) must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

NOTE 4 In Mux mode, PG[73] is for PS1 Rank1, PG[72] is for PS1 Rank0, PG[1] is for PS0 Rank1, and PG[0] is for PS0 Rank0. In Rank mode, PG[73] is for Rank3, PG[72] is for Rank2, PG[1] is for Rank1, and PG[0] is for Rank0.

NOTE 5 Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

## 11.4.2 Page 2 Vref Paged Control Word Decoding

Table 68 — Page 2 Vref Paged Control Word Decoding

Page	Register Control Word	MRA [7:0] HEX <sup>1</sup>	Meaning
[0x02]	RWE0 <sup>2</sup>	0xE0	DQ0 VrefDQ
	RWE1 <sup>2</sup>	0xE1	DQ1 VrefDQ
	RWE2 <sup>2</sup>	0xE2	DQ2 VrefDQ
	RWE3 <sup>2</sup>	0xE3	DQ3 VrefDQ
	RWE4 <sup>2</sup>	0xE4	DQ4 VrefDQ
	RWE5 <sup>2</sup>	0xE5	DQ5 VrefDQ
	RWE6 <sup>2</sup>	0xE6	DQ6 VrefDQ
	RWE7 <sup>2</sup>	0xE7	DQ7 VrefDQ
	RWE8	0xE8	Reserved
	RWE9	0xE9	Reserved
	RWEA	0xEA	Reserved
	RWEB	0xEB	Reserved
	RWEC	0xEC	Reserved
	RWED	0xED	Reserved
	RWEE	0xEE	Reserved
	RWEF	0xEF	Reserved
	RWF0 <sup>2</sup>	0xF0	PS0 or {R0, R1} group Lower Nibble VrefMDQ
	RWF1 <sup>2</sup>	0xF1	PS0 or {R0, R1} group Upper Nibble VrefMDQ
	RWF2 <sup>2</sup>	0xF2	PS1 or {R2, R3} group Lower Nibble VrefMDQ
	RWF3 <sup>2</sup>	0xF3	PS1 or {R2, R3} group Upper Nibble VrefMDQ
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	BVref
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

NOTE 2 Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

### 11.4.3 Page 3 Serial Number Control Word Decoding

Page 3 [RWE0](#) ~ [RWEE](#) control words in the DDR5MDB02 contain detailed MDB manufacturing information provided by MDB vendor. This information is programmed in one-time programmable memory (OTP), which must not be possible for the user to modify. The purpose is for improved manufacturing logistics management and not meant to be used by Host platform to control normal operation. These registers must be accessible during run time.

**Table 69 — Page 3 Serial Number Control Word Decoding**

Page	Register Control Word	MR [7:0] HEX <sup>1</sup>	Meaning
0x03	<a href="#">RWE0</a>	0xE0	Date Code Byte 0
	<a href="#">RWE1</a>	0xE1	Date Code Byte 1
	<a href="#">RWE2</a>	0xE2	Date Code Byte 2
	<a href="#">RWE3</a>	0xE3	Vendor Specific Unique Unit Code Byte 0
	<a href="#">RWE4</a>	0xE4	Vendor Specific Unique Unit Code Byte 1
	<a href="#">RWE5</a>	0xE5	Vendor Specific Unique Unit Code Byte 2
	<a href="#">RWE6</a>	0xE6	Vendor Specific Unique Unit Code Byte 3
	<a href="#">RWE7</a>	0xE7	Vendor Specific Unique Unit Code Byte 4
	<a href="#">RWE8</a>	0xE8	Vendor Specific Unique Unit Code Byte 5
	<a href="#">RWE9</a>	0xE9	Vendor Specific Unique Unit Code Byte 6
	<a href="#">RWEA</a>	0xEA	Vendor ID Byte 0
	<a href="#">RWEB</a>	0xEB	Vendor ID Byte 1
	<a href="#">RWEC</a>	0xEC	Vendor Device ID Byte 0
	<a href="#">RWED</a>	0xED	Vendor Device ID Byte 1
	<a href="#">RWEE</a>	0xEE	Revision ID
	<a href="#">RWEF</a>	0xEF	Reserved
	<a href="#">RWF0</a>	0xF0	Reserved
	<a href="#">RWF1</a>	0xF1	Reserved
	<a href="#">RWF2</a>	0xF2	Reserved
	<a href="#">RWF3</a>	0xF3	Reserved
	<a href="#">RWF4</a>	0xF4	Reserved
	<a href="#">RWF5</a>	0xF5	Reserved
	<a href="#">RWF6</a>	0xF6	Reserved
	<a href="#">RWF7</a>	0xF7	Reserved
	<a href="#">RWF8</a>	0xF8	Reserved
	<a href="#">RWF9</a>	0xF9	Reserved
	<a href="#">RWFA</a>	0xFA	Reserved
	<a href="#">RWFB</a>	0xFB	Reserved
	<a href="#">RWFC</a>	0xFC	Reserved
	<a href="#">RWFD</a>	0xFD	Reserved
	<a href="#">RWFE</a>	0xFE	Reserved
	<a href="#">RWFF</a>	0xFF	Reserved

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

## 11.4.4 Page 4 DQ[3:0]DFE Control Word Decoding

Table 70 — Page 4 DQ[3:0]DFE Control Word Decoding

Page	Register Control Word	MR [7:0] HEX <sup>1</sup>	Meaning
0x04	RWE0 <sup>2</sup>	0xE0	DQ0 Rx DFE Gain Coefficients
	RWE1 <sup>2</sup>	0xE1	DQ0 Rx DFE Tap 1 Coefficients
	RWE2 <sup>2</sup>	0xE2	DQ0 Rx DFE Tap 2 Coefficients
	RWE3 <sup>2</sup>	0xE3	DQ0 Rx DFE Tap 3 Coefficients
	RWE4 <sup>2</sup>	0xE4	DQ0 Rx DFE Tap 4 Coefficients
	RWE5 <sup>2</sup>	0xE5	DQ0 Rx DFE Tap 5 Coefficients
	RWE6 <sup>2</sup>	0xE6	DQ0 Rx DFE Tap 6 Coefficients
	RWE7	0xE7	RFU
	RWE8 <sup>2</sup>	0xE8	DQ1 Rx DFE Gain Coefficients
	RWE9 <sup>2</sup>	0xE9	DQ1 Rx DFE Tap 1 Coefficients
	RWEA <sup>2</sup>	0xEA	DQ1 Rx DFE Tap 2 Coefficients
	RWEB <sup>2</sup>	0xEB	DQ1 Rx DFE Tap 3 Coefficients
	RWEC <sup>2</sup>	0xEC	DQ1 Rx DFE Tap 4 Coefficients
	RWED <sup>2</sup>	0xED	DQ1 Rx DFE Tap 5 Coefficients
	RWEE <sup>2</sup>	0xEE	DQ1 Rx DFE Tap 6 Coefficients
	RWEF	0xEF	RFU
	RWF0 <sup>2</sup>	0xF0	DQ2 Rx DFE Gain Coefficients
	RWF1 <sup>2</sup>	0xF1	DQ2 Rx DFE Tap 1 Coefficients
	RWF2 <sup>2</sup>	0xF2	DQ2 Rx DFE Tap 2 Coefficients
	RWF3 <sup>2</sup>	0xF3	DQ2 Rx DFE Tap 3 Coefficients
	RWF4 <sup>2</sup>	0xF4	DQ2 Rx DFE Tap 4 Coefficients
	RWF5 <sup>2</sup>	0xF5	DQ2 Rx DFE Tap 5 Coefficients
	RWF6 <sup>2</sup>	0xF6	DQ2 Rx DFE Tap 6 Coefficients
	RWF7	0xF7	RFU
	RWF8 <sup>2</sup>	0xF8	DQ3 Rx DFE Gain Coefficients
	RWF9 <sup>2</sup>	0xF9	DQ3 Rx DFE Tap 1 Coefficients
	RWFA <sup>2</sup>	0xFA	DQ3 Rx DFE Tap 2 Coefficients
	RWFB <sup>2</sup>	0xFB	DQ3 Rx DFE Tap 3 Coefficients
	RWFC <sup>2</sup>	0xFC	DQ3 Rx DFE Tap 4 Coefficients
	RWFD <sup>2</sup>	0xFD	DQ3 Rx DFE Tap 5 Coefficients
	RWFE <sup>2</sup>	0xFE	DQ3 Rx DFE Tap 6 Coefficients
	RWFF	0xFF	RFU

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

NOTE 2 Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.



## 11.4.5 Page 5 DQ[7:4] DFE Paged Control Word Decoding

Table 71 — Page 5 DQ[7:4]DFE Paged Control Word Decoding

Page	Register Control Word	MR [7:0] HEX <sup>1</sup>	Meaning
0x05	RWE0 <sup>2</sup>	0xE0	DQ4 Rx DFE Gain Coefficients
	RWE1 <sup>2</sup>	0xE1	DQ4 Rx DFE Tap 1 Coefficients
	RWE2 <sup>2</sup>	0xE2	DQ4 Rx DFE Tap 2 Coefficients
	RWE3 <sup>2</sup>	0xE3	DQ4 Rx DFE Tap 3 Coefficients
	RWE4 <sup>2</sup>	0xE4	DQ4 Rx DFE Tap 4 Coefficients
	RWE5 <sup>2</sup>	0xE5	DQ4 Rx DFE Tap 5 Coefficients
	RWE6 <sup>2</sup>	0xE6	DQ4 Rx DFE Tap 6 Coefficients
	RWE7	0xE7	RFU
	RWE8 <sup>2</sup>	0xE8	DQ5 Rx DFE Gain Coefficients
	RWE9 <sup>2</sup>	0xE9	DQ5 Rx DFE Tap 1 Coefficients
	RWEA <sup>2</sup>	0xEA	DQ5 Rx DFE Tap 2 Coefficients
	RWEB <sup>2</sup>	0xEB	DQ5 Rx DFE Tap 3 Coefficients
	RWEC <sup>2</sup>	0xEC	DQ5 Rx DFE Tap 4 Coefficients
	RWED <sup>2</sup>	0xED	DQ5 Rx DFE Tap 5 Coefficients
	RWEE <sup>2</sup>	0xEE	DQ5 Rx DFE Tap 6 Coefficients
	RWEF	0xEF	RFU
	RWF0 <sup>2</sup>	0xF0	DQ6 Rx DFE Gain Coefficients
	RWF1 <sup>2</sup>	0xF1	DQ6 Rx DFE Tap 1 Coefficients
	RWF2 <sup>2</sup>	0xF2	DQ6 Rx DFE Tap 2 Coefficients
	RWF3 <sup>2</sup>	0xF3	DQ6 Rx DFE Tap 3 Coefficients
	RWF4 <sup>2</sup>	0xF4	DQ6 Rx DFE Tap 4 Coefficients
	RWF5 <sup>2</sup>	0xF5	DQ6 Rx DFE Tap 5 Coefficients
	RWF6 <sup>2</sup>	0xF6	DQ6 Rx DFE Tap 6 Coefficients
	RWF7	0xF7	RFU
	RWF8 <sup>2</sup>	0xF8	DQ7 Rx DFE Gain Coefficients
	RWF9 <sup>2</sup>	0xF9	DQ7 Rx DFE Tap 1 Coefficients
	RWFA <sup>2</sup>	0xFA	DQ7 Rx DFE Tap 2 Coefficients
	RWFB <sup>2</sup>	0xFB	DQ7 Rx DFE Tap 3 Coefficients
	RWFC <sup>2</sup>	0xFC	DQ7 Rx DFE Tap 4 Coefficients
	RWFD <sup>2</sup>	0xFD	DQ7 Rx DFE Tap 5 Coefficients
	RWFE <sup>2</sup>	0xFE	DQ7 Rx DFE Tap 6 Coefficients
	RWFF	0xFF	RFU

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

NOTE 2 Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

### 11.4.6 Page 6 DFE\_Vref and Error Counter DFE Paged Control Word Decoding

Table 72 — Page 6 DFE\_Vref and Error Counter DFE Control Word Decoding

Page	Register Control Word	MR [7:0] HEX <sup>1</sup>	Meaning
0x06	RWE0	0xE0	DQ0 Rx DFE Error Counter Lower 8 Bits
	RWE1	0xE1	DQ0 Rx DFE Error Counter Upper 8 Bits
	RWE2	0xE2	DQ0 DFE_Vref <sup>2</sup>
	RWE3	0xE3	Sign bit DQ0 DFE_Vref
	RWE4	0xE4	DQ1 Rx DFE Error Counter Lower 8 Bits
	RWE5	0xE5	DQ1 Rx DFE Error Counter Upper 8 Bits
	RWE6	0xE6	DQ1 DFE_Vref <sup>2</sup>
	RWE7	0xE7	Sign bit DQ1 DFE_Vref
	RWE8	0xE8	DQ2 Rx DFE Error Counter Lower 8 Bits
	RWE9	0xE9	DQ2 Rx DFE Error Counter Upper 8 Bits
	RWEA	0xEA	DQ2 DFE_Vref <sup>2</sup>
	RWEB	0xEB	Sign bit DQ2 DFE_Vref
	RWEC	0xEC	DQ3 Rx DFE Error Counter Lower 8 Bits
	RWED	0xED	DQ3 Rx DFE Error Counter Upper 8 Bits
	RWEE	0xEE	DQ3 DFE_Vref <sup>2</sup>
	RWEF	0xEF	Sign bit DQ3 DFE_Vref
	RWF0	0xF0	DQ4 Rx DFE Error Counter Lower 8 Bits
	RWF1	0xF1	DQ4 Rx DFE Error Counter Upper 8 Bits
	RWF2	0xF2	DQ4 DFE_Vref <sup>2</sup>
	RWF3	0xF3	Sign bit DQ4 DFE_Vref
	RWF4	0xF4	DQ5 Rx DFE Error Counter Lower 8 Bits
	RWF5	0xF5	DQ5 Rx DFE Error Counter Upper 8 Bits
	RWF6	0xF6	DQ5 DFE_Vref <sup>2</sup>
	RWF7	0xF7	Sign bit DQ5 DFE_Vref
	RWF8	0xF8	DQ6 Rx DFE Error Counter Lower 8 Bits
	RWF9	0xF9	DQ6 Rx DFE Error Counter Upper 8 Bits
	RWFA	0xFA	DQ6 DFE_Vref <sup>2</sup>
	RWFB	0xFB	Sign bit DQ6 DFE_Vref
	RWFC	0xFC	DQ7 Rx DFE Error Counter Lower 8 Bits
	RWFD	0xFD	DQ7 Rx DFE Error Counter Upper 8 Bits
	RWFE	0xFE	DQ7 DFE_Vref <sup>2</sup>
	RWFF	0xFF	Sign bit DQ7 DFE_Vref

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

NOTE 2 Each DQ I/O has its own Margin Monitor with DFE\_Vref control.

### 11.4.7 Page 7 PS0 or {R0, R1} group MDQ Error Counters Paged Control Word Decoding

Table 73 — Page 7 PS0 or {R0, R1} group MDQ Error Counters Paged Control Word Decoding<sup>1</sup>

Page	Register Control Word	MR [7:0] HEX <sup>2</sup>	Meaning
0x07	RWE0	0xE0	MDQ0 Rx Error Counter Lower 8 Bits
	RWE1	0xE1	MDQ0 Rx Error Counter Upper 8 Bits
	RWE2	0xE2	MDQ1 Rx Error Counter Lower 8 Bits
	RWE3	0xE3	MDQ1 Rx Error Counter Upper 8 Bits
	RWE4	0xE4	MDQ2 Rx Error Counter Lower 8 Bits
	RWE5	0xE5	MDQ2 Rx Error Counter Upper 8 Bits
	RWE6	0xE6	MDQ3 Rx Error Counter Lower 8 Bits
	RWE7	0xE7	MDQ3 Rx Error Counter Upper 8 Bits
	RWE8	0xE8	MDQ4 Rx Error Counter Lower 8 Bits
	RWE9	0xE9	MDQ4 Rx Error Counter Upper 8 Bits
	RWEA	0xEA	MDQ5 Rx Error Counter Lower 8 Bits
	RWEB	0xEB	MDQ5 Rx Error Counter Upper 8 Bits
	RWEC	0xEC	MDQ6 Rx Error Counter Lower 8 Bits
	RWED	0xED	MDQ6 Rx Error Counter Upper 8 Bits
	RWEE	0xEE	MDQ7 Rx Error Counter Lower 8 Bits
	RWEF	0xEF	MDQ7 Rx Error Counter Upper 8 Bits
	RWF0	0xF0	Error Counter Reset
	RWF1	0xF1	Reserved
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 Read-only register for MDQ Error Counters

NOTE 2 [MRA7](#) must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

### 11.4.8 Page 8 MR Snooped Settings Paged Control Word Decoding

Upon receiving a DRAM MR command, the DDR5 MRCD snoops relevant bits that are needed by the MDB for its operation and sends them to the MDB via an MRS Write command over the BCOM bus. The data buffer stores these bit settings in DB-space MRWs. The stored snooped MR settings can be read by means of MRR commands. The MRW command can be used to program these settings directly and override the results of any prior MR snooping.

**Table 74 — Page 8 MR Snooped Setting Paged Control Word Decoding**

Page	Register Control Word	MR [7:0] HEX <sup>1</sup>	Meaning
0x08	RWE0	0xE0	BL and CL MR0
	RWE1	0xE1	Dram Interface Read and write pre-amble and post-amble settings MR8
	RWE2	0xE2	Read training pattern mode settings MR25
	RWE3	0xE3	PS0 or {R0, R1} group Read training pattern Data0/LFSR0 setting MR26
	RWE4	0xE4	PS0 or {R0, R1} group Read training pattern Data1/LFSR1 setting MR27
	RWE5	0xE5	PS0 or {R0, R1} group Read training pattern invert DQL MR28
	RWE6	0xE6	PS0 or {R0, R1} group Read LFSR assignment MR30 MR30
	RWE7	0xE7	DQS Interval Timer Run Time MR45
	RWE8	0xE8	Read and Write CRC enable MR50[2:0]
	RWE9	0xE9	PS1 or {R2, R3} group Read training pattern Data0/LFSR0 setting MR26
	RWEA	0xEA	PS1 or {R2, R3} group Read training pattern Data1/LFSR1 setting MR27
	RWEB	0xEB	PS1 or {R2, R3} group Read training pattern invert DQL MR28
	RWEC	0xEC	PS1 or {R2, R3} group Read LFSR assignment MR30
	RWED	0xED	Host Interface Read and write pre-amble and post-amble settings MR8
	RWEE	0xEE	Reserved
	RWEF	0xEF	Reserved
	RWF0	0xF0	Reserved
	RWF1	0xF1	Reserved
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 [MRA7](#) must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

### 11.4.9 Page 9 DFE Training Accelerator Paged Control Word Decoding

Table 75 — Page 9 DFE Training Accelerator Paged Control Word Decoding

Page	Register Control Word	MR [7:0] HEX <sup>1</sup>	Meaning
0x09	RWE0	0xE0	DFETA Training Mode
	RWE1	0xE1	DFETA Inner Loop Start Value [7:0]
	RWE2	0xE2	DFETA Inner Loop Start Value, Bit [8]
	RWE3	0xE3	DFETA Outer Loop Start Value
	RWE4	0xE4	DFETA Inner Loop Current Value, Bit [7:0]
	RWE5	0xE5	DFETA Inner Loop Current Value, Bit [8]
	RWE6	0xE6	DFETA Outer Loop Current Value
	RWE7	0xE7	DFETA Inner and Outer Loop Step Size
	RWE8	0xE8	DFETA Inner Loop Number of Increments, Bit [7:0]
	RWE9	0xE9	DFETA Inner Loop Number of Increments, Bit [8]
	RWEA	0xEA	DFETA Outer Loop Number of Increments
	RWEB	0xEB	DFETA Inner Loop Current Increment, Bit [7:0]
	RWEC	0xEC	DFETA Inner Loop Current Increment, Bit [8]
	RWED	0xED	DFETA Outer Loop Current Increment
	RWEE	0xEE	DFETA Write Limit Value - Lower Byte
	RWEF	0xEF	DFETA Write Limit Value - Upper Byte
	RWF0	0xF0	DFETA Write Limit Counter Value Status - Lower Byte
	RWF1	0xF1	DFETA Write Limit Counter Value Status - Upper Byte
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 [MRA7](#) must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

### 11.4.10 Page A Periodic Update PS0 Paged Control Word Decoding

**Table 76 — Page A Periodic Update PS0 Paged Control Word Decoding<sup>1</sup>**

Page	Register Control Word	MR [7:0] HEX <sup>2</sup>	Meaning
0x0A	RWE0	0xE0	Lower-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter LSB
	RWE1	0xE1	Lower-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter MSB
	RWE2	0xE2	Lower-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter LSB
	RWE3	0xE3	Lower-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter MSB
	RWE4	0xE4	Upper-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter LSB
	RWE5	0xE5	Upper-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter MSB
	RWE6	0xE6	Upper-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter LSB
	RWE7	0xE7	Upper-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter MSB
	RWE8	0xE8	Lower-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay LSB
	RWE9	0xE9	Lower-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay MSB
	RWEA	0xEA	Lower-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay LSB
	RWEB	0xEB	Lower-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay MSB
	RWEC	0xEC	Upper-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay LSB
	RWED	0xED	Upper-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay MSB
	RWEE	0xEE	Upper-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay LSB
	RWEF	0xEF	Upper-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay MSB
	RWF0	0xF0	Lower-Nibble, Rank-0 Current DRAM DQS Oscillator Counter LSB
	RWF1	0xF1	Lower-Nibble, Rank-0 Current DRAM DQS Oscillator Counter MSB
	RWF2	0xF2	Lower-Nibble, Rank-1 Current DRAM DQS Oscillator Counter LSB
	RWF3	0xF3	Lower-Nibble, Rank-1 Current DRAM DQS Oscillator Counter MSB
	RWF4	0xF4	Upper-Nibble, Rank-0 Current DRAM DQS Oscillator Counter LSB
	RWF5	0xF5	Upper-Nibble, Rank-0 Current DRAM DQS Oscillator Counter MSB
	RWF6	0xF6	Upper-Nibble, Rank-1 Current DRAM DQS Oscillator Counter LSB
	RWF7	0xF7	Upper-Nibble, Rank-1 Current DRAM DQS Oscillator Counter MSB
	RWF8	0xF8	Lower-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay LSB
	RWF9	0xF9	Lower-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay MSB
	RWFA	0xFA	Lower-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay LSB
	RWFB	0xFB	Lower-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay MSB
	RWFC	0xFC	Upper-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay LSB
	RWFD	0xFD	Upper-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay MSB
	RWFE	0xFE	Upper-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay LSB
	RWFF	0xFF	Upper-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay MSB

NOTE 1 In the Mux mode, PG[A] control words are used for rank 0 and rank 1 of PS0. In the Rank mode, PG[A] control words are used for rank 0 and rank 1.

NOTE 2 [MRA7](#) must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

### 11.4.11 Page C Duty Cycle Adjuster Control Word Decoding

Table 77 — Page C DCA Control Word Decoding

Page	Register Control Word	MRA [7:0] HEX <sup>1</sup>	Meaning
0x0C	RWE0	0xE0	DCA Configuration (Read-Only)
	RWE1	0xE1	Lower Nibble DQS0 DCA Adjustment
	RWE2	0xE2	Lower Nibble DQ[3:0] DCA Adjustment <sup>2,3</sup>
	RWE3	0xE3	Upper Nibble DQS1 DCA Adjustment <sup>4</sup>
	RWE4	0xE4	Upper Nibble DQ[7:4] DCA Adjustment <sup>2,3</sup>
	RWE5	0xE5	Reserved
	RWE6	0xE6	Reserved
	RWE7	0xE7	Reserved
	RWE8	0xE8	Reserved
	RWE9	0xE9	Reserved
	RWEA	0xEA	Reserved
	RWEB	0xEB	Reserved
	RWEC	0xEC	Reserved
	RWED	0xED	Reserved
	RWEE	0xEE	Reserved
	RWEF	0xEF	Reserved
	RWF0	0xF0	Per-Pin DQS0_t DCA Adjustment <sup>2</sup>
	RWF1	0xF1	Per-Pin DQS0_c DCA Adjustment <sup>2</sup>
	RWF2	0xF2	Per-Pin DQ0 DCA Adjustment
	RWF3	0xF3	Per-Pin DQ1 DCA Adjustment
	RWF4	0xF4	Per-Pin DQ2 DCA Adjustment
	RWF5	0xF5	Per-Pin DQ3 DCA Adjustment
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Per-Pin DQS1_t DCA Adjustment <sup>2,4</sup>
	RWF9	0xF9	Per-Pin DQS1_c DCA Adjustment <sup>2,4</sup>
	RWFA	0xFA	Per-Pin DQ4 DCA Adjustment
	RWFB	0xFB	Per-Pin DQ5 DCA Adjustment
	RWFC	0xFC	Per-Pin DQ6 DCA Adjustment
	RWFD	0xFD	Per-Pin DQ7 DCA Adjustment
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for MDB Control Words accesses.

NOTE 2 This register has no function when PG[C]RWE0[0] = 1.

NOTE 3 PG[C]RWE2 and PG[C]RWE4 must be set to the same value when PG[C]RWE0[0] = 0 and the Host Strobe Mode is x8 with PG[70]RWF0[1] set.

NOTE 4 This register has no function when the Host Strobe Mode is x8 with PG[70]RWF0[1] set.

## 11.4.12 Page D Rx CTLE for DQ Control Word Decoding

Table 78 — Page D Rx CTLE for DQ Control Word Decoding

Page	Register Control Word	MRA [7:0] HEX <sup>1</sup>	Meaning
0x0D	RWE0	0xE0	Rx CTLE for DQ Control
	RWE1	0xE1	Per-Pin CTLE Disable Control for DQ[7:0]
	RWE2	0xE2	CTLE Disable Control for DQS1 as CRC
	RWE3	0xE3	Reserved
	RWE4	0xE4	Reserved
	RWE5	0xE5	Reserved
	RWE6	0xE6	Reserved
	RWE7	0xE7	Reserved
	RWE8	0xE8	Reserved
	RWE9	0xE9	Reserved
	RWEA	0xEA	Reserved
	RWEB	0xEB	Reserved
	RWEC	0xEC	Reserved
	RWED	0xED	Reserved
	RWEE	0xEE	Reserved
	RWEF	0xEF	Reserved
	RWF0	0xF0	Rx CTLE setting for DQ0
	RWF1	0xF1	Rx CTLE setting for DQ1
	RWF2	0xF2	Rx CTLE setting for DQ2
	RWF3	0xF3	Rx CTLE setting for DQ3
	RWF4	0xF4	Rx CTLE setting for DQ4
	RWF5	0xF5	Rx CTLE setting for DQ5
	RWF6	0xF6	Rx CTLE setting for DQ6
	RWF7	0xF7	Rx CTLE setting for DQ7
	RWF8	0xF8	Rx CTLE setting for DQS1 as CRC
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.



## 11.4.13 Page F - DESTM and CRC DFE Control Word Decoding

Table 79 — Page F - DESTM and CRC DFE Control Word Decoding

Page	Register Control Word	MRA [7:0] HEX <sup>1</sup>	Meaning
0x0F	RWE0	0xE0	DESTM Control Word
	RWE1	0xE1	Reserved
	RWE2	0xE2	DESTM CTLE and DFE Select
	RWE3	0xE3	DESTM DQS1 as CRC Select and Status
	RWE4	0xE4	DESTM DQ Select
	RWE5	0xE5	DESTM DQ Status
	RWE6	0xE6	Reserved
	RWE7	0xE7	Reserved
	RWE8	0xE8	Reserved
	RWE9	0xE9	Reserved
	RWEA	0xEA	Reserved
	RWEB	0xEB	Reserved
	RWEC	0xEC	Reserved
	RWED	0xED	Reserved
	RWEE	0xEE	Reserved
	RWEF	0xEF	Reserved
	RWF0	0xF0	CRC DFE Coefficient and Sign, Tap 1
	RWF1	0xF1	CRC DFE Coefficient and Sign, Tap 2
	RWF2	0xF2	CRC DFE Coefficient and Sign, Tap 3
	RWF3	0xF3	CRC DFE Coefficient and Sign, Tap 4
	RWF4	0xF4	CRC DFE Coefficient and Sign, Tap 5
	RWF5	0xF5	CRC DFE Coefficient and Sign, Tap 6
	RWF6	0xF6	CRC DFE Coefficient and Sign, Tap 7
	RWF7	0xF7	CRC DFE Coefficient and Sign, Tap 8
	RWF8	0xF8	CRC DFE Gain Coefficient
	RWF9	0xF9	CRC DFE Vref
	RWFA	0xFA	CRC DFE Vref Sign
	RWFB	0xFB	CRC Rx DFE Error Counter Lower 8 Bits
	RWFC	0xFC	CRC Rx DFE Error Counter Upper 8 Bits
	RWFD	0xFD	CRC DFE Tap Enable for DQS1
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

## 11.4.14 Page 10 Enhanced Training Control Word Decoding

Table 80 — Page 10 Enhanced Training Control Word Decoding

Page	Register Control Word	MR [7:0] HEX <sup>1</sup>	Meaning
0x10	RWE0	0xE0	Host Interface Error Counter Status 0-7
	RWE1	0xE1	Host Interface Error Counter Status 8-15
	RWE2	0xE2	Host Interface Error Counter Status 16-23
	RWE3	0xE3	Host Interface Error Counter Status 24- 31
	RWE4	0xE4	Reserved
	RWE5	0xE5	Reserved
	RWE6	0xE6	Reserved
	RWE7	0xE7	Reserved
	RWE8	0xE8	Reserved
	RWE9	0xE9	Reserved
	RWEA	0xEA	CRC (DQS1) UI Error Status
	RWEB	0xEB	DQ0/DQ1 UI Error Status
	RWEC	0xEC	DQ2/DQ3 UI Error Status
	RWED	0xED	DQ4/DQ5 UI Error Status
	RWEE	0xEE	DQ6/DQ7 UI Error Status
	RWEF	0xEF	Reserved
	RWF0	0xF0	CRC Training Global Control Status Clear
	RWF1	0xF1	Pattern Control
	RWF2	0xF2	Reserved
	RWF3	0xF3	Read error detect threshold (5-bit)
	RWF4	0xF4	Error mask for DQ lanes
	RWF5	0xF5	Error mask for CRC lanes
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	PS0 16-bit UI mask Lower
	RWF9	0xF9	PS0 16-bit UI mask Upper
	RWFA	0xFA	PS1 16-bit UI mask Lower
	RWFB	0xFB	PS1 16-bit UI mask Upper
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

#### 11.4.15 Page 11 PS0 16-bit LFSR Seed Control Word Decoding

Table 81 — Page 11 PS0 16-bit LFSR Seed Control Word Decoding

Page	Register Control Word	MR [7:0] HEX <sup>1</sup>	Meaning
0x11	RWE0	0xE0	DQ0 LFSR Seed Lower Byte
	RWE1	0xE1	DQ0 LFSR Seed Upper Byte
	RWE2	0xE2	DQ1 LFSR Seed Lower Byte
	RWE3	0xE3	DQ1 LFSR Seed Upper Byte
	RWE4	0xE4	DQ2 LFSR Seed Lower Byte
	RWE5	0xE5	DQ2 LFSR Seed Upper Byte
	RWE6	0xE6	DQ3 LFSR Seed Lower Byte
	RWE7	0xE7	DQ3 LFSR Seed Upper Byte
	RWE8	0xE8	DQ4 LFSR Seed Lower Byte
	RWE9	0xE9	DQ4 LFSR Seed Upper Byte
	RWEA	0xEA	DQ5 LFSR Seed Lower Byte
	RWEB	0xEB	DQ5 LFSR Seed Upper Byte
	RWEC	0xEC	DQ6 LFSR Seed Lower Byte
	RWED	0xED	DQ6 LFSR Seed Upper Byte
	RWEE	0xEE	DQ7 LFSR Seed Lower Byte
	RWEF	0xEF	DQ7; LFSR Seed Upper Byte
	RWF0	0xF0	DQS1 LFSR Seed Lower Byte
	RWF1	0xF1	DQS1 LFSR Seed Upper Byte
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

## 11.4.16 Page 12 PS0 16-bit LFSR Training Status Control Word Decoding

Table 82 — Page 12 PS0 16-bit LFSR Training Status Control Word Decoding

Page	Register Control Word	MR [7:0] HEX <sup>1</sup>	Meaning
0x12	RWE0	0xE0	DQ0 LFSR Lower Byte Status
	RWE1	0xE1	DQ0 LFSR Upper Byte Status
	RWE2	0xE2	DQ1 LFSR Lower Byte Status
	RWE3	0xE3	DQ1 LFSR Upper Byte Status
	RWE4	0xE4	DQ2 LFSR Lower Byte Status
	RWE5	0xE5	DQ2 LFSR Upper Byte Status
	RWE6	0xE6	DQ3 LFSR Lower Byte Status
	RWE7	0xE7	DQ3 LFSR Upper Byte Status
	RWE8	0xE8	DQ4 LFSR Lower Byte Status
	RWE9	0xE9	DQ4 LFSR Upper Byte Status
	RWEA	0xEA	DQ5 LFSR Lower Byte Status
	RWEB	0xEB	DQ5 LFSR Upper Byte Status
	RWEC	0xEC	DQ6 LFSR Lower Byte Status
	RWED	0xED	DQ6 LFSR Upper Byte Status
	RWEE	0xEE	DQ7 LFSR Lower Byte Status
	RWEF	0xEF	DQ7 LFSR Upper Byte Status
	RWF0	0xF0	DQS1 LFSR Lower Byte Status
	RWF1	0xF1	DQS1 LFSR Upper Byte Status
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 [MRA7](#) must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

## 11.4.17 Page 13 PS1 16-bit LFSR Seed Control Word Decoding

Table 83 — Page 13 PS1 16-bit LFSR Seed Control Word Decoding

Page	Register Control Word	MR [7:0] HEX <sup>1</sup>	Meaning
0x13	RWE0	0xE0	DQ0 LFSR Seed Lower Byte
	RWE1	0xE1	DQ0 LFSR Seed Upper Byte
	RWE2	0xE2	DQ1 LFSR Seed Lower Byte
	RWE3	0xE3	DQ1 LFSR Seed Upper Byte
	RWE4	0xE4	DQ2 LFSR Seed Lower Byte
	RWE5	0xE5	DQ2 LFSR Seed Upper Byte
	RWE6	0xE6	DQ3 LFSR Seed Lower Byte
	RWE7	0xE7	DQ3 LFSR Seed Upper Byte
	RWE8	0xE8	DQ4 LFSR Seed Lower Byte
	RWE9	0xE9	DQ4 LFSR Seed Upper Byte
	RWEA	0xEA	DQ5 LFSR Seed Lower Byte
	RWEB	0xEB	DQ5 LFSR Seed Upper Byte
	RWEC	0xEC	DQ6 LFSR Seed Lower Byte
	RWED	0xED	DQ6 LFSR Seed Upper Byte
	RWEE	0xEE	DQ7 LFSR Seed Lower Byte
	RWEF	0xEF	DQ7 LFSR Seed Upper Byte
	RWF0	0xF0	DQS1 LFSR Seed Lower Byte
	RWF1	0xF1	DQS1 LFSR Seed Upper Byte
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 [MRA7](#) must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

## 11.4.18 Page 14 PS1 16-bit LFSR Status Control Word

Table 84 — Page 14 PS1 16-bit LFSR Status Control Word Decoding

Page	Register Control Word	MR [7:0] HEX <sup>1</sup>	Meaning
0x14	RWE0	0xE0	DQ0 LFSR Lower Byte Status
	RWE1	0xE1	DQ0 LFSR Upper Byte Status
	RWE2	0xE2	DQ1 LFSR Lower Byte Status
	RWE3	0xE3	DQ1 LFSR Upper Byte Status
	RWE4	0xE4	DQ2 LFSR Lower Byte Status
	RWE5	0xE5	DQ2 LFSR Upper Byte Status
	RWE6	0xE6	DQ3 LFSR Lower Byte Status
	RWE7	0xE7	DQ3 LFSR Upper Byte Status
	RWE8	0xE8	DQ4 LFSR Lower Byte Status
	RWE9	0xE9	DQ4 LFSR Upper Byte Status
	RWEA	0xEA	DQ5 LFSR Lower Byte Status
	RWEB	0xEB	DQ5 LFSR Upper Byte Status
	RWEC	0xEC	DQ6 LFSR Lower Byte Status
	RWED	0xED	DQ6 LFSR Upper Byte Status
	RWEE	0xEE	DQ7 LFSR Lower Byte Status
	RWEF	0xEF	DQ7 LFSR Upper Byte Status
	RWF0	0xF0	DQS1 LFSR Lower Byte Status
	RWF1	0xF1	DQS1 LFSR Upper Byte Status
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

## 11.5 Specific Registers

### 11.5.1 Page 60 Miscellaneous Rank Mode Control Word Decoding

Table 85 — Page 60 Miscellaneous Rank Mode Control Word Decoding <sup>1</sup>

Page	Register Control Word	MRA [7:0] HEX <sup>2</sup>	Meaning
0x60	RWE0 <sup>3</sup>	0xE0	MDB Rank Mode Global Control Word
	RWE1	0xE1	Reserved
	RWE2 <sup>3</sup>	0xE2	Reserved
	RWE3 <sup>3</sup>	0xE3	Reserved
	RWE4	0xE4	MDB Rank Mode Training Control Word
	RWE5	0xE5	Reserved
	RWE6	0xE6	Reserved
	RWE7	0xE7	Reserved
	RWE8 <sup>3</sup>	0xE8	Reserved
	RWE9	0xE9	Reserved
	RWEA	0xEA	Reserved
	RWEB	0xEB	Reserved
	RWEC	0xEC	Reserved
	RWED	0xED	Reserved
	RWEE	0xEE	Reserved
	RWEF	0xEF	Reserved
	RWF0	0xF0	Reserved
	RWF1	0xF1	Reserved
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 The Data Path Training modes are performed with Fixed BL16

NOTE 2 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

NOTE 3 Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

## 11.5.2 Page 70 Miscellaneous Control Word Decoding

Table 86 — Page 70 Miscellaneous Control Word Decoding <sup>1</sup>

Page	Register Control Word	MRA [7:0] HEX <sup>2</sup>	Meaning
0x70	RWE0 <sup>3</sup>	0xE0	MDB Global Features
	RWE1	0xE1	DRAM Interface Receiver Type
	RWE2 <sup>3</sup>	0xE2	Host Interface DQS Driver Control Word
	RWE3 <sup>3</sup>	0xE3	DRAM Interface MDQS Driver Control Word
	RWE4	0xE4	MDB Training Mode
	RWE5	0xE5	Static Mux select for DQ Pass Through
	RWE6	0xE6	Static Mode data
	RWE7	0xE7	Reserved
	RWE8 <sup>3</sup>	0xE8	DFE Taps 5, 6, 7 and 8 enables
	RWE9	0xE9	Reserved
	RWEA	0xEA	Reserved
	RWEB	0xEB	Reserved
	RWEC	0xEC	Current State of Read LFSR0 - PS1 or {R2, R3} group
	RWED	0xED	Current State of Read LFSR1 - PS1 or {R2, R3} group
	RWEE	0xEE	Current State of Write LFSR0 - PS1 or {R2, R3} group
	RWEF	0xEF	Current State of Write LFSR1 - PS1 or {R2, R3} group
	RWF0	0xF0	DQS / MDQS Strobe Mode
	RWF1	0xF1	Reserved
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Extended Read Preamble and 1.5-cycle Postamble Modes
	RWF5	0xF5	Extended Write Preamble Modes
	RWF6	0xF6	Continuous DQS Toggle Mode
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Programmable Read Delay
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 The Data Path Training modes are performed with Fixed BL16

NOTE 2 MRA7 must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

NOTE 3 Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.



### 11.5.3 Page 71 Periodic Update PS1 Paged Control Word Decoding

**Table 87 — Page 71 Periodic Update PS1 Paged Control Word Decoding<sup>1</sup>**

Page	Register Control Word	MR [7:0] HEX <sup>2</sup>	Meaning
0x71	RWE0	0xE0	Lower-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter LSB
	RWE1	0xE1	Lower-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter MSB
	RWE2	0xE2	Lower-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter LSB
	RWE3	0xE3	Lower-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter MSB
	RWE4	0xE4	Upper-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter LSB
	RWE5	0xE5	Upper-Nibble, Rank-0 Initial DRAM DQS Oscillator Counter MSB
	RWE6	0xE6	Upper-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter LSB
	RWE7	0xE7	Upper-Nibble, Rank-1 Initial DRAM DQS Oscillator Counter MSB
	RWE8	0xE8	Lower-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay LSB
	RWE9	0xE9	Lower-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay MSB
	RWEA	0xEA	Lower-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay LSB
	RWEB	0xEB	Lower-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay MSB
	RWEC	0xEC	Upper-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay LSB
	RWED	0xED	Upper-Nibble, Rank-0 Initial DRAM DQS Clock Tree Delay MSB
	RWEE	0xEE	Upper-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay LSB
	RWEF	0xEF	Upper-Nibble, Rank-1 Initial DRAM DQS Clock Tree Delay MSB
	RWF0	0xF0	Lower-Nibble, Rank-0 Current DRAM DQS Oscillator Counter LSB
	RWF1	0xF1	Lower-Nibble, Rank-0 Current DRAM DQS Oscillator Counter MSB
	RWF2	0xF2	Lower-Nibble, Rank-1 Current DRAM DQS Oscillator Counter LSB
	RWF3	0xF3	Lower-Nibble, Rank-1 Current DRAM DQS Oscillator Counter MSB
	RWF4	0xF4	Upper-Nibble, Rank-0 Current DRAM DQS Oscillator Counter LSB
	RWF5	0xF5	Upper-Nibble, Rank-0 Current DRAM DQS Oscillator Counter MSB
	RWF6	0xF6	Upper-Nibble, Rank-1 Current DRAM DQS Oscillator Counter LSB
	RWF7	0xF7	Upper-Nibble, Rank-1 Current DRAM DQS Oscillator Counter MSB
	RWF8	0xF8	Lower-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay LSB
	RWF9	0xF9	Lower-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay MSB
	RWFA	0xFA	Lower-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay LSB
	RWFB	0xFB	Lower-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay MSB
	RWFC	0xFC	Upper-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay LSB
	RWFD	0xFD	Upper-Nibble, Rank-0 Current DRAM DQS Clock Tree Delay MSB
	RWFE	0xFE	Upper-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay LSB
	RWFF	0xFF	Upper-Nibble, Rank-1 Current DRAM DQS Clock Tree Delay MSB

NOTE 1 In the Mux mode, PG[71] control words are used for rank 0 and rank 1 of PS1. In the Rank mode, the PG[71] “Rank-0” related control words are used for rank 2, and the PG[71] “Rank-1” related control words are used for rank 3.

NOTE 2 [MRA7](#) must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

### 11.5.4 Page 74 Error Counters Paged Control Word Decoding

**Table 88 — Page 74 MDQ PS1 or {R2, R3} Group Error Counters Paged Control Word Decoding<sup>1</sup>**

Page	Register Control Word	MR [7:0] HEX <sup>2</sup>	Meaning
0x74	RWE0	0xE0	MDQ0 Rx Error Counter Lower 8 Bits
	RWE1	0xE1	MDQ0 Rx Error Counter Upper 8 Bits
	RWE2	0xE2	MDQ1 Rx Error Counter Lower 8 Bits
	RWE3	0xE3	MDQ1 Rx Error Counter Upper 8 Bits
	RWE4	0xE4	MDQ2 Rx Error Counter Lower 8 Bits
	RWE5	0xE5	MDQ2 Rx Error Counter Upper 8 Bits
	RWE6	0xE6	MDQ3 Rx Error Counter Lower 8 Bits
	RWE7	0xE7	MDQ3 Rx Error Counter Upper 8 Bits
	RWE8	0xE8	MDQ4 Rx Error Counter Lower 8 Bits
	RWE9	0xE9	MDQ4 Rx Error Counter Upper 8 Bits
	RWEA	0xEA	MDQ5 Rx Error Counter Lower 8 Bits
	RWEB	0xEB	MDQ5 Rx Error Counter Upper 8 Bits
	RWEC	0xEC	MDQ6 Rx Error Counter Lower 8 Bits
	RWED	0xED	MDQ6 Rx Error Counter Upper 8 Bits
	RWEE	0xEE	MDQ7 Rx Error Counter Lower 8 Bits
	RWEF	0xEF	MDQ7 Rx Error Counter Upper 8 Bits
	RWF0	0xF0	Reserved
	RWF1	0xF1	Reserved
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	Reserved
	RWF5	0xF5	Reserved
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	Reserved
	RWF9	0xF9	Reserved
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	Reserved
	RWFD	0xFD	Reserved
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 Read-only register for MDQ Error Counters

NOTE 2 [MRA7](#) must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

### 11.5.5 Page 7B DQ[7:0] DFE Tap 7 and 8 Control Word Decoding

**Table 89 — Page 7B DQ[7:0] DFE Tap 7 and 8 Control Word Decoding<sup>1</sup>**

Page	Register Control Word	MR [7:0] HEX <sup>2</sup>	Meaning
0x7B	RWE0	0xE0	DQ0 Rx DFE Tap 7 Coefficients
	RWE1	0xE1	DQ0 Rx DFE Tap 8 Coefficients
	RWE2	0xE2	Reserved
	RWE3	0xE3	Reserved
	RWE4	0xE4	DQ1 Rx DFE Tap 7 Coefficients
	RWE5	0xE5	DQ1 Rx DFE Tap 8 Coefficients
	RWE6	0xE6	Reserved
	RWE7	0xE7	Reserved
	RWE8	0xE8	DQ2 Rx DFE Tap 7 Coefficients
	RWE9	0xE9	DQ2 Rx DFE Tap 8 Coefficients
	RWEA	0xEA	Reserved
	RWEB	0xEB	Reserved
	RWEC	0xEC	DQ3 Rx DFE Tap 7 Coefficients
	RWED	0xED	DQ3 Rx DFE Tap 8 Coefficients
	RWEE	0xEE	Reserved
	RWEF	0xEF	Reserved
	RWF0	0xF0	DQ4 Rx DFE Tap 7 Coefficients
	RWF1	0xF1	DQ4 Rx DFE Tap 8 Coefficients
	RWF2	0xF2	Reserved
	RWF3	0xF3	Reserved
	RWF4	0xF4	DQ5 Rx DFE Tap 7 Coefficients
	RWF5	0xF5	DQ5 Rx DFE Tap 8 Coefficients
	RWF6	0xF6	Reserved
	RWF7	0xF7	Reserved
	RWF8	0xF8	DQ6 Rx DFE Tap 7 Coefficients
	RWF9	0xF9	DQ6 Rx DFE Tap 8 Coefficients
	RWFA	0xFA	Reserved
	RWFB	0xFB	Reserved
	RWFC	0xFC	DQ7 Rx DFE Tap 7 Coefficients
	RWFD	0xFD	DQ7 Rx DFE Tap 8 Coefficients
	RWFE	0xFE	Reserved
	RWFF	0xFF	Reserved

NOTE 1 [MRA7](#) must be 0 for MRCD accesses and must be 1 for Data Buffer (MDB) Control Words accesses.

NOTE 2 Control Word contains sticky bits, some or all cleared by power cycle not reset, see specific control word definition for details.

## 11.6 Sticky Bits

### 11.6.1 Direct Control Words

1. [RW80\[2:1\]](#): Low Nibble/Upper Nibble disable
2. [RW80\[5:4\]](#): R1/R0 disable
3. [RW81\[4:3\]](#): R3/R2 disable
4. [RW84\[6\]](#): Context for operation training
5. [RW84\[4:0\]](#): DIMM Operating Speed
6. [RW85\[4:0\]](#): Fine Granularity DIMM Operating Speed
7. [RW86\[7:4, 2:0\]](#): DQS RTT Park Termination
8. [RW87\[2:0\]](#): Host Interface DQ RTT Termination
9. [RW8A\[6:0\]](#): Host Interface DQ Driver
10. [RW8B\[6:0\]](#): DRAM Interface MDQ Driver
11. [RW8C\[5:0\]](#): DRAM Interface MDQ Driver
12. [RW8F\[3:0\]](#): Host Interface DQS0 Pre-launch
13. [RW8F\[7:4\]](#): Host Interface DQS1 Pre-launch
14. [RW92\[3:0\]](#): PBA Enumerate ID
15. [RW93\[3:0\]](#): PBA Buffer Select ID
16. [RWA0\[7:0\]](#): DFE Feature ENB/DFE\_Vref ENB/ERROR Counter ENB/Broadcast ENB/tap1/2/3/4 ENB
17. [RWB0\[0\]](#): DRAM tDQS2DQ Tracking
18. [RWB1\[7:0\]](#): DRAM tDQS2DQ Tracking Return Value

### 11.6.2 Paged Control Words

1. [PG\[73,72,1,0\]RW\[F1:E0\]OP\[7:0\]](#): Additional Cycles of DRAM Interface Write Leveling/DRAM interface receive enable/MDQS read delay control/MDQ Write Baseline Delay/DRAM interface write leveling/per pin RD-delay/per pin WR-delay
2. [PG\[2\]RW\[E7:E0\]OP\[7:0\]](#): Host Interface Internal per pin VrefDQ
3. [PG\[2\]RW\[F3:F0\]OP\[7:0\]](#): DRAM Interface Internal per nibble VrefMDQ
4. [PG\[5:4\]RW\[E1,E9,F1,F9\]OP\[7:0\]](#): tap1
5. [PG\[5:4\]RW\[E2,EA,F2,FA\]OP\[7:0\]](#): tap2
6. [PG\[5:4\]RW\[E3,EB,F3,FB\]OP\[7:0\]](#): tap3
7. [PG\[5:4\]RW\[E4,EC,F4,FC\]OP\[7:0\]](#): tap4
8. [PG\[5:4\]RW\[E5,ED,F5,FD\]OP\[7:0\]](#): tap5
9. [PG\[5:4\]RW\[E6,EE,F6,FE\]OP\[7:0\]](#): tap6
10. [PG\[7B\]RW\[E0,E4,E8,EC,F0,F4,F8,FC\]OP\[7:0\]](#): tap7
11. [PG\[7B\]RW\[E1,E5,E9,ED,F1,F5,F9,FD\]OP\[7:0\]](#): tap8
12. [PG\[5:4\]RW\[E0,E8,F0,F8\]OP\[7:0\]](#): gain offset
13. [PG\[8\]RWE7](#): DQS Interval Timer Runtime MR45
14. [PG\[71,A\]RW\[FF:E0\]](#): Periodic Update PS0 and PS1
15. [PG\[C\]RW\[FD:F8, F5:F0, E4:E1\]](#): Per-nibble and per-bit DCA Adjustments
16. [PG\[D\]RWE0\[1:0\]](#), [PG\[D\]RWE1\[7:0\]](#), [PG\[D\]RWE2\[0\]](#), [PG\[D\]RW\[F8:F0\]](#): Rx CTLE Control
17. [PG\[F\]RW\[FD,F8:F0\]](#): CRC lane DFE tap 1~8 control
18. [PG\[60\]RWE0\[0\]](#): Rank operating mode
19. [PG\[70\]RWE0\[7,3:0\]](#): Mux operating Mode and CRC control
20. [PG\[70\]RW\[E2, E3\]](#): Host Interface DQS output driver, DRAM Interface MDQS output driver
21. [PG\[70\]RWE8\[3:0\]](#): Tap 5/6/7/8 Enable
22. [PG\[70\]RWF0\[1:0\]](#): DQS/MDQS Strobe Mode
23. [PG\[70\]RWF9\[7, 3:0\]](#): Programmable Read Delay

## 11.7 Mode Control Words

### 11.7.1 RW80 - Features Control Word

Table 90 — RW80: Features Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DNU	DNU
x	x	x	x	x	x	x	1		DNU
x	x	x	x	x	x	0	x	Low Nibble I/O buffer Disable <sup>2,3</sup>	Enable
x	x	x	x	x	x	1	x		Disable <sup>4,5</sup>
x	x	x	x	x	0	x	x	Upper Nibble I/O buffer	Enable
x	x	x	x	x	1	x	x	Disable <sup>2,6</sup>	Disable <sup>3</sup>
x	x	x	x	0	x	x	x	Lockout Protection Enable <sup>7</sup>	No effect <sup>8</sup>
x	x	x	x	1	x	x	x		Protection enabled <sup>9</sup>
x	x	x	0	x	x	x	x	Rank0 Present <sup>10</sup>	(Default) Package Rank 0 Enabled
x	x	x	1	x	x	x	x		Package Rank 0 Disabled <sup>11</sup>
x	x	0	x	x	x	x	x	Rank 1 Present <sup>9</sup>	(Default) Package Rank 1 Enabled
x	x	1	x	x	x	x	x		Package Rank 1 Disabled <sup>12</sup>
x	0	x	x	x	x	x	x	DNU	DNU
x	1	x	x	x	x	x	x		DNU
0	x	x	x	x	x	x	x	DNU	DNU
1	x	x	x	x	x	x	x		DNU

NOTE 1 RW80[7], RW80[5:4] and RW80[2:1] will be sticky, cleared by power cycle not reset.

NOTE 2 Nibble Enable/Disable configuration applies to both PS0 and PS1 in Mux mode, or both rank groups in Rank mode. When either Host or DRAM side is configured in x8 mode, both Nibbles must be enabled.

NOTE 3 When this bit is set [M]DQS0\_t, [M]DQS0\_c, [M]DQ[3:0] are disabled.

NOTE 4 Disable does not affect buffer control words, or the BCOM programming of buffer control words

NOTE 5 Per Buffer and Per DRAM Enumeration must be completed before disabling either nibble's I/O buffers

NOTE 6 When this bit is set [M]DQS1\_t, [M]DQS1\_c, [M]DQ[7:4] are disabled.

NOTE 7 This feature is intended to protect the Data Buffer against lockout state that is unrecoverable with BRST\_n Reset and is caused by invalid BCOM commands associated with incorrect input signal voltage levels or timing.

NOTE 8 This control bit is type "Write-1 Only" and cannot be written to 0 by the user. It only gets cleared to zero by BRST\_n Reset or by internal Power-On Reset.

NOTE 9 When OP[3] = 1, the Data Buffer prevents Writes to vendor specific CW pages (i.e., Pages 80 to FFh) triggered by commands received at the BCOM interface of the Data Buffer including MRW commands.

NOTE 10 This control word contains the number of package rank used on an MRDIMM. The Host controller will write RW80[5:4] to indicate which package ranks are used on the MRDIMM so that the DDR5MDB02 can power down unnecessary logic for unused package ranks. In Mux mode, Rank 0 and Rank 1 refer to these two ranks in both pseudo-channels.

NOTE 11 When RW80[4] is set to "1", package Rank 0 is not present.

NOTE 12 When RW80[5] is set to "1", package Rank 1 is not present.

### 11.7.2 RW81 Buffer Configuration Mode Control Word

This control word contains data buffer mode information that does not come from snooping of DRAM MRW commands.

**Table 91 — RW81: Buffer Configuration Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	PBA Enumerate Programming Mode <sup>2</sup>	PBA Enumerate Mode Disabled
x	x	x	x	x	x	x	1		PBA Enumerate Mode Enabled
x	x	x	x	x	x	0	x	VrefDQ broadcast	Disabled
x	x	x	x	x	x	1	x		Enabled
x	x	x	x	x	0	x	x	VrefMDQ broadcast	Disabled
x	x	x	x	x	1	x	x		Enabled
x	x	x	x	0	x	x	x	Rank 2 Present <sup>3</sup>	Package Rank 2 Enabled
x	x	x	x	1	x	x	x		(Default) Package Rank 2 Disabled <sup>4</sup>
x	x	x	0	x	x	x	x	Rank 3 Present <sup>2</sup>	Package Rank 3 Enabled
x	x	x	1	x	x	x	x		(Default) Package Rank 3 Disabled <sup>5</sup>
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 RW81[4:3] will be sticky, cleared by power cycle not reset.

NOTE 2 Assigns IDs to specific Data Buffer on the DIMM.

NOTE 3 This control word contains the number of package rank used on an MRDIMM. The Host controller will write RW81[4:3] to indicate which package ranks are used on the MRDIMM so that the DDR5MDB02 can power down unnecessary logic for unused package ranks. In Mux mode, Rank 2 and Rank 3 refer to these two ranks in both pseudo-channels.

NOTE 4 When RW81[3] is set to “1”, package Rank 2 is not present.

NOTE 5 When RW81[4] is set to “1”, package Rank 3 is not present.

### 11.7.3 RW82 - Transparent and DQ Pass Through Control Word

Table 92 — RW82: Transparent and DQ Pass Through Support Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Transparent Mode Enable	Transparent mode disabled
x	x	x	x	x	x	x	1		Transparent mode enabled <sup>1</sup>
x	x	x	x	x	x	0	x	Termination disable for TPM and DQ PTM	Termination enabled
x	x	x	x	x	x	1	x		Termination disabled
x	x	x	x	x	0	x	x	DQ Pass Through Mode	Disabled
x	x	x	x	x	1	x	x		Enabled
x	x	x	x	0	x	x	x	DQ pass through mode direction select	Write direction (default)
x	x	x	x	1	x	x	x		Read direction
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 A waiting time  $t_{TM\_Entry}$  applies when Transparent Mode is enabled in RW82[0].

### 11.7.4 RW83 - [M]DQS, [M]DQ Training Modes Control Word

Table 93 — RW83: [M]DQS, [M]DQ Training Modes Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Normal operation	Exit any of the training mode
x	x	x	x	0	0	0	1	MRE	DRAM Interface Receive Enable Training
x	x	x	x	0	0	1	0	MRD	MDQS Read Delay Training
x	x	x	x	0	0	1	1	DWL	DRAM Write Leveling
x	x	x	x	0	1	0	0	MWD	MDQ Write Delay Training
x	x	x	x	0	1	0	1	HWL	Host Interface Write Leveling
x	x	x	x	0	1	1	0	HIR	Host Interface Read Training
x	x	x	x	0	1	1	1	HIW <sup>2</sup>	Host Interface Write Training
x	x	x	x	1	0	0	0	Reserved	Reserved
x	x	x	0	x	x	x	x	HPA <sup>3</sup>	Host Preamble Training Mode disabled
x	x	x	1	x	x	x	x		Host Preamble Training Mode enabled
x	x	0	x	x	x	x	x	EWTM	Enhanced Write Training Mode disabled
x	x	1	x	x	x	x	x		Enhanced Write Training Mode enabled
x	0	x	x	x	x	x	x	ERTM	Enhanced Read Training Mode disabled
x	1	x	x	x	x	x	x		Enhanced Read Training Mode enabled
0	x	x	x	x	x	x	x	Host interface training support during Self-Refresh mode	Disabled (Default)
1	x	x	x	x	x	x	x		Enabled

NOTE 1 To allow the MDB to enter mode, the Host must wait  $t_{MRD\_L2}$  after write to RW83.

NOTE 2 HIW feature is supported only in Mux mode, not in Rank mode.

NOTE 3 When HPA is enabled the MDB ignores non-target read/MRR events

## 11.8 Timing and Voltage Control Words

### 11.8.1 RW84 - MRDIMM Host Interface Operating Speed

Table 94 — RW84: MRDIMM Host Interface Operating Speed<sup>1,2</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Operating Speed	DDR5-3200 (2800 MT/s < f ≤ 3200 MT/s) <sup>3</sup>
x	x	x	0	0	0	0	1		DDR5-3600 (3200 MT/s < f ≤ 3600 MT/s) <sup>3</sup>
x	x	x	0	0	0	1	0		DDR5-4000 (3600 MT/s < f ≤ 4000 MT/s) <sup>3</sup>
x	x	x	0	0	0	1	1		DDR5-4400 (4000 MT/s < f ≤ 4400 MT/s) <sup>3</sup>
x	x	x	0	0	1	0	0		DDR5-4800 (4400 MT/s < f ≤ 4800 MT/s) <sup>3</sup>
x	x	x	0	0	1	0	1		DDR5-4000 (4800 MT/s < f ≤ 5200 MT/s) <sup>3</sup>
x	x	x	0	0	1	1	0		DDR5-4400 (5200 MT/s < f ≤ 5600 MT/s) <sup>3</sup>
x	x	x	0	0	1	1	1		DDR5-4800 (5600 MT/s < f ≤ 6000 MT/s) <sup>3</sup>
x	x	x	0	1	0	0	0		(Default) DDR5 6400 (6000 MT/s < f ≤ 6400 MT/s) <sup>3,4</sup>
x	x	x	0	1	0	0	1		DDR5 6800 (6400 MT/s < f ≤ 6800 MT/s) <sup>4</sup>
x	x	x	0	1	0	1	0		DDR5 7200 (6800 MT/s < f ≤ 7200 MT/s) <sup>4</sup>
x	x	x	0	1	0	1	1		DDR5 7600 (7200 MT/s < f ≤ 7600 MT/s) <sup>4</sup>
x	x	x	0	1	1	0	0		DDR5 8000 (7600 MT/s < f ≤ 8000 MT/s) <sup>4</sup>
x	x	x	0	1	1	0	1		DDR5 8400 (8000 MT/s < f ≤ 8400 MT/s) <sup>4</sup>
x	x	x	0	1	1	1	0		Down-bin Data Rate (1980 MT/s < f ≤ 2100 MT/s) <sup>3</sup>
x	x	x	0	1	1	1	1		Test Frequency Range (560 MT/s < f < 1980 MT/s) <sup>5</sup>
x	x	x	1	0	0	0	0		DDR5-8800 (8400 MT/s < f ≤ 8800 MT/s) <sup>4</sup>
x	x	x	1	0	0	0	1		DDR5-9200 (8800 MT/s < f ≤ 9200 MT/s) <sup>4</sup>
x	x	x	1	0	0	1	0		DDR5-9600 (9200 MT/s < f ≤ 9600 MT/s) <sup>4</sup>
x	x	x	1	0	0	1	1		DDR5-10000 (9600 MT/s < f ≤ 10000 MT/s) <sup>4</sup>
x	x	x	1	0	1	0	0		DDR5-10400 (10000 MT/s < f ≤ 10400 MT/s) <sup>4</sup>
x	x	x	1	0	1	0	1		DDR5-10800 (10400 MT/s < f ≤ 10800 MT/s) <sup>4</sup>
x	x	x	1	0	1	1	0		DDR5-11200 (10800 MT/s < f ≤ 11200 MT/s) <sup>4</sup>
x	x	x	1	0	1	1	1		DDR5-11600 (11200 MT/s < f ≤ 11600 MT/s) <sup>4</sup>
x	x	x	1	1	0	0	0		DDR5-12000 (11600 MT/s < f ≤ 12000 MT/s) <sup>4</sup>
x	x	x	1	1	0	0	1		DDR5-12400 (12000 MT/s < f ≤ 12400 MT/s) <sup>4</sup>
x	x	x	1	1	0	1	0		DDR5-12800 (12400 MT/s < f ≤ 12800 MT/s) <sup>4</sup>
x	x	x	.....						Reserved
x	x	x	1	1	1	1	0		Down-bin Data Rate (3960 MT/s < f ≤ 4200 MT/s) <sup>4</sup>
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Context for operation training	Default; Context 1 operation
x	1	x	x	x	x	x	x		Context 2 operation <sup>6</sup>
0	x	x	x	x	x	x	x	Buffer V <sub>DD</sub> Operating Voltage <sup>7</sup>	1.1 V
1	x	x	x	x	x	x	x		Reserved

NOTE 1 The encoding value is used to inform the data buffer the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a data buffer can run.

NOTE 2 RW84[7:6] and RW84[4:0] will be sticky, cleared by power cycle not reset.

NOTE 3 This setting is applicable in Rank mode.

NOTE 4 This setting is applicable in Mux mode.

NOTE 5 The test frequency (0 1111) is in units of the DRAM frequency. This selection is used in transparent mode only, so the data rate is the same on both the DRAM and Host side of the interface.

NOTE 6 The control words listed in Table 11 are duplicated by the DDR5MDB02 for the 2nd frequency context.

NOTE 7 RW84[7] will be used to inform DDR5MDB02 under what operating voltage V<sub>DD</sub> will be used. The Data Buffer can use the information to optimize functionality and performance at low-voltage conditions.



## 11.8.2 RW85 - Host Interface Fine Granularity DIMM Operating Speed Control Word

Table 95 — RW85: Host Interface Fine Granularity DIMM Operating Speed Control Word<sup>1,2</sup>

Setting								Definition	Encoding <sup>3</sup>	
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0			
x	x	x	0	0	0	0	0	Fine Granularity Operating Speed in terms of $f_{bin}$ , where $f_{bin}$ is the top speed for the speed range selected in RW84 OP[3:0]	$(f_{bin} - 20 \text{ MT/s}) < f \leq f_{bin}$	
x	x	x	0	0	0	0	1		$(f_{bin} - 40 \text{ MT/s}) < f \leq (f_{bin} - 20 \text{ MT/s})$	
x	x	x	0	0	0	1	0		$(f_{bin} - 60 \text{ MT/s}) < f \leq (f_{bin} - 40 \text{ MT/s})$	
x	x	x	0	0	0	1	1		$(f_{bin} - 80 \text{ MT/s}) < f \leq (f_{bin} - 60 \text{ MT/s})$	
x	x	x	0	0	1	0	0		$(f_{bin} - 100 \text{ MT/s}) < f \leq (f_{bin} - 80 \text{ MT/s})$	
x	x	x	0	0	1	0	1		$(f_{bin} - 120 \text{ MT/s}) < f \leq (f_{bin} - 100 \text{ MT/s})$	
x	x	x	0	0	1	1	0		$(f_{bin} - 140 \text{ MT/s}) < f \leq (f_{bin} - 120 \text{ MT/s})$	
x	x	x	0	0	1	1	1		$(f_{bin} - 160 \text{ MT/s}) < f \leq (f_{bin} - 140 \text{ MT/s})$	
x	x	x	0	1	0	0	0		$(f_{bin} - 180 \text{ MT/s}) < f \leq (f_{bin} - 160 \text{ MT/s})$	
x	x	x	0	1	0	0	1		$(f_{bin} - 200 \text{ MT/s}) < f \leq (f_{bin} - 180 \text{ MT/s})$	
x	x	x	0	1	0	1	0		$(f_{bin} - 220 \text{ MT/s}) < f \leq (f_{bin} - 200 \text{ MT/s})$	
x	x	x	0	1	0	1	1		$(f_{bin} - 240 \text{ MT/s}) < f \leq (f_{bin} - 220 \text{ MT/s})$	
x	x	x	0	1	1	0	0		$(f_{bin} - 260 \text{ MT/s}) < f \leq (f_{bin} - 240 \text{ MT/s})$	
x	x	x	0	1	1	0	1		$(f_{bin} - 280 \text{ MT/s}) < f \leq (f_{bin} - 260 \text{ MT/s})$	
x	x	x	0	1	1	1	0		$(f_{bin} - 300 \text{ MT/s}) < f \leq (f_{bin} - 280 \text{ MT/s})$	
x	x	x	0	1	1	1	1		$(f_{bin} - 320 \text{ MT/s}) < f \leq (f_{bin} - 300 \text{ MT/s})$	
x	x	x	1	0	0	0	0		$(f_{bin} - 340 \text{ MT/s}) < f \leq (f_{bin} - 320 \text{ MT/s})$	
x	x	x	1	0	0	0	1		$(f_{bin} - 360 \text{ MT/s}) < f \leq (f_{bin} - 340 \text{ MT/s})$	
x	x	x	1	0	0	1	0		$(f_{bin} - 380 \text{ MT/s}) < f \leq (f_{bin} - 360 \text{ MT/s})$	
x	x	x	1	0	0	1	1		$(f_{bin} - 400 \text{ MT/s}) < f \leq (f_{bin} - 380 \text{ MT/s})$	
x	x	x	1	0	1	0	0		Reserved	
x	x	x	...						Reserved	
x	x	x	1	1	1	1	1		Reserved	
x	x	0	x	x	x	x	x		Reserved	Reserved
x	x	1	x	x	x	x	x			Reserved
x	0	x	x	x	x	x	x		Reserved	Reserved
x	1	x	x	x	x	x	x	Reserved		
0	x	x	x	x	x	x	x	Reserved	Reserved	
1	x	x	x	x	x	x	x		Reserved	

NOTE 1 This control word defines the frequency of the BCK<sub>t</sub> - BCK<sub>c</sub> input reference clock during normal operation (i.e., when not in test frequency range) in units of 20 MT/s (i.e., 10 MHz).

NOTE 2 RW85[4:0] will be sticky, cleared by power cycle not reset.

NOTE 3 The frequency ranges shown in this column are for the base frequency of the input clock and they do not include SSC modulation effects. In some cases, due to SSC modulation, the actual frequency of the input clock can straddle two adjacent frequency ranges.

### 11.8.3 RW86 - DQS RTT Park Termination Control Word

Table 96 — RW86: DQS RTT Park Termination Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	DQS_RTT_PARK	RTT_OFF (Default)
x	x	x	x	x	0	0	1		RZQ/1 (240 Ω)
x	x	x	x	x	0	1	0		RZQ/2 (120 Ω)
x	x	x	x	x	0	1	1		RZQ/3 (80 Ω)
x	x	x	x	x	1	0	0		RZQ/4 (60 Ω)
x	x	x	x	x	1	0	1		RZQ/5 (48 Ω)
x	x	x	x	x	1	1	0		RZQ/6 (40 Ω)
x	x	x	x	x	1	1	1		RZQ/7 (34 Ω)
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	DQS1_RTT_PARK	RTT_OFF (Default)
x	0	0	1	x	x	x	x		RZQ/1 (240 Ω)
x	0	1	0	x	x	x	x		RZQ/2 (120 Ω)
x	0	1	1	x	x	x	x		RZQ/3 (80 Ω)
x	1	0	0	x	x	x	x		RZQ/4 (60 Ω)
x	1	0	1	x	x	x	x		RZQ/5 (48 Ω)
x	1	1	0	x	x	x	x		RZQ/6 (40 Ω)
x	1	1	1	x	x	x	x		RZQ/7 (34 Ω)
0	x	x	x	x	x	x	x	DQS RTT Control	(Default) Apply RW86[2:0] setting to both DQS0 and DQS1
1	x	x	x	x	x	x	x		Apply RW86[2:0] setting to DQS0, and apply RW86[6:4] setting to DQS1.

NOTE 1 RW86[2:0, 7:4] will be sticky, cleared by power cycle not reset

### 11.8.4 RW87 - Host Interface DQ RTT Park Termination Control Word

Table 97 — RW87: Host Interface DQ RTT Park Termination Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	DQ RTT_PARK	RTT_OFF Default
x	x	x	x	x	0	0	1		RZQ/1 (240 Ω)
x	x	x	x	x	0	1	0		RZQ/2 (120 Ω)
x	x	x	x	x	0	1	1		RZQ/3 (80 Ω)
x	x	x	x	x	1	0	0		RZQ/4 (60 Ω)
x	x	x	x	x	1	0	1		RZQ/5 (48 Ω)
x	x	x	x	x	1	1	0		RZQ/6(40 Ω)
x	x	x	x	x	1	1	1		RZQ/7(34 Ω)
x	x	0	0	0	x	x	x	Reserved	Reserved
x	x	0	0	1	x	x	x		Reserved
x	x	0	1	0	x	x	x		Reserved
x	x	0	1	1	x	x	x		Reserved
x	x	1	0	0	x	x	x		Reserved
x	x	1	0	1	x	x	x		Reserved
x	x	1	1	0	x	x	x		Reserved
x	x	1	1	1	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 RW87[5:0] will be sticky, cleared by power cycle not reset

### 11.8.5 RW8A - Host Interface DQ Driver Control Word

Table 98 — RW8A: Host Interface DQ Driver Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Host Interface DQ/DQS Output Disable	Normal Operation -Default
x	x	x	x	x	x	x	1		Outputs Disabled
x	x	x	x	0	0	0	x	Host Interface DQ Output Driver Pull up Impedance control	RZQ/7 (34 Ω)
x	x	x	x	0	0	1	x		Reserved
x	x	x	x	0	1	0	x		RZQ/5 (48 Ω)
x	x	x	x	0	1	1	x		Reserved
x	x	x	x	1	0	0	x		Reserved
x	x	x	x	1	0	1	x		Reserved
x	x	x	x	1	1	0	x		Reserved
x	x	x	x	1	1	1	x		Reserved
x	0	0	0	x	x	x	x	Host Interface DQ Output Driver Pull Down Impedance control	RZQ/7 (34 Ω)
x	0	0	1	x	x	x	x		Reserved
x	0	1	0	x	x	x	x		RZQ/5 (48 Ω)
x	0	1	1	x	x	x	x		Reserved
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		Reserved
x	1	1	0	x	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 RW8A[6:0] will be sticky, cleared by power cycle not reset

### 11.8.6 RW8B - DRAM Interface MDQ Driver Control Word

Table 99 — RW8B: DRAM Interface MDQ Driver Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DRAM Interface MDQ/MDQS Output Disable	Normal Operation -Default
x	x	x	x	x	x	x	1		Outputs Disabled
x	x	x	x	0	0	0	x	DRAM Interface MDQ Output Driver Pull up Impedance control	RZQ / 7 (34 Ω)
x	x	x	x	0	0	1	x		RZQ / 6 (40 Ω)
x	x	x	x	0	1	0	x		RZQ / 5 (48 Ω)
x	x	x	x	0	1	1	x		RZQ / 4 (60Ω)
x	x	x	x	1	0	0	x		Reserved
x	x	x	x	1	0	1	x		Reserved
x	x	x	x	1	1	0	x		Reserved
x	x	x	x	1	1	1	x		Reserved
x	0	0	0	x	x	x	x	DRAM Interface MDQ Output Driver Pull Down Impedance control	RZQ / 7 (34 Ω)
x	0	0	1	x	x	x	x		RZQ / 6 (40 Ω)
x	0	1	0	x	x	x	x		RZQ / 5 (48 Ω)
x	0	1	1	x	x	x	x		RZQ / 4 (60Ω)
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		Reserved
x	1	1	0	x	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 RW8B[6:0] will be sticky, cleared by power cycle not reset

## 11.8.7 RW8C - MDQS and MDQ Park Termination Control Word

Table 100 — RW8C: MDQS and MDQ Park Termination Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	MDQS_RTT_PARK	RTT_OFF (Default)
x	x	x	x	x	0	0	1		RZQ/1 (240 $\Omega$ )
x	x	x	x	x	0	1	0		RZQ/2 (120 $\Omega$ )
x	x	x	x	x	0	1	1		RZQ/3 (80 $\Omega$ )
x	x	x	x	x	1	0	0		RZQ/4 (60 $\Omega$ )
x	x	x	x	x	1	0	1		RZQ/5 (48 $\Omega$ )
x	x	x	x	x	1	1	0		RZQ/6 (40 $\Omega$ )
x	x	x	x	x	1	1	1		RZQ/7 (34 $\Omega$ )
x	x	0	0	0	x	x	x	MDQ_RTT_PARK	RTT_OFF (Default)
x	x	0	0	1	x	x	x		RZQ/1 (240 $\Omega$ )
x	x	0	1	0	x	x	x		RZQ/2 (120 $\Omega$ )
x	x	0	1	1	x	x	x		RZQ/3 (80 $\Omega$ )
x	x	1	0	0	x	x	x		RZQ/4 (60 $\Omega$ )
x	x	1	0	1	x	x	x		RZQ/5 (48 $\Omega$ )
x	x	1	1	0	x	x	x		RZQ/6 (40 $\Omega$ )
x	x	1	1	1	x	x	x		RZQ/7 (34 $\Omega$ )
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x	Reserved	Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

NOTE 1 RW8C[5:0] will be sticky, cleared by power cycle not reset

### 11.8.8 RW8D - Loopback Control Word

Table 101 — RW8D: Loopback Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Loopback Enabled	Loopback mode disabled (default)
x	x	x	x	x	x	x	1		Loopback mode Enabled
x	x	x	x	x	x	0	x	Loopback Output Mode <sup>1</sup>	DQS qualified output (default) <sup>2</sup>
x	x	x	x	x	x	1	x		WE qualified output <sup>3</sup>
x	x	x	0	0	0	x	x	DQ Loopback selection	DQ0 selected (default)
x	x	x	0	0	1	x	x		DQ1
x	x	x	0	1	0	x	x		DQ2
x	x	x	0	1	1	x	x		DQ3
x	x	x	1	0	0	x	x		DQ4
x	x	x	1	0	1	x	x		DQ5
x	x	x	1	1	0	x	x		DQ6
x	x	x	1	1	1	x	x		DQ7
x	0	0	x	x	x	x	x	Loopback Phase Select <sup>4</sup>	Phase A selected (default)
x	x0	1	x	x	x	x	x		Phase B selected
x	1	0	x	x	x	x	x		Phase C selected
x	1	1	x	x	x	x	x		Phase D selected
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 This bit configures the MDB loopback output to either send data out every time the DQS toggles, or to only send it out when qualified with the write enable, so that only burst data is sent out via the loopback.

NOTE 2 Since this mode does not support normal WR and RD commands, only DQ\_RTT\_PARK termination, if enabled, is available in DQ pins. DQS\_RTT\_PARK termination, if enabled, is available for DQS pins.

NOTE 3 All termination features from normal operation available in DQ pins. DQS\_RTT\_PARK termination, if enabled, is available for DQS pins.

NOTE 4 Phase A refers to UI D0, D4, D8, etc. Phase B refers to UI D1, D5, D9, etc. Phase C refers to UI D2, D6, D10, etc. Phase D refers to UI D3, D7, D11, etc.

### 11.8.9 RW8E- Loopback RTT and Ron Control Word

Table 102 — RW8E: Loopback RTT and Ron Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	RTT_Loopback	RTT_OFF
x	x	x	x	x	0	0	1		Reserved
x	x	x	x	x	0	1	0		Reserved
x	x	x	x	x	0	1	1		Reserved
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		RZQ/5 (48 $\Omega$ ) Default
x	x	x	x	x	1	1	0		Reserved
x	x	x	x	x	1	1	1		Reserved
x	x	0	0	0	x	x	x	Loopback Driver Strength Settings	RZQ/7 (34 $\Omega$ ) Default
x	x	0	0	1	x	x	x		RZQ/6 (40 $\Omega$ )
x	x	0	1	0	x	x	x		RZQ/5 (48 $\Omega$ )
x	x	0	1	1	x	x	x		Reserved
x	x	1	0	0	x	x	x		Reserved
x	x	1	0	1	x	x	x		Reserved
x	x	1	1	0	x	x	x		Reserved
x	x	1	1	1	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

## 11.8.10 RW8F - Host Interface Read DQS Offset Timing Control Word

Table 103 — RW8F: Host Interface Read DQS Offset Timing Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Host Interface DQS0 Pre-launch <sup>2</sup>	0 tHDQS (DQS match DQ delay)
x	x	x	x	x	0	0	1		1 tHDQS
x	x	x	x	x	0	1	0		2 tHDQS
x	x	x	x	x	0	1	1		3 tHDQS
x	x	x	x	x	1	0	0		4 tHDQS
x	x	x	x	x	1	0	1		5 tHDQS
x	x	x	x	x	1	1	0		6 tHDQS
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	DQS0 0.5 tHDQS Granularity Mode	(Default) Normal operation
x	x	x	x	1	x	x	x		Enable 0.5 tHDQS Mode - This mode adds 0.5 tHDQS to each of the Host Interface DQS0 Pre-launch values from RW8F[2:0]
x	0	0	0	x	x	x	x	Host Interface DQS1 Pre-launch <sup>2</sup>	0 tHDQS (DQS match DQ delay)
x	0	0	1	x	x	x	x		1 tHDQS
x	0	1	0	x	x	x	x		2 tHDQS
x	0	1	1	x	x	x	x		3 tHDQS
x	1	0	0	x	x	x	x		4 tHDQS
x	1	0	1	x	x	x	x		5 tHDQS
x	1	1	0	x	x	x	x		6 tHDQS
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	DQS1 0.5 tHDQS Granularity Mode	(Default) Normal operation
1	x	x	x	x	x	x	x		Enable 0.5 tHDQS Mode - This mode adds 0.5 tHDQS to each of the Host Interface DQS1 Pre-launch values from RW8F[6:4]

NOTE 1 RW8F[7:0] will be sticky, cleared by power cycle not reset.

NOTE 2 In Mux mode, the supported range is up to 6 tHDQS, or 3 tBCK. In Rank mode with half data rate compared to Mux mode, the supported range is up to 3 tHDQS, which is still 3 tBCK. It is the Host's responsibility to program the Pre-launch settings properly.

## 11.9 DQ Training Configuration

### 11.9.1 RW90 - Continuous Burst Mode Control Word

Table 104 — RW90: Continuous Burst Mode Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Continuous Burst Mode Enable <sup>1</sup>	Mode disabled (default)
x	x	x	x	x	x	x	1		Mode enabled
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 This feature is not intended to be used when the DRAM pattern generator is also enabled.

### 11.9.2 RW92 - PBA Enumerate ID Control Word

Table 105 — RW92: PBA Enumerate ID Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	PBA Set ID <sup>2</sup>	ID = 0
x	x	x	x	0	0	0	1		ID = 1
x	x	x	x	0	0	1	0		ID = 2
x	x	x	x	0	0	1	1		ID = 3
x	x	x	x	0	1	0	0		ID = 4
x	x	x	x	0	1	0	1		ID = 5
x	x	x	x	0	1	1	0		ID = 6
x	x	x	x	0	1	1	1		ID = 7
x	x	x	x	1	0	0	0		ID = 8
x	x	x	x	1	0	0	1		ID = 9
x	x	x	x	1	0	1	0		ID = 10
x	x	x	x	1	0	1	1		ID = 11
x	x	x	x	1	1	0	0		ID = 12
x	x	x	x	1	1	0	1		ID = 13
x	x	x	x	1	1	1	0		ID = 14
x	x	x	x	1	1	1	1		ID = 15 (default)
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 RW92[3:0] will be sticky, cleared by power cycle not reset

NOTE 2 Only are written when PBA Enumerated Programming mode is enabled RW81[0] = 1.

### 11.9.3 RW93 - PBA Buffer Select ID Control Word

Table 106 — RW93: PBA Buffer Select ID Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	PBA Select ID <sup>2</sup>	ID = 0
x	x	x	x	0	0	0	1		ID = 1
x	x	x	x	0	0	1	0		ID = 2
x	x	x	x	0	0	1	1		ID = 3
x	x	x	x	0	1	0	0		ID = 4
x	x	x	x	0	1	0	1		ID = 5
x	x	x	x	0	1	1	0		ID = 6
x	x	x	x	0	1	1	1		ID = 7
x	x	x	x	1	0	0	0		ID = 8
x	x	x	x	1	0	0	1		ID = 9
x	x	x	x	1	0	1	0		ID = 10
x	x	x	x	1	0	1	1		ID = 11
x	x	x	x	1	1	0	0		ID = 12
x	x	x	x	1	1	0	1		ID = 13
x	x	x	x	1	1	1	0		ID = 14
x	x	x	x	1	1	1	1		ID = 15 Selects All Buffers (Default)
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 RW93[3:0] will be sticky, cleared by power cycle not reset

NOTE 2 Selects the data buffer or all data buffer to accept MRW command

### 11.9.4 RW[96:94] - Read-only register for the Internal Receive Enable Offset

Table 107 — RW[96:94]: Read-only Register for the Internal Receive Enable Offset<sup>1</sup>

RW	Description	Encoding
RW94[3:0]	Internal Receive Enable Offset	Lower Nibble Additional Cycles of DRAM Interface Receive Enable Delay
RW94[7:4]	Coarse Status	Upper Nibble Additional Cycles of DRAM Interface Receive Enable Delay
RW95[5:0]	Internal Receive Enable Offset Fine Lower Nibble Status	DRAM Interface Receive Enable Timing Phase Control in Steps of (1/64) * tBCK
RW96[5:0]	Internal Receive Enable Offset Fine Upper Nibble Status	DRAM Interface Receive Enable Timing Phase Control in Steps of (1/64) * tBCK

NOTE 1 RW[96:94]: are Read-only register for the Internal Receive Enable Offset



### 11.9.5 RW 97 - Buffer Training Configuration Control Word

**Table 108 — RW97: Buffer Training Configuration Control Word**

Settings (DA[7:0])								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Clear feedback status bit <sup>1</sup>	Default
x	x	x	x	x	x	x	1		Clear feedback status (all DQ feedback returns to HIGH)
x	x	x	x	x	x	0	x	Per UI Filtering	Disabled
x	x	x	x	x	x	1	x		Enabled
x	x	x	x	x	0	x	x	Long Read pattern sticky status feedback mode <sup>2</sup>	Enabled
x	x	x	x	x	1	x	x		Disabled
x	x	x	x	0	x	x	x	per-bit vs. per-transaction	Per-bit (default)
x	x	x	x	1	x	x	x		Per-transaction (per-nibble)
0	0	0	0	x	x	x	x	Select 1 of 16 UIs for Per UI Filtering	UI-0
0	0	0	1	x	x	x	x		UI-1
0	0	1	0	x	x	x	x		UI-2
0	0	1	1	x	x	x	x		UI-3
0	1	0	0	x	x	x	x		UI-4
0	1	0	1	x	x	x	x		UI-5
0	1	1	0	x	x	x	x		UI-6
0	1	1	1	x	x	x	x		UI-7
1	0	0	0	x	x	x	x		UI-8
1	0	0	1	x	x	x	x		UI-9
1	0	1	0	x	x	x	x		UI-10
1	0	1	1	x	x	x	x		UI-11
1	1	0	0	x	x	x	x		UI-12
1	1	0	1	x	x	x	x		UI-13
1	1	1	0	x	x	x	x		UI-14
1	1	1	1	x	x	x	x		UI-15

NOTE 1 Set to 1 to clear feedback status (all DQ feedback returns to HIGH). This bit automatically returns to 0.

NOTE 2 When Enabled, the Host DQ feedback will hold any mis-compare output (i.e., continue driving LOW) until Host sets the Clear Feedback Status bit in [RW97\[0\]](#). After exiting the training mode (i.e., MRD or MWD), the feedback status will be removed from the DQ pins to support Read/Write normal operation. The DDR5MDB02 hardware may clear the sticky status, but the Host is required to set the Clear Feedback Status bit in [RW97\[0\]](#) to guarantee that the sticky status will not be carried over into a new (MRD or MWD) training mode entry. When Disabled, the Host DQ feedback will change with each RD burst, depending on the comparison result. If only a single RD occurs and there is a mis-compare, the DQ feedback will still hold a LOW value until the next RD, or when the Host sets the “Clear Feedback Status” bit.

### 11.9.6 RW98 - Buffer Training Status Word

This control word contains status information that indicates the result of certain training modes.

The state of each bit in the Buffer Training Status Word must be preserved when the MDB enters or exits any training mode. This is needed because in most cases the data buffer needs to be taken out of training mode before the Host controller can access the Buffer Training Status Word by means of MRR commands. The MDB hardware should only update the state of the Buffer Training Status Word when a new result is generated by the corresponding training logic.

**Table 109 — RW98: PS0 or {R0, R1} Group Buffer Training Status Word<sup>1, 2</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ 0 status PS0 or {R0, R1} group	DQ status based on previous Read comparison
x	x	x	x	x	x	x	1		
x	x	x	x	x	x	0	x	DQ 1 status PS0 or {R0, R1} group	
x	x	x	x	x	x	1	x		
x	x	x	x	x	0	x	x	DQ 2 status PS0 or {R0, R1} group	
x	x	x	x	x	1	x	x		
x	x	x	x	0	x	x	x	DQ 3 status PS0 or {R0, R1} group	
x	x	x	x	1	x	x	x		
x	x	x	0	x	x	x	x	DQ 4 status PS0 or {R0, R1} group	
x	x	x	1	x	x	x	x		
x	x	0	x	x	x	x	x	DQ 5 status PS0 or {R0, R1} group	
x	x	1	x	x	x	x	x		
x	0	x	x	x	x	x	x	DQ 6 status PS0 or {R0, R1} group	
x	1	x	x	x	x	x	x		
0	x	x	x	x	x	x	x	DQ 7 status PS0 or {R0, R1} group	
1	x	x	x	x	x	x	x		

NOTE 1 The Training Status should always report per-DQ results per MRR or Read command (i.e. update the status register even if Long Read pattern sticky status is enabled) and should represent the results for the UI filtering setting in [RW97](#).

NOTE 2 [RW98](#) gets cleared with RESET strap command (BRST\_n assertion pulse with BCOM[2:0] driven All HIGH or All LOW) and power cycle or when the Clear Feedback Status bit in [RW97\[0\]](#) is set to 1.

### 11.9.6 RW98 - Buffer Training Status Word (cont'd)

**Table 110 — RW99: PS1 or {R2, R3} Group Buffer Training Status Word<sup>1, 2</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ 0 status PS1 or {R2, R3} group	DQ status based on previous Read comparison
x	x	x	x	x	x	x	1		
x	x	x	x	x	x	0	x	DQ 1 status PS1 or {R2, R3} group	
x	x	x	x	x	x	1	x		
x	x	x	x	x	0	x	x	DQ 2 status PS1 or {R2, R3} group	
x	x	x	x	x	1	x	x		
x	x	x	x	0	x	x	x	DQ 3 status PS1 or {R2, R3} group	
x	x	x	x	1	x	x	x		
x	x	x	0	x	x	x	x	DQ 4 status PS1 or {R2, R3} group	
x	x	x	1	x	x	x	x		
x	x	0	x	x	x	x	x	DQ 5 status PS1 or {R2, R3} group	
x	x	1	x	x	x	x	x		
x	0	x	x	x	x	x	x	DQ 6 status PS1 or {R2, R3} group	
x	1	x	x	x	x	x	x		
0	x	x	x	x	x	x	x	DQ 7 status PS1 or {R2, R3} group	
1	x	x	x	x	x	x	x		

NOTE 1 The Training Status should always report per-DQ results per MRR or Read command (i.e. update the status register even if Long Read pattern sticky status is enabled) and should represent the results for the UI filtering setting in [RW97](#).

NOTE 2 [RW99](#) gets cleared with RESET strap command (BRST\_n assertion pulse with BCOM[2:0] driven All HIGH or All LOW) and power cycle or when the Clear Feedback Status bit in [RW97\[0\]](#) is set to 1.

### 11.9.7 RW[9F:9C] PS0 or {R0, R1} Group Read and Write LFSR State Monitors

**Table 111 — RW[9F:9C] PS0 or {R0, R1} Group Read Training Mode Settings Control Words**

RW	Description	Encoding
<a href="#">RW9C[7:0]</a>	PS0 or {R0, R1} group READ LFSR0 State Monitor (Read Only)	The current state of READ LFSR0
<a href="#">RW9D[7:0]</a>	PS0 or {R0, R1} group READ LFSR1 State Monitor (Read Only)	The current state of READ LFSR1
<a href="#">RW9E[7:0]</a>	PS0 or {R0, R1} group WRITE LFSR0 State Monitor (Read Only)	The current state of WRITE LFSR0
<a href="#">RW9F[7:0]</a>	PS0 or {R0, R1} group WRITE LFSR1 State Monitor (Read Only)	The current state of WRITE LFSR1

## 11.10 DFE Control Words

### 11.10.1 RWA0 DFE Control Word.

Table 112 — RWA0: DFE Control Word Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DFE Feature Enable <sup>2</sup>	DFE and gain features Disabled (Default)
x	x	x	x	x	x	x	1		DFE and gain features Enabled
x	x	x	x	x	x	0	x	DFE_Vref Enable <sup>3</sup>	DFE_Vref Circuitry Disabled
x	x	x	x	x	x	1	x		DFE_Vref Circuitry Enabled
x	x	x	x	x	0	x	x	ERROR Counter Enable	All ERROR Counters Disable
x	x	x	x	x	1	x	x		All ERROR Counters Enabled
x	x	x	x	0	x	x	x	RW Control Word Writes Broadcasted <sup>4</sup>	RW Write to select DQn
x	x	x	x	1	x	x	x		RW Writes Broadcast to DQ[7:0] and DQS1 as CRC
x	x	x	0	x	x	x	x	Tap 1 Enable Bit for all DQ[7:0]	(Default) Tap 1 disabled
x	x	x	1	x	x	x	x		Tap 1 enabled
x	x	0	x	x	x	x	x	Tap 2 Enable Bit for all DQ[7:0]	(Default) Tap 2 disabled
x	x	1	x	x	x	x	x		Tap 2 enabled
x	0	x	x	x	x	x	x	Tap 3 Enable Bit for all DQ[7:0]	(Default) Tap 3 disabled
x	1	x	x	x	x	x	x		Tap 3 enabled
0	x	x	x	x	x	x	x	Tap 4 Enable Bit for all DQ[7:0]	(Default) Tap 4 disabled
1	x	x	x	x	x	x	x		Tap 4 enabled

NOTE 1 [RWA0\[7:0\]](#) will be sticky, cleared by power cycle not reset

NOTE 2 This control bit enables DFE circuitry in the Data Buffer

NOTE 3 To save power the Host can disable the DFE\_Vref Circuitry when not in use.

NOTE 4 When this bit is enabled, DFE RW Control Word Writes are broadcasted to all DQ pins and DQS1 as CRC which are selected for DFE training in [RWA2](#) and [RWA1\[7\]](#).

### 11.10.2 RWA1 - DQ[7:0] and DQS1 DFE Training Mode Control Word

Table 113 — RWA1 - DQ[7:0] and DQS1 DFE Training Mode Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Global DFE Training Mode Enable <sup>1</sup>	DFE Training Mode disabled
x	x	x	x	x	x	x	1		DFE Training Mode enabled <sup>2,3</sup>
x	x	x	x	x	0	0	x	Training Source	Monitor
x	x	x	x	x	0	1	x		Monitor XOR Slicer Output
x	x	x	x	x	1	0	x		Reserved
x	x	x	x	x	1	1	x		Reserved
x	x	x	x	0	x	x	x	DFE Error Counter Reset	Normal Operation
x	x	x	x	1	x	x	x		Resets upper and lower Error counters
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	DQS1 as CRC DFE pin selection <sup>1</sup>	DQS1 as CRC - Not Selected
1	x	x	x	x	x	x	x		DQS1 as CRC - Selected

NOTE 1 [RWA2\[7:0\]](#) and [RWA1\[7\]](#) determines the target receiver for DFE training.

NOTE 2 DFE circuits are configured into training mode for selected pin [RWA2](#) and [RWA1\[7\]](#).

NOTE 3 Vref generator circuits are configured so that a DFE training reference voltage (DFE\_Vref) is controlled by [PG\[6\]RW\[E2, E3, E6, E7, EA, EB, EE, EF, F2, F3, F6, F7, FA, FB, FE, FF\]](#) and [PG\[F\]RW\[F9:FA\]](#).

### 11.10.3 RWA2 - DQn DFE Pin Selection Control Word

Table 114 — RWA2 - DQn DFE Pin Selection Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQn DFE pin selection <sup>1</sup>	DQ0 - Not Selected
x	x	x	x	x	x	x	1		DQ0 - Selected
x	x	x	x	x	x	0	x		DQ1 - Not Selected
x	x	x	x	x	x	1	x		DQ1 - Selected
x	x	x	x	x	0	x	x		DQ2 - Not Selected
x	x	x	x	x	1	x	x		DQ2 - Selected
x	x	x	x	0	x	x	x		DQ3 - Not Selected
x	x	x	x	1	x	x	x		DQ3 - Selected
x	x	x	0	x	x	x	x		DQ4 - Not Selected
x	x	x	1	x	x	x	x		DQ4 - Selected
x	x	0	x	x	x	x	x		DQ5 - Not Selected
x	x	1	x	x	x	x	x		DQ5 - Selected
x	0	x	x	x	x	x	x		DQ6 - Not Selected
x	1	x	x	x	x	x	x		DQ6 - Selected
0	x	x	x	x	x	x	x		DQ7 - Not Selected
1	x	x	x	x	x	x	x		DQ7 - Selected

NOTE 1 RWA2[7:0] determines the target receivers for DFE training.

## 11.11 Periodic Update Control Words

### 11.11.1 RWB0: DRAM tDQS2DQ Tracking Control Word

Table 115 — RWB0: DRAM tDQS2DQ Tracking Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Tracking mode	DRAM tDQS2DQ tracking initialization mode enabled (default)
x	x	x	x	x	x	x	1		DRAM tDQS2DQ tracking mode enabled <sup>1</sup>
x	x	x	x	x	x	0	x	Clear all Tracking RWs in Page A and Page 71 <sup>2</sup>	Normal operation
x	x	x	x	x	x	1	x		All periodic control words are reset to zero. <sup>3</sup>
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	0	x	x	x	x	x	x		Reserved
x	1	x	x	x	x	x	x	Reserved	Reserved
0	x	x	x	x	x	x	x		Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved
									Reserved

NOTE 1 RWB0[0] will be sticky, cleared by power cycle not reset.

NOTE 2 RWB0[1] will only reset the PG[71,A] current context registers

NOTE 3 This applies to PG[A]RW[FF:E0] and PG[71]RW[FF:E0] control words. When this bit is set, all periodic control words are reset to zero. This bit is self-clearing in the next cycle.

### 11.11.2 RWB1: DRAM tDQS2DQ Tracking Return Value Control Word

Table 116 — RWB1: DRAM tDQS2DQ Tracking Return Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	x	DRAM tDQS2DQ Tracking Return Value <sup>1,2</sup>	Whenever there is a DRAM MRR to MR46 or MR47 the MDB will return the value from this register. This register defaults to 8'h00.

NOTE 1 The Host will program this register prior to DRAM tDQS2DQ tracking initialization mode or DRAM tDQS2DQ tracking mode or any access to DRAM MR46 or MR47.

NOTE 2 **RWB1** will be sticky, cleared by power cycle not reset

## 11.12 Static MRR Control Words

### 11.12.1 RWC0 - Target Read Page Address Control Word

Table 117 — RWC0: Target Read Page Address Control Word

RW	MRA[7:0] HEX	Meaning	Default
RWC0	0xC0	Target read page address in the Static MRR mode	0x0

### 11.12.2 RWC1 - Target Read Byte Address Control Word

Table 118 — RWC1: Target Read Byte Address Control Word

RW	MRA[7:0] HEX	Meaning	Default
RWC1	0xC1	Target read byte address in the Static MRR mode <sup>1</sup>	0x80

NOTE 1 When the value in RWC1 is in the range from 0x80 to 0xDF, the target read byte is from the direct control word space and RWC0 is ignored by the MDB. When the value in **RWC1** is in the range from 0xE0 to 0xFF, the target read byte is from the paged control word space with RWC0 as the page address. Any other values in RWC1 are illegal settings.

### 11.12.3 RWC2 - Static MRR Control Word Paging Control Words

Table 119 — RWC2: Static MRR Control Word

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	x	x	x	0	0	0	Target read bit offset in the Static MRR mode	(Default) Select bit 0 in the target control word byte
x	x	x	x	x	0	0	1		Select bit 1 in the target control word byte
x	x	x	x	x	0	1	0		Select bit 2 in the target control word byte
x	x	x	x	x	0	1	1		Select bit 3 in the target control word byte
x	x	x	x	x	1	0	0		Select bit 4 in the target control word byte
x	x	x	x	x	1	0	1		Select bit 5 in the target control word byte
x	x	x	x	x	1	1	0		Select bit 6 in the target control word byte
x	x	x	x	x	1	1	1		Select bit 7 in the target control word byte
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Static MRR output data return format select	(Default) Read one RW bit on eight DQ bits output <sup>1</sup>
x	1	x	x	x	x	x	x		Read eight RW bits on eight DQ bits output <sup>2</sup>
0	x	x	x	x	x	x	x	Static MRR mode enable	(Default) Static MRR mode disabled
1	x	x	x	x	x	x	x		Static MRR mode enabled

NOTE 1 In this mode, the selected RW bit by **RWC2[2:0]** will be driven to all eight DQ bits output.

NOTE 2 In this mode, **RWC2[2:0]** will be ignored. Each bit of the selected RW byte will be driven to the corresponding bit of the eight DQ bits output. RW bit 0 will be driven to DQ bit 0, RW bit 1 will be driven to DQ bit 1, and so on.

## 11.13 Paging Control Words

### 11.13.1 RWDF - CW Page Control Word

Table 120 — RWDF- CW Page Control Word

Page Control Register <sup>1</sup>							
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0

NOTE 1 Power on Default is **OP[7:0] = 0**.

## 11.14 Paged [M]DQS/[M]DQ Training Support Control Words

### 11.14.1 PG[0,1,72,73]RWE0: Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for all Ranks

The lower 4 bits of this control word is for the additional cycles of trained receive enable timing on the lower nibble (MDQS0\_t/MDQS0\_c) and upper 4 bits of this control word is for the upper nibble (MDQS1\_t/MDQS1\_c).

**Table 121 — PG[0,1,72,73]RWE0: Lower/Upper Nibble Additional Cycles DRAM Interface Receive Enable Control Word for all Ranks<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Receive Enable Delay <sup>2</sup>	0 tBCK receive enable timing latency adder.
x	x	x	x	0	0	0	1		+1 tBCK receive enable timing latency adder
x	x	x	x	0	0	1	0		+2 tBCK receive enable timing latency adder
x	x	x	x	0	0	1	1		+3 tBCK receive enable timing latency adder
x	x	x	x	0	1	0	0		+4 tBCK receive enable timing latency adder
x	x	x	x	0	1	0	1		+5 tBCK receive enable timing latency adder
x	x	x	x	0	1	1	0		+6 tBCK receive enable timing latency adder
x	x	x	x	0	1	1	1		+7 tBCK receive enable timing latency adder
x	x	x	x	1	0	0	0		0 tBCK receive enable timing latency adder.
x	x	x	x	1	0	0	1		-1 tBCK receive enable timing latency adder
x	x	x	x	1	0	1	0		-2 tBCK receive enable timing latency adder
x	x	x	x	1	0	1	1		-3 tBCK receive enable timing latency adder
x	x	x	x	1	1	0	0		-4 tBCK receive enable timing latency adder
x	x	x	x	1	1	0	1		-5 tBCK receive enable timing latency adder <sup>3</sup>
x	x	x	x	1	1	1	0		-6 tBCK receive enable timing latency adder <sup>3</sup>
x	x	x	x	1	1	1	1		-7 tBCK receive enable timing latency adder <sup>3</sup>
0	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Receive Enable Delay <sup>2</sup>	0 tBCK receive enable timing latency adder.
0	0	0	1	x	x	x	x		+1 tBCK receive enable timing latency adder
0	0	1	0	x	x	x	x		+2 tBCK receive enable timing latency adder
0	0	1	1	x	x	x	x		+3 tBCK receive enable timing latency adder
0	1	0	0	x	x	x	x		+4 tBCK receive enable timing latency adder
0	1	0	1	x	x	x	x		+5 tBCK receive enable timing latency adder
0	1	1	0	x	x	x	x		+6 tBCK receive enable timing latency adder
0	1	1	1	x	x	x	x		+7 tBCK receive enable timing latency adder
1	0	0	0	x	x	x	x		0 tBCK receive enable timing latency adder.
1	0	0	1	x	x	x	x		-1 tBCK receive enable timing latency adder
1	0	1	0	x	x	x	x		-2 tBCK receive enable timing latency adder
1	0	1	1	x	x	x	x		-3 tBCK receive enable timing latency adder
1	1	0	0	x	x	x	x		-4 tBCK receive enable timing latency adder
1	1	0	1	x	x	x	x		-5 tBCK receive enable timing latency adder <sup>3</sup>
1	1	1	0	x	x	x	x		-6 tBCK receive enable timing latency adder <sup>3</sup>
1	1	1	1	x	x	x	x		-7 tBCK receive enable timing latency adder <sup>3</sup>

NOTE 1 PG[0,1,72,73]RWE0 will be sticky, cleared by power cycle not reset.

NOTE 2 The baseline delay includes the snooped values for CL.

NOTE 3 It is guaranteed by the Host that this setting can be selected only at data rate above DDR5-8800.



### 11.14.2 PG[0,1,72,73]RWE1 - Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word

The lower 4 bits of this control word is for the additional cycles of trained write leveling timing on the lower nibble of Rank [1:0] (MDQS0\_t/MDQS0\_c) and upper 4 bits of this control word is for the upper nibble of Rank [1:0] (MDQS1\_t/MDQS1\_c).

**Table 122 — PG[0,1,72,73]RWE1: Lower/Upper Nibble Additional Cycles DRAM Interface Write Leveling Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Lower Nibble Additional Cycles of DRAM Interface Write Leveling Delay <sup>2</sup>	0 tBCK write leveling timing latency adder.
x	x	x	x	0	0	0	1		+1 tBCK write leveling timing latency adder
x	x	x	x	0	0	1	0		+2 tBCK write leveling timing latency adder
x	x	x	x	0	0	1	1		+3 tBCK write leveling timing latency adder
x	x	x	x	0	1	0	0		+4 tBCK write leveling timing latency adder
x	x	x	x	0	1	0	1		+5 tBCK write leveling timing latency adder
x	x	x	x	0	1	1	0		+6 tBCK write leveling timing latency adder
x	x	x	x	0	1	1	1		+7 tBCK write leveling timing latency adder
x	x	x	x	1	0	0	0		0 tBCK write leveling timing latency adder.
x	x	x	x	1	0	0	1		-1 tBCK write leveling timing latency adder
x	x	x	x	1	0	1	0		-2 tBCK write leveling timing latency adder
x	x	x	x	1	0	1	1		-3 tBCK write leveling timing latency adder
x	x	x	x	1	1	0	0		-4 tBCK write leveling timing latency adder
x	x	x	x	1	1	0	1		-5 tBCK write leveling timing latency adder <sup>3</sup>
x	x	x	x	1	1	1	0		-6 tBCK write leveling timing latency adder <sup>3</sup>
x	x	x	x	1	1	1	1		-7 tBCK write leveling timing latency adder <sup>3</sup>
0	0	0	0	x	x	x	x	Upper Nibble Additional Cycles of DRAM Interface Write Leveling Delay <sup>2</sup>	0 tBCK write leveling timing latency adder.
0	0	0	1	x	x	x	x		+1 tBCK write leveling timing latency adder
0	0	1	0	x	x	x	x		+2 tBCK write leveling timing latency adder
0	0	1	1	x	x	x	x		+3 tBCK write leveling timing latency adder
0	1	0	0	x	x	x	x		+4 tBCK write leveling timing latency adder
0	1	0	1	x	x	x	x		+5 tBCK write leveling timing latency adder
0	1	1	0	x	x	x	x		+6 tBCK write leveling timing latency adder
0	1	1	1	x	x	x	x		+7 tBCK write leveling timing latency adder
1	0	0	0	x	x	x	x		0 tBCK write leveling timing latency adder
1	0	0	1	x	x	x	x		-1 tBCK write leveling timing latency adder
1	0	1	0	x	x	x	x		-2 tBCK write leveling timing latency adder
1	0	1	1	x	x	x	x		-3 tBCK write leveling timing latency adder
1	1	0	0	x	x	x	x		-4 tBCK write leveling timing latency adder
1	1	0	1	x	x	x	x		-5 tBCK write leveling timing latency adder <sup>3</sup>
1	1	1	0	x	x	x	x		-6 tBCK write leveling timing latency adder <sup>3</sup>
1	1	1	1	x	x	x	x		-7 tBCK write leveling timing latency adder <sup>3</sup>

NOTE 1 PG[0,1,72,73]RWE1 will be sticky, cleared by power cycle not reset.

NOTE 2 The baseline delay includes the snooped values for CWL.

NOTE 3 It is guaranteed by the Host that this setting can be selected only at data rate above DDR5-8800.

### 11.14.3 PG[0,1,72,73]RWE2 - Lower Nibble DRAM Interface Receive Enable Training Control Word (per Rank)

**Table 123 — PG[0,1,72,73]RWE2: Lower Nibble DRAM Interface Receive Enable Training Control Word (per Rank)<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	DRAM Interface Receive Enable Timing Phase Control in Steps of (1/64) * tBCK	Delay MDQS receive enable timing by (0/64) * tBCK
x	x	0	0	0	0	0	1		Delay MDQS receive enable timing by (1/64) * tBCK
x	x	0	0	0	0	1	0		Delay MDQS receive enable timing by (2/64) * tBCK
x	x	0	0	0	0	1	1		Delay MDQS receive enable timing by (3/64) * tBCK
x	x	...							...
x	x	1	1	1	1	0	0		Delay MDQS receive enable timing by (60/64) * tBCK
x	x	1	1	1	1	0	1		Delay MDQS receive enable timing by (61/64) * tBCK
x	x	1	1	1	1	1	0		Delay MDQS receive enable timing by (62/64) * tBCK
x	x	1	1	1	1	1	1		Delay MDQS receive enable timing by (63/64) * tBCK
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

NOTE 1 PG[0,1,72,73]RWE2[5:0] will be sticky, cleared by power cycle not reset.

### 11.14.4 PG[0,1,72,73]RWE3 - Upper Nibble DRAM Interface Receive Enable Training Control Word (per Rank)

**Table 124 — PG[0,1,72,73]RWE3: Upper Nibble DRAM Interface Receive Enable Training Control Word (per Rank)<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	DRAM Interface Receive Enable Timing Phase Control in Steps of (1/64) * tBCK	Delay MDQS receive enable timing by (0/64) * tBCK
x	x	0	0	0	0	0	1		Delay MDQS receive enable timing by (1/64) * tBCK
x	x	0	0	0	0	1	0		Delay MDQS receive enable timing by (2/64) * tBCK
x	x	0	0	0	0	1	1		Delay MDQS receive enable timing by (3/64) * tBCK
x	x	...							...
x	x	1	1	1	1	0	0		Delay MDQS receive enable timing by (60/64) * tBCK
x	x	1	1	1	1	0	1		Delay MDQS receive enable timing by (61/64) * tBCK
x	x	1	1	1	1	1	0		Delay MDQS receive enable timing by (62/64) * tBCK
x	x	1	1	1	1	1	1		Delay MDQS receive enable timing by (63/64) * tBCK
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

NOTE 1 PG[0,1,72,73]RWE3[5:0] will be sticky, cleared by power cycle not reset.

### 11.14.5 PG[0,1,72,73]RWE4 - Lower Nibble MDQS Read Delay Control Word

**Table 125 — PG[0,1,72,73]RWE4 - Lower Nibble MDQS Read Delay Control Word (per Rank, per Nibble)<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Lower Nibble MDQS Delay Control During Read Transactions in Steps of (1/64) * t <sub>BCK</sub>	Default <sup>2</sup>
x	0	0	0	0	0	0	1		Delay MDQS by (01/64 + Default)*t <sub>BCK</sub>
x	0	0	0	0	0	1	0		Delay MDQS by (02/64 + Default)*t <sub>BCK</sub>
x	0	0	0	0	0	1	1		Delay MDQS by (03/64 + Default)*t <sub>BCK</sub>
...									...
x	0	0	0	1	1	1	1		Delay MDQS by (15/64 + Default)*t <sub>BCK</sub>
x	0	0	1	0	0	0	0		Default
x	0	0	1	0	0	0	1		Delay MDQS by (-01/64 + Default)*t <sub>BCK</sub>
x	0	0	1	0	0	1	0		Delay MDQS by (-02/64 + Default)*t <sub>BCK</sub>
x	0	0	1	0	0	1	1		Delay MDQS by (-03/64 + Default)*t <sub>BCK</sub>
...									...
x	0	0	1	1	1	1	1		Delay MDQS by (-15/64 + Default)*t <sub>BCK</sub>
x	0	1	0	0	0	0	0		Reserved
...									
x	0	1	0	1	1	1	1		Delay MDQS by (-16/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
x	0	1	1	0	0	0	0		...
...									Delay MDQS by (-31/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
x	0	1	1	1	1	1	1		Reserved
x	1	0	0	0	0	0	0		
...									Reserved
x	1	0	0	1	1	1	1		
x	1	0	1	0	0	0	0		Delay MDQS by (-32/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
...									...
x	1	0	1	1	1	1	1		Delay MDQS by (-47/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
x	1	1	0	0	0	0	0		Reserved
...									
x	1	1	0	1	1	1	1		Delay MDQS by (-48/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
x	1	1	1	0	0	0	0		...
...									Delay MDQS by (-63/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
x	1	1	1	1	1	1	1		

NOTE 1 This control word will be sticky, cleared by power cycle, not reset.

NOTE 2 Default =  $(1 + 1/4) * t_{BCK}$  if PG[70]RWE1 = 0; Default =  $1/4 * t_{BCK}$  if PG[70]RWE1[0] = 1. The value is applied for both Rank mode and Mux mode.

NOTE 3 Reserved if PG[70]RWE1[0] = 1.

### 11.14.6 PG[0,1,72,73]RWE5 - Upper Nibble MDQS Read Delay Control Word

Table 126 — PG[0,1,72,73]RWE5 - Upper Nibble MDQS Read Delay Control Word (per Rank, per Nibble)<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Upper Nibble MDQS Delay Control During Read Transactions in Steps of (1/64) * t <sub>BCK</sub>	Default <sup>2</sup>
x	0	0	0	0	0	0	1		Delay MDQS by (01/64 + Default)*t <sub>BCK</sub>
x	0	0	0	0	0	1	0		Delay MDQS by (02/64 + Default)*t <sub>BCK</sub>
x	0	0	0	0	0	1	1		Delay MDQS by (03/64 + Default)*t <sub>BCK</sub>
...									...
x	0	0	0	1	1	1	1		Delay MDQS by (15/64 + Default)*t <sub>BCK</sub>
x	0	0	1	0	0	0	0		Default
x	0	0	1	0	0	0	1		Delay MDQS by (-01/64 + Default)*t <sub>BCK</sub>
x	0	0	1	0	0	1	0		Delay MDQS by (-02/64 + Default)*t <sub>BCK</sub>
x	0	0	1	0	0	1	1		Delay MDQS by (-03/64 + Default)*t <sub>BCK</sub>
...									...
x	0	0	1	1	1	1	1		Delay MDQS by (-15/64 + Default)*t <sub>BCK</sub>
x	0	1	0	0	0	0	0		Reserved
...									
x	0	1	0	1	1	1	1		Delay MDQS by (-16/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
x	0	1	1	0	0	0	0		
...									...
x	0	1	1	1	1	1	1		Delay MDQS by (-31/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
x	1	0	0	0	0	0	0		
...									Reserved
x	1	0	0	1	1	1	1		
x	1	0	1	0	0	0	0		Delay MDQS by (-32/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
...									
x	1	0	1	1	1	1	1		Delay MDQS by (-47/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
x	1	1	0	0	0	0	0		
...									Reserved
x	1	1	0	1	1	1	1		
x	1	1	1	0	0	0	0		Delay MDQS by (-48/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
...									
x	1	1	1	1	1	1	1		Delay MDQS by (-63/64 + Default)*t <sub>BCK</sub> <sup>3</sup>
...									

NOTE 1 This control word will be sticky, cleared by power cycle, not reset.

NOTE 2 Default =  $(1 + 1/4) * t_{BCK}$  if PG[70]RWE1 = 0; Default =  $1/4 * t_{BCK}$  if PG[70]RWE1[0] = 1. The value is applied for both Rank mode and Mux mode.

NOTE 3 Reserved if PG[70]RWE1[0] = 1.

## 11.14.7 PG[0,1,72,73]RWE6 - Lower Nibble MDQ Write Baseline Delay Control Word

Table 127 — PG[0,1,72,73]RWE6: Lower Nibble MDQ Write Baseline Delay Control Word<sup>1</sup>

Setting								Definition	Encoding	
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0			
0	0	0	0	0	0	0	0	1	Phase Control for Lower Nibble MDQ with respect to MDQS_t During Write Transactions in Steps of (1/64) * tBCK <sup>2,3</sup>	MDQ phase delay = - tBCK/2
0	0	0	0	0	0	0	0	1		MDQ phase delay = - tBCK/2 + (1/64) * tBCK
0	0	0	0	0	0	0	1	0		MDQ phase delay = - tBCK/2 + (2/64) * tBCK
0	0	0	0	0	0	0	1	1		MDQ phase delay = - tBCK/2 + (3/64) * tBCK
0	0	0	0	0	0	1	0	0		MDQ phase delay = - tBCK/2 + (4/64) * tBCK
0	0	0	0	0	0	1	0	1		MDQ phase delay = - tBCK/2 + (5/64) * tBCK
0	0	0	0	0	0	1	1	0		MDQ phase delay = - tBCK/2 + (6/64) * tBCK
0	0	0	0	0	0	1	1	1		MDQ phase delay = - tBCK/2 + (7/64) * tBCK
0	0	0	0	0	1	0	0	0		MDQ phase delay = - tBCK/2 + (8/64) * tBCK
0	0	0	0	0	1	0	0	1		MDQ phase delay = - tBCK/2 + (9/64) * tBCK
0	0	0	0	0	1	0	1	0		MDQ phase delay = - tBCK/2 + (10/64) * tBCK
0	0	0	0	0	1	0	1	1		MDQ phase delay = - tBCK/2 + (11/64) * tBCK
0	0	0	0	0	1	1	0	0		MDQ phase delay = - tBCK/2 + (12/64) * tBCK
0	0	0	0	0	1	1	0	1		MDQ phase delay = - tBCK/2 + (13/64) * tBCK
0	0	0	0	0	1	1	1	0		MDQ phase delay = - tBCK/2 + (14/64) * tBCK
0	0	0	0	0	1	1	1	1		MDQ phase delay = - tBCK/2 + (15/64) * tBCK
0	0	0	0	1	0	0	0	0		MDQ phase delay = - tBCK/2 + (16/64)* tBCK (Default)
...										...
...										...
...										...
1	1	1	1	0	0	0	0	1		MDQ phase delay = - tBCK/2 + (241/64) * tBCK
1	1	1	1	0	0	0	1	0		MDQ phase delay = - tBCK/2 + (242/64) * tBCK
1	1	1	1	0	0	0	1	1		MDQ phase delay = - tBCK/2 + (243/64) * tBCK
1	1	1	1	0	1	0	0	0		MDQ phase delay = - tBCK/2 + (244/64) * tBCK
1	1	1	1	0	1	0	1	0		MDQ phase delay = - tBCK/2 + (245/64) * tBCK
1	1	1	1	0	1	1	0	0		MDQ phase delay = - tBCK/2 + (246/64) * tBCK
1	1	1	1	0	1	1	1	0		MDQ phase delay = - tBCK/2 + (247/64) * tBCK
1	1	1	1	1	0	0	0	0		MDQ phase delay = - tBCK/2 + (248/64) * tBCK
1	1	1	1	1	0	0	0	1		MDQ phase delay = - tBCK/2 + (249/64) * tBCK
1	1	1	1	1	0	1	0	0		MDQ phase delay = - tBCK/2 + (250/64) * tBCK
1	1	1	1	1	0	1	1	0		MDQ phase delay = - tBCK/2 + (251/64) * tBCK
1	1	1	1	1	1	0	0	0		MDQ phase delay = - tBCK/2 + (252/64) * tBCK
1	1	1	1	1	1	0	1	0		MDQ phase delay = - tBCK/2 + (253/64) * tBCK
1	1	1	1	1	1	1	0	0		MDQ phase delay = - tBCK/2 + (254/64) * tBCK
1	1	1	1	1	1	1	1	0		MDQ phase delay = - tBCK/2 + (255/64) * tBCK

NOTE 1 PG[73,72,1,0]RWE6 will be sticky, cleared by power cycle not reset.

NOTE 2 By default, the phase between the MDQ and MDQS signals driven by the DDR5MDB02 during write commands is tBCK/4 for both Rank mode and Mux mode, meaning MDQ is "tBCK/4" earlier than MDQS. The PG[73,72,1,0]RWE6 control bits can be used by the Host to adjust the phase relationship between lower nibble MDQ and MDQS to a more optimal position.

NOTE 3 MDQ needs to be delayed instead of MDQS since the MDQS phase is fixed after write leveling.

## 11.14.8 PG[0,1,72,73]RWE7 - Upper Nibble MDQ Write Baseline Delay Control Word

Table 128 — PG[0,1,72,73]RWE7: Upper Nibble MDQ Write Baseline Delay Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Phase Control for Upper Nibble MDQ with respect to MDQS_t During Write Transactions in Steps of (1/64) * tBCK <sup>2,3</sup>	MDQ phase delay = - tBCK/2
0	0	0	0	0	0	0	1		MDQ phase delay = - tBCK/2 + (1/64) * tBCK
0	0	0	0	0	0	0	1		MDQ phase delay = - tBCK/2 + (2/64) * tBCK
0	0	0	0	0	0	0	1		MDQ phase delay = - tBCK/2 + (3/64) * tBCK
0	0	0	0	0	0	1	0		MDQ phase delay = - tBCK/2 + (4/64) * tBCK
0	0	0	0	0	0	1	0		MDQ phase delay = - tBCK/2 + (5/64) * tBCK
0	0	0	0	0	0	1	1		MDQ phase delay = - tBCK/2 + (6/64) * tBCK
0	0	0	0	0	0	1	1		MDQ phase delay = - tBCK/2 + (7/64) * tBCK
0	0	0	0	0	1	0	0		MDQ phase delay = - tBCK/2 + (8/64) * tBCK
0	0	0	0	0	1	0	0		MDQ phase delay = - tBCK/2 + (9/64) * tBCK
0	0	0	0	0	1	0	1		MDQ phase delay = - tBCK/2 + (10/64) * tBCK
0	0	0	0	0	1	0	1		MDQ phase delay = - tBCK/2 + (11/64) * tBCK
0	0	0	0	0	1	1	0		MDQ phase delay = - tBCK/2 + (12/64) * tBCK
0	0	0	0	0	1	1	0		MDQ phase delay = - tBCK/2 + (13/64) * tBCK
0	0	0	0	0	1	1	1		MDQ phase delay = - tBCK/2 + (14/64) * tBCK
0	0	0	0	0	1	1	1		MDQ phase delay = - tBCK/2 + (15/64) * tBCK
0	0	0	0	1	0	0	0		MDQ phase delay = - tBCK/2 + (16/64) * tBCK (Default)
...									...
...									...
...									...
1	1	1	1	0	0	0	1	MDQ phase delay = - tBCK/2 + (241/64) * tBCK	
1	1	1	1	0	0	1	0	MDQ phase delay = - tBCK/2 + (242/64) * tBCK	
1	1	1	1	0	0	1	1	MDQ phase delay = - tBCK/2 + (243/64) * tBCK	
1	1	1	1	0	1	0	0	MDQ phase delay = - tBCK/2 + (244/64) * tBCK	
1	1	1	1	0	1	0	1	MDQ phase delay = - tBCK/2 + (245/64) * tBCK	
1	1	1	1	0	1	1	0	MDQ phase delay = - tBCK/2 + (246/64) * tBCK	
1	1	1	1	0	1	1	1	MDQ phase delay = - tBCK/2 + (247/64) * tBCK	
1	1	1	1	1	0	0	0	MDQ phase delay = - tBCK/2 + (248/64) * tBCK	
1	1	1	1	1	0	0	1	MDQ phase delay = - tBCK/2 + (249/64) * tBCK	
1	1	1	1	1	0	1	0	MDQ phase delay = - tBCK/2 + (250/64) * tBCK	
1	1	1	1	1	0	1	1	MDQ phase delay = - tBCK/2 + (251/64) * tBCK	
1	1	1	1	1	1	0	0	MDQ phase delay = - tBCK/2 + (252/64) * tBCK	
1	1	1	1	1	1	0	1	MDQ phase delay = - tBCK/2 + (253/64) * tBCK	
1	1	1	1	1	1	1	0	MDQ phase delay = - tBCK/2 + (254/64) * tBCK	
1	1	1	1	1	1	1	1	MDQ phase delay = - tBCK/2 + (255/64) * tBCK	

NOTE 1 PG[0,1,72,73]RWE7 will be sticky, cleared by power cycle not reset.

NOTE 2 By default, the phase between the MDQ and MDQS signals driven by the DDR5MDB02 during write commands is tBCK/4 for both Rank mode and Mux mode, meaning MDQ is "tBCK/4" earlier than MDQS. The PG[0,1,72,73]RWE7 control bits can be used by the Host to adjust the phase relationship between upper nibble MDQ and MDQS to a more optimal position.

NOTE 3 MDQ needs to be delayed instead of MDQS since the MDQS phase is fixed after write leveling.

### 11.14.9 PG[0,1,72,73]RWE8 - Lower Nibble DRAM Interface Write Leveling Control Word (per Rank)

Table 129 — PG[0,1,72,73]RWE8: Lower Nibble DRAM Interface Write Leveling Control Word (per Rank)<sup>1</sup>

Setting								Definition	Encoding	
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0			
x	x	0	0	0	0	0	0	DRAM Interface Write Leveling Timing Phase Control in Steps of (1/64) * tBCK	Delay MDQS write leveling timing by (0/64) * tBCK	
x	x	0	0	0	0	0	1		Delay MDQS write leveling timing by (1/64) * tBCK	
x	x	0	0	0	0	1	0		Delay MDQS write leveling timing by (2/64) * tBCK	
x	x	0	0	0	0	1	1		Delay MDQS write leveling timing by (3/64) * tBCK	
x	x	...							...	
x	x	1	1	1	1	0	0		Delay MDQS write leveling timing by (60/64) * tBCK	
x	x	1	1	1	1	0	1		Delay MDQS write leveling timing by (61/64) * tBCK	
x	x	1	1	1	1	1	0		Delay MDQS write leveling timing by (62/64) * tBCK	
x	x	1	1	1	1	1	1		Delay MDQS write leveling timing by (63/64) * tBCK	
0	0	x	x	x	x	x	x	Reserved	Reserved	
0	1	x	x	x	x	x	x		Reserved	
1	0	x	x	x	x	x	x		Reserved	
1	1	x	x	x	x	x	x		Reserved	

NOTE 1 PG[0,1,72,73]RWE8[5:0] will be sticky, cleared by power cycle not reset.

### 11.14.10 PG[0,1,72,73]RWE9 - Upper Nibble DRAM Interface Write Leveling Control Word (per Rank)

Table 130 — PG[0,1,72,73]RWE9: Upper Nibble DRAM Interface Write Leveling Control Word (per Rank)<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	DRAM Interface Write Leveling Timing Phase Control in Steps of (1/64) * tBCK	Delay MDQS write leveling timing by (0/64) * tBCK
x	x	0	0	0	0	0	1		Delay MDQS write leveling timing by (1/64) * tBCK
x	x	0	0	0	0	1	0		Delay MDQS write leveling timing by (2/64) * tBCK
x	x	0	0	0	0	1	1		Delay MDQS write leveling timing by (3/64) * tBCK
x	x	...							...
x	x	1	1	1	1	0	0		Delay MDQS write leveling timing by (60/64) * tBCK
x	x	1	1	1	1	0	1		Delay MDQS write leveling timing by (61/64) * tBCK
x	x	1	1	1	1	1	0		Delay MDQS write leveling timing by (62/64) * tBCK
x	x	1	1	1	1	1	1		Delay MDQS write leveling timing by (63/64) * tBCK
0	0	x	x	x	x	x	x	Reserved	Reserved
0	1	x	x	x	x	x	x		Reserved
1	0	x	x	x	x	x	x		Reserved
1	1	x	x	x	x	x	x		Reserved

NOTE 1 PG[0,1,72,73]RWE9[5:0] will be sticky, cleared by power cycle not reset.

### 11.14.11 PG[0,1,72,73]RWEA- MDQ0/4 Read Delay Control Word

The control word location PG[0,1,72,73]RWEA is used to store per lane precise delay adjustment for MDQ0 and MDQ4 relative to the whole nibble delays in PG[0,1,72,73]RW[E5:E4].

**Table 131 — PG[0,1,72,73]RWEA: MDQ0/4 Read Delay Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ0 and Lower Nibble	Delay MDQ0 with respect to baseline by +0/64 * tBCK (Default)
x	x	x	x	x	0	0	1	Baseline MDQS Delay	Delay MDQ0 with respect to baseline by +1/64 * tBCK
x	x	x	x	x	0	1	0	During Read Transactions in Steps of (1/64) * tBCK <sup>2</sup>	Delay MDQ0 with respect to baseline by +2/64 * tBCK
x	x	x	x	x	0	1	1		Delay MDQ0 with respect to baseline by +3/64 * tBCK
x	x	x	x	x	1	0	0		Delay MDQ0 with respect to baseline by -0/64 * tBCK (same as default)
x	x	x	x	x	1	0	1		Delay MDQ0 with respect to baseline by -1/64 * tBCK
x	x	x	x	x	1	1	0		Delay MDQ0 with respect to baseline by -2/64 * tBCK
x	x	x	x	x	1	1	1		Delay MDQ0 with respect to baseline by -3/64 * tBCK
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ4 and Upper Nibble	Delay MDQ4 with respect to baseline by +0/64 * tBCK (Default)
x	0	0	1	x	x	x	x	Baseline MDQS Delay	Delay MDQ4 with respect to baseline by +1/64 * tBCK
x	0	1	0	x	x	x	x	During Read Transactions in Steps of (1/64) * tBCK <sup>3</sup>	Delay MDQ4 with respect to baseline by +2/64 * tBCK
x	0	1	1	x	x	x	x		Delay MDQ4 with respect to baseline by +3/64 * tBCK
x	1	0	0	x	x	x	x		Delay MDQ4 with respect to baseline by -0/64 * tBCK (same as default)
x	1	0	1	x	x	x	x		Delay MDQ4 with respect to baseline by -1/64 * tBCK
x	1	1	0	x	x	x	x		Delay MDQ4 with respect to baseline by -2/64 * tBCK
x	1	1	1	x	x	x	x		Delay MDQ4 with respect to baseline by -3/64 * tBCK
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 PG[0,1,72,73]RWEA[6:4,2:0] will be sticky, cleared by power cycle not reset.

NOTE 2 The delay of the lower nibble MDQS<sub>t</sub>/MDQS<sub>c</sub> signals received by the DDR5MDB02 during read commands is set by PG[0,1,72,73]RWE4. The PG[0,1,72,73]RWEA[2:0] control bits can be used by the Host to adjust the phase relationship for the MDQ0 lane relative to the lower nibble baseline delay for a more optimal position.

NOTE 3 The delay of the upper nibble MDQS<sub>t</sub>/MDQS<sub>c</sub> signals received by the DDR5MDB02 during read commands is set by PG[0,1,72,73]RWE5. The PG[0,1,72,73]RWEA[6:4] control bits can be used by the Host to adjust the phase relationship for the MDQ4 lane relative to the upper nibble baseline delay for a more optimal position.



### 11.14.12 PG[0,1,72,73]RWEB- MDQ1/5 Read Delay Control Word

The control word location PG[0,1,72,73]RWEB is used to store per lane precise delay adjustment for MDQ1 and MDQ5 relative to the whole nibble delays in PG[0,1,72,73]RW[E5:E4].

**Table 132 — PG[0,1,72,73]RWEB: MDQ1/5 Read Delay Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ1 and Lower Nibble	Delay MDQ1 with respect to baseline by +0/64 * tBCK (Default)
x	x	x	x	x	0	0	1	Baseline MDQS Delay	Delay MDQ1 with respect to baseline by +1/64 * tBCK
x	x	x	x	x	0	1	0	During Read Transactions in Steps of (1/64) * tBCK <sup>2</sup>	Delay MDQ1 with respect to baseline by +2/64 * tBCK
x	x	x	x	x	0	1	1		Delay MDQ1 with respect to baseline by +3/64 * tBCK
x	x	x	x	x	1	0	0		Delay MDQ1 with respect to baseline by -0/64 * tBCK (same as default)
x	x	x	x	x	1	0	1		Delay MDQ1 with respect to baseline by -1/64 * tBCK
x	x	x	x	x	1	1	0		Delay MDQ1 with respect to baseline by -2/64 * tBCK
x	x	x	x	x	1	1	1		Delay MDQ1 with respect to baseline by -3/64 * tBCK
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ5 and Upper Nibble	Delay MDQ5 with respect to baseline by +0/64 * tBCK (Default)
x	0	0	1	x	x	x	x	Baseline MDQS Delay	Delay MDQ5 with respect to baseline by +1/64 * tBCK
x	0	1	0	x	x	x	x	During Read Transactions in Steps of (1/64) * tBCK <sup>3</sup>	Delay MDQ5 with respect to baseline by +2/64 * tBCK
x	0	1	1	x	x	x	x		Delay MDQ5 with respect to baseline by +3/64 * tBCK
x	1	0	0	x	x	x	x		Delay MDQ5 with respect to baseline by -0/64 * tBCK (same as default)
x	1	0	1	x	x	x	x		Delay MDQ5 with respect to baseline by -1/64 * tBCK
x	1	1	0	x	x	x	x		Delay MDQ5 with respect to baseline by -2/64 * tBCK
x	1	1	1	x	x	x	x		Delay MDQ5 with respect to baseline by -3/64 * tBCK
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 PG[0,1,72,73]RWEB[6:4,2:0] will be sticky, cleared by power cycle not reset.

NOTE 2 The delay of the lower nibble MDQS\_t/MDQS\_c signals received by the DDR5MDB02 during read commands is set by PG[0,1,72,73]RWE4. The PG[0,1,72,73]RWEB[2:0] control bits can be used by the Host to adjust the phase relationship for the MDQ1 lane relative to the lower nibble baseline delay for a more optimal position.

NOTE 3 The delay of the upper nibble MDQS\_t/MDQS\_c signals received by the DDR5MDB02 during read commands is set by PG[0,1,72,73]RWE5. The PG[0,1,72,73]RWEB[6:4] control bits can be used by the Host to adjust the phase relationship for the MDQ5 lane relative to the upper nibble baseline delay for a more optimal position.

### 11.14.13 PG[0,1,72,73]RWEC- MDQ2/6 Read Delay Control Word

The control word location PG[0,1,72,73]RWEC is used to store per lane precise delay adjustment for MDQ2 and MDQ6 relative to the whole nibble delays in PG[0,1,72,73]RW[E5:E4].

**Table 133 — PG[0,1,72,73]RWEC: MDQ2/6 Read Delay Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ2 and Lower Nibble	Delay MDQ2 with respect to baseline by +0/64 * tBCK (Default)
x	x	x	x	x	0	0	1	Baseline MDQS Delay	Delay MDQ2 with respect to baseline by +1/64 * tBCK
x	x	x	x	x	0	1	0	During Read Transactions	Delay MDQ2 with respect to baseline by +2/64 * tBCK
x	x	x	x	x	0	1	1	in Steps of (1/64) * tBCK <sup>2</sup>	Delay MDQ2 with respect to baseline by +3/64 * tBCK
x	x	x	x	x	1	0	0		Delay MDQ2 with respect to baseline by -0/64 * tBCK (same as default)
x	x	x	x	x	1	0	1		Delay MDQ2 with respect to baseline by -1/64 * tBCK
x	x	x	x	x	1	1	0		Delay MDQ2 with respect to baseline by -2/64 * tBCK
x	x	x	x	x	1	1	1		Delay MDQ2 with respect to baseline by -3/64 * tBCK
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x	Reserved	Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ6 and Upper Nibble	Delay MDQ6 with respect to baseline by +0/64 * tBCK (Default)
x	0	0	1	x	x	x	x	Baseline MDQS Delay	Delay MDQ6 with respect to baseline by +1/64 * tBCK
x	0	1	0	x	x	x	x	During Read Transactions	Delay MDQ6 with respect to baseline by +2/64 * tBCK
x	0	1	1	x	x	x	x	in Steps of (1/64) * tBCK <sup>3</sup>	Delay MDQ6 with respect to baseline by +3/64 * tBCK
x	1	0	0	x	x	x	x		Delay MDQ6 with respect to baseline by -0/64 * tBCK (same as default)
x	1	0	1	x	x	x	x		Delay MDQ6 with respect to baseline by -1/64 * tBCK
x	1	1	0	x	x	x	x		Delay MDQ6 with respect to baseline by -2/64 * tBCK
x	1	1	1	x	x	x	x		Delay MDQ6 with respect to baseline by -3/64 * tBCK
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

NOTE 1 PG[0,1,72,73]RWEC[6:4,2:0] will be sticky, cleared by power cycle not reset.

NOTE 2 The delay of the lower nibble MDQS\_t/MDQS\_c signals received by the DDR5MDB02 during read commands is set by PG[0,1,72,73]RWE4. The PG[0,1,72,73]RWEC[2:0] control bits can be used by the Host to adjust the phase relationship for the MDQ2 lane relative to the lower nibble baseline delay for a more optimal position.

NOTE 3 The delay of the upper nibble MDQS\_t/MDQS\_c signals received by the DDR5MDB02 during read commands is set by PG[0,1,72,73]RWE5. The PG[0,1,72,73]RWEC[6:4] control bits can be used by the Host to adjust the phase relationship for the MDQ6 lane relative to the upper nibble baseline delay for a more optimal position.

### 11.14.14 PG[0,1,72,73]RWED - MDQ3/7 Read Delay Control Word

The control word location PG[0,1,72,73]RWED is used to store per lane precise delay adjustment for MDQ3 and MDQ7 relative to the whole nibble delays in PG[0,1,72,73]RW[E5:E4].

**Table 134 — PG[0,1,72,73]RWED: MDQ3/7 Read Delay Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ3 and Lower Nibble	Delay MDQ3 with respect to baseline by +0/64 * tBCK (Default)
x	x	x	x	x	0	0	1	Baseline MDQS Delay	Delay MDQ3 with respect to baseline by +1/64 * tBCK
x	x	x	x	x	0	1	0	During Read Transactions	Delay MDQ3 with respect to baseline by +2/64 * tBCK
x	x	x	x	x	0	1	1	in Steps of (1/64) * tBCK <sup>2</sup>	Delay MDQ3 with respect to baseline by +3/64 * tBCK
x	x	x	x	x	1	0	0		Delay MDQ3 with respect to baseline by -0/64 * tBCK (same as default)
x	x	x	x	x	1	0	1		Delay MDQ3 with respect to baseline by -1/64 * tBCK
x	x	x	x	x	1	1	0		Delay MDQ3 with respect to baseline by -2/64 * tBCK
x	x	x	x	x	1	1	1		Delay MDQ3 with respect to baseline by -3/64 * tBCK
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x	Reserved	Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ7 and Upper Nibble	Delay MDQ7 with respect to baseline by +0/64 * tBCK (Default)
x	0	0	1	x	x	x	x	Baseline MDQS Delay	Delay MDQ7 with respect to baseline by +1/64 * tBCK
x	0	1	0	x	x	x	x	During Read Transactions	Delay MDQ7 with respect to baseline by +2/64 * tBCK
x	0	1	1	x	x	x	x	in Steps of (1/64) * tBCK <sup>3</sup>	Delay MDQ7 with respect to baseline by +3/64 * tBCK
x	1	0	0	x	x	x	x		Delay MDQ7 with respect to baseline by -0/64 * tBCK (same as default)
x	1	0	1	x	x	x	x		Delay MDQ7 with respect to baseline by -1/64 * tBCK
x	1	1	0	x	x	x	x		Delay MDQ7 with respect to baseline by -2/64 * tBCK
x	1	1	1	x	x	x	x		Delay MDQ7 with respect to baseline by -3/64 * tBCK
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

NOTE 1 PG[0,1,72,73]RWED[6:4,2:0] will be sticky, cleared by power cycle not reset.

NOTE 2 The delay of the lower nibble MDQS\_t/MDQS\_c signals received by the DDR5MDB02 during read commands is set by PG[0,1,72,73]RWE4. The PG[0,1,72,73]RWED[2:0] control bits can be used by the Host to adjust the phase relationship for the MDQ3 lane relative to the lower nibble baseline delay for a more optimal position.

NOTE 3 The delay of the upper nibble MDQS\_t/MDQS\_c signals received by the DDR5MDB02 during read commands is set by PG[0,1,72,73]RWE5. The PG[0,1,72,73]RWED[6:4] control bits can be used by the Host to adjust the phase relationship for the MDQ7 lane relative to the upper nibble baseline delay for a more optimal position.

### 11.14.15 PG[0,1,72,73]RWEE - MDQ0/4 Write Delay Control Word

The control word location PG[0,1,72,73]RWEE are used to store per lane precise delay adjustment for MDQ0 and MDQ4 relative to the whole nibble delays in PG[0,1,72,73]RW[E7:E6].

**Table 135 — PG[0,1,72,73]RWEE: MDQ0/4 Write Delay Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ0 and Lower Nibble	Delay MDQ0 with respect to baseline by +0/64 * tBCK (Default)
x	x	x	x	x	0	0	1	Baseline MDQ Delay	Delay MDQ0 with respect to baseline by +1/64 * tBCK
x	x	x	x	x	0	1	0	During Write Transactions	Delay MDQ0 with respect to baseline by +2/64 * tBCK
x	x	x	x	x	0	1	1	in Steps of (1/64) * tBCK <sup>2</sup>	Delay MDQ0 with respect to baseline by +3/64 * tBCK
x	x	x	x	x	1	0	0		Delay MDQ0 with respect to baseline by -0/64 * tBCK (same as default)
x	x	x	x	x	1	0	1		Delay MDQ0 with respect to baseline by -1/64 * tBCK
x	x	x	x	x	1	1	0		Delay MDQ0 with respect to baseline by -2/64 * tBCK
x	x	x	x	x	1	1	1		Delay MDQ0 with respect to baseline by -3/64 * tBCK
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x	Reserved	Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ4 and Upper Nibble	Delay MDQ4 with respect to baseline by +0/64 * tBCK (Default)
x	0	0	1	x	x	x	x	Baseline MDQ Delay	Delay MDQ4 with respect to baseline by +1/64 * tBCK
x	0	1	0	x	x	x	x	During Write Transactions	Delay MDQ4 with respect to baseline by +2/64 * tBCK
x	0	1	1	x	x	x	x	in Steps of (1/64) * tBCK <sup>3</sup>	Delay MDQ4 with respect to baseline by +3/64 * tBCK
x	1	0	0	x	x	x	x		Delay MDQ4 with respect to baseline by -0/64 * tBCK (same as default)
x	1	0	1	x	x	x	x		Delay MDQ4 with respect to baseline by -1/64 * tBCK
x	1	1	0	x	x	x	x		Delay MDQ4 with respect to baseline by -2/64 * tBCK
x	1	1	1	x	x	x	x		Delay MDQ4 with respect to baseline by -3/64 * tBCK
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

NOTE 1 PG[0,1,72,73]RWEE[6:4,2:0] will be sticky, cleared by power cycle not reset.

NOTE 2 The phase between the lower nibble MDQ and MDQS signals driven by the DDR5MDB02 during write commands is set by PG[0,1,72,73]RWE6. The PG[0,1,72,73]RWEE[2:0] control bits can be used by the Host to adjust the phase relationship for the MDQ0 lane relative to the lower nibble baseline for a more optimal position.

NOTE 3 The phase between the upper nibble MDQ and MDQS signals driven by the DDR5MDB02 during write commands is set by PG[0,1,72,73]RWE7. The PG[0,1,72,73]RWEE[6:4] control bits can be used by the Host to adjust the phase relationship for the MDQ4 lane relative to the upper nibble baseline for a more optimal position.

### 11.14.16 PG[0,1,72,73]RWEF- MDQ1/5 Write Delay Control Word

The control word location PG[0,1,72,73]RWEF is used to store per lane precise delay adjustment for MDQ1 and MDQ5 relative to the whole nibble delays in PG[0,1,72,73]RW[E7:E6].

**Table 136 — PG[0,1,72,73]RWEF: MDQ1/5 Write Delay Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ1 and Lower Nibble	Delay MDQ1 with respect to baseline by +0/64 * tBCK (Default)
x	x	x	x	x	0	0	1	Baseline MDQ Delay	Delay MDQ1 with respect to baseline by +1/64 * tBCK
x	x	x	x	x	0	1	0	During Write Transactions	Delay MDQ1 with respect to baseline by +2/64 * tBCK
x	x	x	x	x	0	1	1	in Steps of (1/64) * tBCK <sup>2</sup>	Delay MDQ1 with respect to baseline by +3/64 * tBCK
x	x	x	x	x	1	0	0		Delay MDQ1 with respect to baseline by -0/64 * tBCK (same as default)
x	x	x	x	x	1	0	1		Delay MDQ1 with respect to baseline by -1/64 * tBCK
x	x	x	x	x	1	1	0		Delay MDQ1 with respect to baseline by -2/64 * tBCK
x	x	x	x	x	1	1	1		Delay MDQ1 with respect to baseline by -3/64 * tBCK
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x	Reserved	Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ5 and Upper Nibble	Delay MDQ5 with respect to baseline by +0/64 * tBCK (Default)
x	0	0	1	x	x	x	x	Baseline MDQ Delay	Delay MDQ5 with respect to baseline by +1/64 * tBCK
x	0	1	0	x	x	x	x	During Write Transactions	Delay MDQ5 with respect to baseline by +2/64 * tBCK
x	0	1	1	x	x	x	x	in Steps of (1/64) * tBCK <sup>3</sup>	Delay MDQ5 with respect to baseline by +3/64 * tBCK
x	1	0	0	x	x	x	x		Delay MDQ5 with respect to baseline by -0/64 * tBCK (same as default)
x	1	0	1	x	x	x	x		Delay MDQ5 with respect to baseline by -1/64 * tBCK
x	1	1	0	x	x	x	x		Delay MDQ5 with respect to baseline by -2/64 * tBCK
x	1	1	1	x	x	x	x		Delay MDQ5 with respect to baseline by -3/64 * tBCK
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

NOTE 1 PG[0,1,72,73]RWEF[6:4,2:0] will be sticky, cleared by power cycle not reset.

NOTE 2 The phase between the lower nibble MDQ and MDQS signals driven by the DDR5MDB02 during write commands is set by PG[0,1,72,73]RWE6. The PG[0,1,72,73]RWEF[2:0] control bits can be used by the Host to adjust the phase relationship for the MDQ1 lane relative to the lower nibble baseline for a more optimal position.

NOTE 3 The phase between the upper nibble MDQ and MDQS signals driven by the DDR5MDB02 during write commands is set by PG[0,1,72,73]RWE7. The PG[0,1,72,73]RWEF[6:4] control bits can be used by the Host to adjust the phase relationship for the MDQ5 lane relative to the upper nibble baseline for a more optimal position.

### 11.14.17 PG[0,1,72,73]RWF0- MDQ2/6 Write Delay Control Word

The control word location PG[0,1,72,73]RWF0 is used to store per lane precise delay adjustment for MDQ2 and MDQ6 relative to the whole nibble delays in PG[0,1,72,73]RW[E7:E6].

**Table 137 — PG[0,1,72,73]RWF0: MDQ2/6 Write Delay Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ2 and Lower Nibble	Delay MDQ2 with respect to baseline by +0/64 * tBCK (Default)
x	x	x	x	x	0	0	1	Baseline MDQ Delay	Delay MDQ2 with respect to baseline by +1/64 * tBCK
x	x	x	x	x	0	1	0	During Write Transactions in Steps of (1/64) * tBCK <sup>2</sup>	Delay MDQ2 with respect to baseline by +2/64 * tBCK
x	x	x	x	x	0	1	1		Delay MDQ2 with respect to baseline by +3/64 * tBCK
x	x	x	x	x	1	0	0		Delay MDQ2 with respect to baseline by -0/64 * tBCK (same as default)
x	x	x	x	x	1	0	1		Delay MDQ2 with respect to baseline by -1/64 * tBCK
x	x	x	x	x	1	1	0		Delay MDQ2 with respect to baseline by -2/64 * tBCK
x	x	x	x	x	1	1	1		Delay MDQ2 with respect to baseline by -3/64 * tBCK
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ6 and Upper Nibble	Delay MDQ6 with respect to baseline by +0/64 * tBCK (Default)
x	0	0	1	x	x	x	x	Baseline MDQ Delay	Delay MDQ6 with respect to baseline by +1/64 * tBCK
x	0	1	0	x	x	x	x	During Write Transactions in Steps of (1/64) * tBCK <sup>3</sup>	Delay MDQ6 with respect to baseline by +2/64 * tBCK
x	0	1	1	x	x	x	x		Delay MDQ6 with respect to baseline by +3/64 * tBCK
x	1	0	0	x	x	x	x		Delay MDQ6 with respect to baseline by -0/64 * tBCK (same as default)
x	1	0	1	x	x	x	x		Delay MDQ6 with respect to baseline by -1/64 * tBCK
x	1	1	0	x	x	x	x		Delay MDQ6 with respect to baseline by -2/64 * tBCK
x	1	1	1	x	x	x	x		Delay MDQ6 with respect to baseline by -3/64 * tBCK
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 PG[0,1,72,73]RWF0[6:4,2:0] will be sticky, cleared by power cycle not reset.

NOTE 2 The phase between the lower nibble MDQ and MDQS signals driven by the DDR5MDB02 during write commands is set by PG[0,1,72,73]RWE6. The PG[0,1,72,73]RWF0[2:0] control bits can be used by the Host to adjust the phase relationship for the MDQ2 lane relative to the lower nibble baseline for a more optimal position.

NOTE 3 The phase between the upper nibble MDQ and MDQS signals driven by the DDR5MDB02 during write commands is set by PG[0,1,72,73]RWE7. The PG[0,1,72,73]RWF0[6:4] control bits can be used by the Host to adjust the phase relationship for the MDQ6 lane relative to the upper nibble baseline for a more optimal position.

### 11.14.18 PG[0,1,72,73]RWF1- MDQ3/7 Write Delay Control Word

The control word location PG[0,1,72,73]RWF1 is used to store per lane precise delay adjustment for MDQ3 and MDQ7 relative to the whole nibble delays in PG[0,1,72,73]RW[E7:E6].

**Table 138 — PG[0,1,72,73]RWF1: MDQ3/7 Write Delay Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Phase Control Between MDQ3 and Lower Nibble	Delay MDQ3 with respect to baseline by +0/64 * tBCK (Default)
x	x	x	x	x	0	0	1	Baseline MDQ Delay	Delay MDQ3 with respect to baseline by +1/64 * tBCK
x	x	x	x	x	0	1	0	During Write Transactions in Steps of (1/64) * tBCK <sup>2</sup>	Delay MDQ3 with respect to baseline by +2/64 * tBCK
x	x	x	x	x	0	1	1		Delay MDQ3 with respect to baseline by +3/64 * tBCK
x	x	x	x	x	1	0	0		Delay MDQ3 with respect to baseline by -0/64 * tBCK (same as default)
x	x	x	x	x	1	0	1		Delay MDQ3 with respect to baseline by -1/64 * tBCK
x	x	x	x	x	1	1	0		Delay MDQ3 with respect to baseline by -2/64 * tBCK
x	x	x	x	x	1	1	1		Delay MDQ3 with respect to baseline by -3/64 * tBCK
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Phase Control Between MDQ7 and Upper Nibble	Delay MDQ7 with respect to baseline by +0/64 * tBCK (Default)
x	0	0	1	x	x	x	x	Baseline MDQ Delay	Delay MDQ7 with respect to baseline by +1/64 * tBCK
x	0	1	0	x	x	x	x	During Write Transactions in Steps of (1/64) * tBCK <sup>3</sup>	Delay MDQ7 with respect to baseline by +2/64 * tBCK
x	0	1	1	x	x	x	x		Delay MDQ7 with respect to baseline by +3/64 * tBCK
x	1	0	0	x	x	x	x		Delay MDQ7 with respect to baseline by -0/64 * tBCK (same as default)
x	1	0	1	x	x	x	x		Delay MDQ7 with respect to baseline by -1/64 * tBCK
x	1	1	0	x	x	x	x		Delay MDQ7 with respect to baseline by -2/64 * tBCK
x	1	1	1	x	x	x	x		Delay MDQ7 with respect to baseline by -3/64 * tBCK
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 PG[0,1,72,73]RWF1[6:4,2:0] will be sticky, cleared by power cycle not reset.

NOTE 2 The phase between the lower nibble MDQ and MDQS signals driven by the DDR5MDB02 during write commands is set by PG[0,1,72,73]RWE6. The PG[0,1,72,73]RWF1[2:0] control bits can be used by the Host to adjust the phase relationship for the MDQ3 lane relative to the lower nibble baseline for a more optimal position.

NOTE 3 The phase between the upper nibble MDQ and MDQS signals driven by the DDR5MDB02 during write commands is set by PG[0,1,72,73]RWE7. The PG[0,1,72,73]RWF1[6:4] control bits can be used by the Host to adjust the phase relationship for the MDQ7 lane relative to the upper nibble baseline for a more optimal position.

## 11.15 Paged Vref Control Words

### 11.15.1 PG[2]RW[E7:E0] - Host Interface Internal VrefDQ Control Word

Table 139 — PG[2]RW[E7:E0]: Host Interface Internal VrefDQ Control Word<sup>1,2</sup>

Setting								Definition	Encoding VrefDQ as % of V <sub>DD</sub> <sup>3</sup>
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Host Interface Internal VrefDQ Control	97.5%
x	0	0	0	0	0	0	1		97.0%
x	0	0	0	0	0	0	1		96.5%
x	0	0	0	0	0	1	1		96.0%
x	0	0	0	0	1	0	0		95.5%
x	0	0	0	0	1	0	1		95.0%
x	0	0	0	0	1	1	0		94.5%
x	0	0	0	0	1	1	1		94.0%
x	...								...
x	0	1	0	1	1	0	1		75% (Default)
x	...								...
x	1	1	1	0	1	0	1		39.0%
x	1	1	1	0	1	1	0		38.5%
x	1	1	1	0	1	1	1		38.0%
x	1	1	1	1	0	0	0		37.5%
x	1	1	1	1	0	0	1		37.0%
x	1	1	1	1	0	1	0		36.5%
x	1	1	1	1	0	1	1		36.0%
x	1	1	1	1	1	0	0		35.5%
x	1	1	1	1	1	0	1		35.0%
x	1	1	1	1	1	1	0		Reserved
x	1	1	1	1	1	1	1		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		

NOTE 1 PG[2]RW[E7:E0] will be sticky, cleared by power cycle not reset

NOTE 2 Table 68 illustrates the assignment of each control word in the PG[2]RW[E7:E0] group to the corresponding input pin it controls.

NOTE 3 These are target VrefDQ values. Acceptable actual values are determined based on tolerances defined in electrical section.



### 11.15.2 PG[2]RW[F3:F0] - DRAM Interface Internal VrefMDQ Control Word

PG[2]RW[F1:F0] controls VrefMDQ for PS0 or {R0, R1} group and PG[2]RW[F3:F2] controls VrefMDQ PS1 or {R2, R3} group

**Table 140 — PG[2]RW[F3:F0]: DRAM Interface Internal VrefMDQ Control Word<sup>1,2,3</sup>**

Setting								Definition	Encoding VrefMDQ as % of V <sub>DD</sub> <sup>4</sup>
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	DRAM Interface Internal VrefMDQ Control	97.5%
x	0	0	0	0	0	0	1		97.0%
x	0	0	0	0	0	0	1		96.5%
x	0	0	0	0	0	1	1		96.0%
x	0	0	0	0	1	0	0		95.5%
x	0	0	0	0	1	0	1		95.0%
x	0	0	0	0	1	1	0		94.5%
x	0	0	0	0	1	1	1		94.0%
x	...								...
x	0	1	0	1	1	0	1		75% (Default)
x	...								...
x	1	1	1	0	1	0	1		39.0%
x	1	1	1	0	1	1	0		38.5%
x	1	1	1	0	1	1	1		38.0%
x	1	1	1	1	0	0	0		37.5%
x	1	1	1	1	0	0	1		37.0%
x	1	1	1	1	0	1	0		36.5%
x	1	1	1	1	0	1	1		36.0%
x	1	1	1	1	1	0	0		35.5%
x	1	1	1	1	1	0	1		35.0%
x	1	1	1	1	1	1	0		Reserved
x	1	1	1	1	1	1	1		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		

NOTE 1 PG[2]RW[F3:F0] will be sticky, cleared by power cycle not reset

NOTE 2 Table 68 illustrates the assignment of each control word in the PG[2]RW[F1:F0] group to the corresponding input pin it controls.

NOTE 3 Table 140 applies to Upper and Lower nibble on DRAM interface.

NOTE 4 These are target VrefMDQ values. Acceptable actual values are determined based on tolerances defined in electrical section.

## 11.15.3 PG[2]RWFA - Internal BVref Control Word

Table 141 — PG[2]RWFA: Internal BVref Control Word

Setting								Definition	Encoding BVref as % of V <sub>DD</sub> <sup>1</sup>
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Internal BVref Control	97.5%
x	0	0	0	0	0	0	1		97.0%
x	0	0	0	0	0	1	0		96.5%
x	0	0	0	0	0	1	1		96.0%
x	0	0	0	0	1	0	0		95.5%
x	0	0	0	0	1	0	1		95.0%
x	0	0	0	0	1	1	0		94.5%
x	0	0	0	0	1	1	1		94.0%
x	...								...
x	0	1	0	1	1	0	1		75% (Default)
x	...								...
x	1	1	1	0	1	0	1		39.0%
x	1	1	1	0	1	1	0		38.5%
x	1	1	1	0	1	1	1		38.0%
x	1	1	1	1	0	0	0		37.5%
x	1	1	1	1	0	0	1		37.0%
x	1	1	1	1	0	1	0		36.5%
x	1	1	1	1	0	1	1		36.0%
x	1	1	1	1	1	0	0		35.5%
x	1	1	1	1	1	0	1		35.0%
x	1	1	1	1	1	1	0		Reserved
x	1	1	1	1	1	1	1		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		

NOTE 1 These are target BVref values. Acceptable actual values are determined based on tolerances defined in electrical section.

## 11.16 Serial Number Paged Control Words

Page 3 contains Read-Only status words related to unique serial number and manufacturing information.

### 11.16.1 PG[3]RWE0 - Date Code Byte 0 Global Word

Table 142 — PG[3]RWE0: Date Code Byte 0 Global Word

Setting								Definition	Encoding	
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0			
x	x	x	x	0	0	0	0	Date Code Digit 0 <sup>1,2</sup> Year Information - Ones Digit (Read Only)	Digit = 0	
x	x	x	x	0	0	0	1		Digit = 1	
x	x	x	x	0	0	1	0		Digit = 2	
x	x	x	x	...					...	
x	x	x	x	0	1	1	1		Digit = 7	
x	x	x	x	1	0	0	0		Digit = 8	
x	x	x	x	1	0	0	1		Digit = 9	
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved	
x	x	x	x	...						
x	x	x	x	1	1	1	1			
0	0	0	0	x	x	x	x	Date Code Digit 1 <sup>1, 2</sup> Year Information - Tens Digit (Read Only)	Digit = 0	
0	0	0	1	x	x	x	x		Digit = 1	
0	0	1	0	x	x	x	x		Digit = 2	
...				x	x	x	x		...	
0	1	1	1	x	x	x	x		Digit = 7	
1	0	0	0	x	x	x	x		Digit = 8	
1	0	0	1	x	x	x	x		Digit = 9	
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved	
...				x	x	x	x			
1	1	1	1	x	x	x	x			

NOTE 1 Programmed and locked in one-time programmable memory by DDR5MDB02 vendor.

NOTE 2 This is year date code byte for the MDB. It must be represented in Binary Coded Decimal (BCD). For example, year 2015 would be coded as 0x15 (0001 0101).

## 11.16.2 PG[3]RWE1 - Date Code Byte 1 Global Word

Table 143 — PG[3]RWE1: Date Code Byte 1 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Date Code Digit 2 <sup>1,2</sup> Work Week Information - Ones Digit ISO 8601-compliant (Read Only)	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x	...					...
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 3 <sup>1, 2</sup> Work Week Information - Tens Digit ISO 8601-compliant (Read Only)	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

NOTE 1 Programmed and locked in one-time programmable memory by DDR5MDB02 vendor.

NOTE 2 This is work week date code byte for the MDB. It must be represented in Binary Coded Decimal (BCD). For example, week 47 would be coded as 0x47 (0100 0111).

## 11.16.3 PG[3]RWE2 - Date Code Byte 2 Global Word

Table 144 — PG[3]RWE2: Date Code Byte 2 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Date Code Digit 4 <sup>1</sup> Reserved (Read Only)	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x	...					...
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x		
0	0	0	1	x	x	x	x	Date Code Digit 5 <sup>1</sup> Reserved (Read Only)	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

NOTE 1 Programmed and locked in one-time programmable memory by DDR5MDB02 vendor.

#### 11.16.4 PG[3]RWE3 - Vendor Specific Unique Unit Code Byte 0 Global Word

Table 145 — PG[3]RWE3: Vendor Specific Unique Unit Code Byte 0 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 0 of Unique Unit Code <sup>1,2</sup> (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE 1 Programmed and locked in one-time programmable memory by DDR5MDB02 vendor.

NOTE 2 A setting of all 0's in PG[3]RW[E9:E3] is not allowed.

#### 11.16.5 PG[3]RWE4 - Vendor Specific Unique Unit Code Byte 1 Global Word

Table 146 — PG[3]RWE4: Vendor Specific Unique Unit Code Byte 1 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 1 of Unique Unit Code <sup>1,2</sup> (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE 1 Programmed and locked in one-time programmable memory by DDR5MDB02 vendor.

NOTE 2 A setting of all 0's in PG[3]RW[E9:E3] is not allowed.

#### 11.16.6 PG[3]RWE5 - Vendor Specific Unique Unit Code Byte 2 Global Word

Table 147 — PG[3]RWE5: Vendor Specific Unique Unit Code Byte 2 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 2 of Unique Unit Code <sup>1,2</sup> (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE 1 Programmed and locked in one-time programmable memory by DDR5MDB02 vendor.

NOTE 2 A setting of all 0's in PG[3]RW[E9:E3] is not allowed.

### 11.16.7 PG[3]RWE6 - Vendor Specific Unique Unit Code Byte 3 Global Word

Table 148 — PG[3]RWE6: Vendor Specific Unique Unit Code Byte 3 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 3 of Unique Unit Code <sup>1,2</sup> (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255
1	1	1	1	1	1	1	1		

NOTE 1 Programmed and locked in one-time programmable memory by DDR5MDB02 vendor.

NOTE 2 A setting of all 0's in PG[3]RW[E9:E3] is not allowed.

### 11.16.8 PG[3]RWE7 - Vendor Specific Unique Unit Code Byte 4 Global Word

Table 149 — PG[3]RWE7: Vendor Specific Unique Unit Code Byte 4 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 4 of Unique Unit Code <sup>1,2</sup> (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255
1	1	1	1	1	1	1	1		Code 255

NOTE 1 Programmed and locked in one-time programmable memory by DDR5MDB02 vendor.

NOTE 2 A setting of all 0's in PG[3]RW[E9:E3] is not allowed.

### 11.16.9 PG[3]RWE8 - Vendor Specific Unique Unit Code Byte 5 Global Word

Table 150 — PG[3]RWE8: Vendor Specific Unique Unit Code Byte 5 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 5 of Unique Unit Code <sup>1,2</sup> (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255
1	1	1	1	1	1	1	1		Code 255

NOTE 1 Programmed and locked in one-time programmable memory by DDR5MDB02 vendor.

NOTE 2 A setting of all 0's in PG[3]RW[E9:E3] is not allowed.

### 11.16.10 PG[3]RWE9 - Vendor Specific Unique Unit Code Byte 6 Global Word

Table 151 — PG[3]RWE9: Vendor Specific Unique Unit Code Byte 6 Global Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 6 of Unique Unit Code <sup>1,2</sup> (Read Only)	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

NOTE 1 Programmed and locked in one-time programmable memory by DDR5MDB02 vendor.

NOTE 2 A setting of all 0's in PG[3]RW[E9:E3] is not allowed.

### 11.16.11 PG[3]RWEA - Vendor ID Byte 0 Global Word

Table 152 — PG[3]RWEA: Vendor ID Byte 0 Global Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 0 of Vendor ID (Read Only)	VID[7:0] = 0x00h
0	0	0	0	0	0	0	1		VID[7:0] = 0x01h
0	0	0	0	0	0	1	0		VID[7:0] = 0x02h
...									...
1	1	1	1	1	1	0	1		VID[7:0] = 0xFDh
1	1	1	1	1	1	1	0		VID[7:0] = 0xFEh
1	1	1	1	1	1	1	1		VID[7:0] = 0xFFh

NOTE 1 Each vendor will have a specific Vendor ID value assigned by JEDEC according to JEP106.

### 11.16.12 PG[3]RWEB - Vendor ID Byte 1 Global Word

Table 153 — PG[3]RWEB: Vendor ID Byte 1 Global Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Byte 1 of Vendor ID (Read Only)	VID[15:8] = 0x00h
0	0	0	0	0	0	0	1		VID[15:8] = 0x01h
0	0	0	0	0	0	1	0		VID[15:8] = 0x02h
...									...
1	1	1	1	1	1	0	1		VID[15:8] = 0xFDh
1	1	1	1	1	1	1	0		VID[15:8] = 0xFEh
1	1	1	1	1	1	1	1		VID[15:8] = 0xFFh

NOTE 1 Each vendor will have a specific Vendor ID value assigned by JEDEC according to JEP106.

**11.16.13 PG[3]RVEC - Device ID Byte 0 Global Word****Table 154 — PG[3]RVEC: Device ID Byte 0 Global Word<sup>1</sup>**

Byte 0 of Device ID (Read Only)							
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	1	0	1	0	0	1	0

NOTE 1 The device ID value is 0x0552.

**11.16.14 PG[3]RWED - Device ID Byte 1 Global Word****Table 155 — PG[3]RWED: Device ID Byte 1 Global Word<sup>1</sup>**

Byte 1 of Device ID (Read Only)							
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	0	0	0	0	1	0	1

NOTE 1 The device ID value is 0x0552.

**11.16.15 PG[3]RWEE - Revision ID Global Word****Table 156 — PG[3]RWEE: Revision ID Global Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Revision ID (Read Only)	RID[7:0] = 0x00h
0	0	0	0	0	0	0	1		RID[7:0] = 0x01h
0	0	0	0	0	0	1	0		RID[7:0] = 0x02h
...									...
1	1	1	1	1	1	0	1		RID[7:0] = 0xFDh
1	1	1	1	1	1	1	0		RID[7:0] = 0xFEh
1	1	1	1	1	1	1	1		RID[7:0] = 0xFFh

NOTE 1 This is a fixed vendor specific register.



## 11.17 Paged DFE Control Words

### 11.17.1 PG[5:4]RW[E0,E8,F0,F8] DQ[7:0] and PG[F]RWF8 CRC Lane Receiver DFE Gain Offset

**Table 157 — PG[5:4]RW[E0,E8,F0,F8] DQ[7:0] and PG[F]RWF8 CRC Lane Receiver DFE Gain Offset Adjustment<sup>1,2</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Flat-band (DC) gain adjustment <sup>3,4,5,6,7</sup>	Gain Adjustment = 0 dB (default)
x	x	x	x	x	0	0	1		Gain Adjustment = +6 dB
x	x	x	x	x	0	1	0		Gain Adjustment = +4 dB
x	x	x	x	x	0	1	1		Gain Adjustment = +2 dB
x	x	x	x	x	1	0	0		Gain Adjustment = 0 dB (same as default)
x	x	x	x	x	1	0	1		Gain Adjustment = -2 dB
x	x	x	x	x	1	1	0		Gain Adjustment = -4 dB
x	x	x	x	x	1	1	1		Gain Adjustment = -6 dB
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x		Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x		Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x		Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x		Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 Table 70 and Table 71 illustrate the assignment of each control word in the PG[5:4]RW[E0,E8,F0,F8] group to the corresponding input pin it controls.

NOTE 2 Since DQS1 as CRC lane is a differential pair instead of a single-ended signal, the DFE Gain range defined in PG[F]RWF8[2:0] is required to support up to +/-2 dB.

NOTE 3 Flat-band (DC) gain adjustment (up to the Nyquist rate) adjustment control from I/O die pad to latching element in DQn.

NOTE 4 The Gain Adjustment is applied to the baseline (default) inherent gain implemented in the receiver.

NOTE 5 Gain Adjustment values shown are verified by design and the measurement from device pins is defined in a separate specification.

NOTE 6 Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 60, “DFE Gain and Tap Coefficient Step Parameters.”

NOTE 7 PG[5:4]RW[E0,E8,F0,F8] will be sticky, cleared by power cycle not reset.

### 11.17.2 PG[5:4]RW[E1,E9,F1,F9] DQ[7:0] and PG[F]RWF0 CRC lane Receiver DFE Tap 1 Coefficients

**Table 158 — PG[5:4]RW[E1,E9,F1,F9] DQ [7:0] and PG[F]RWF0 CRC Lane Receiver DFE Tap 1 Coefficients<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	0	0	0	0	0	0	0	Tap 1 DFE Coefficient <sup>2,3,4</sup>	(Default) Tap 1 DFE bias = 0 mV
x	0	0	0	0	0	0	1		Tap 1 DFE bias +1 Tap Step
x	0	0	0	0	0	1	0		Tap 1 DFE bias +2 Tap Steps
x	0	0	0	0	0	1	1		Tap 1 DFE bias +3 Tap Steps
x	0	0	0	0	1	0	0		Tap 1 DFE bias +4 Tap Steps
x	0	0	0	0	1	0	1		Tap 1 DFE bias +5 Tap Steps
x	0	0	0	0	1	1	0		Tap 1 DFE bias +6 Tap Steps
x	0	0	0	0	1	1	1		Tap 1 DFE bias +7 Tap Steps
x	0	0	0	1	0	0	0		Tap 1 DFE bias +8 Tap Steps
x	0	0	0	1	0	0	1		Tap 1 DFE bias +9 Tap Steps
x	0	0	0	1	0	1	0		Tap 1 DFE bias +10 Tap Steps
x	0	0	0	1	0	1	1		Tap 1 DFE bias +11 Tap Steps
x	0	0	0	1	1	0	0		Tap 1 DFE bias +12 Tap Steps
x	0	0	0	1	1	0	1		Tap 1 DFE bias +13 Tap Steps
x	0	0	0	1	1	1	0		Tap 1 DFE bias +14 Tap Steps
x	0	0	0	1	1	1	1		Tap 1 DFE bias +15 Tap Steps
x	.....								.....
x	1	1	0	0	0	1	0		Tap 1 DFE bias +98 Tap Steps
x	1	1	0	0	0	1	1		Tap 1 DFE bias +99 Tap Steps
x	1	1	0	0	1	0	0		Tap 1 DFE bias +100 Tap Steps
x	1	1	0	0	1	0	1		Reserved
x	.....								Reserved
x	1	1	1	1	1	1	1		Reserved
0	x	x	x	x	x	x	x	Tap 1 Coefficient Sign Bit	(Default) Positive Tap 1 DFE bias when Tap 1 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 1 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 1 DFE bias when Tap 1 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 1 post-cursor)

NOTE 1 Table 70 and Table 71 illustrate the assignment of each control word in the PG[5:4]RW[E1,E9,F1,F9] group to the corresponding input pin it controls.

NOTE 2 Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification.

NOTE 3 Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 60, “DFE Gain and Tap Coefficient Step Parameters,”.

NOTE 4 PG[5:4]RW[E1,E9,F1,F9] will be sticky, cleared by power cycle not reset.

### 11.17.3 PG[5:4]RW[E2,EA,F2,FA] DQ[7:0] and PG[F]RWF1 CRC Lane Receiver DFE Tap 2 Coefficients

Table 159 — PG[5:4]RW[E2,EA,F2,FA] DQ[7:0] and PG[F]RWF1 CRC Lane Receiver DFE Tap 2 Coefficients<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	0	0	0	0	0	0	Tap 2 DFE Coefficient <sup>2,3,4</sup>	(Default) Tap 2 DFE bias = 0 mV
x	x	0	0	0	0	0	1		Tap 2 DFE bias+1 Tap Step
x	x	0	0	0	0	1	0		Tap 2 DFE bias +2 Tap Steps
x	x	0	0	0	0	1	1		Tap 2 DFE bias +3 Tap Steps
x	x	0	0	0	1	0	0		Tap 2 DFE bias +4 Tap Steps
x	x	0	0	0	1	0	1		Tap 2 DFE bias +5 Tap Steps
x	x	0	0	0	1	1	0		Tap 2 DFE bias +6 Tap Steps
x	x	0	0	0	1	1	1		Tap 2 DFE bias +7 Tap Steps
x	x	0	0	1	0	0	0		Tap 2 DFE bias +8 Tap Steps
x	x	0	0	1	0	0	1		Tap 2 DFE bias +9 Tap Steps
x	x	0	0	1	0	1	0		Tap 2 DFE bias +10 Tap Steps
x	x	0	0	1	0	1	1		Tap 2 DFE bias +11 Tap Steps
x	x	0	0	1	1	0	0		Tap 2 DFE bias +12 Tap Steps
x	x	0	0	1	1	0	1		Tap 2 DFE bias +13 Tap Steps
x	x	0	0	1	1	1	0		Tap 2 DFE bias +14 Tap Steps
x	x	0	0	1	1	1	1		Tap 2 DFE bias +15 Tap Steps
x	x	.....							.....
x	x	1	0	0	1	1	0		Tap 2 DFE bias +38 Tap Steps
x	x	1	0	0	1	1	1		Tap 2 DFE bias +39 Tap Steps
x	x	1	0	1	0	0	0		Tap 2 DFE bias +40 Tap Steps
x	x	1	0	1	0	0	1		Reserved
x	x	.....							Reserved
x	x	1	1	1	1	1	1		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Tap 2 Coefficient Sign Bit	(Default) Positive Tap 2 DFE bias when Tap 2 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 2 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 2 DFE bias when Tap 2 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 2 post-cursor)

NOTE 1 Table 70 and Table 71 illustrate the assignment of each control word in the PG[5:4]RW[E2,EA,F2,FA] group to the corresponding input pin it controls.

NOTE 2 Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification.

NOTE 3 Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 60, “DFE Gain and Tap Coefficient Step Parameters.”

NOTE 4 PG[5:4]RW[E2,EA,F2,FA] will be sticky, cleared by power cycle not reset.

### 11.17.4 PG[5:4]RW[E3,EB,F3,FB] DQ[7:0] and PG[F]RWF2 CRC lane Receiver DFE Tap 3 Coefficient

**Table 160 — PG[5:4]RW[E3,EB,F3,FB] DQ[7:0] and PG[F]RWF2 CRC Lane Receiver DFE Tap 3 Coefficient<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Tap 3 DFE Coefficient <sup>2,3,4</sup>	(Default) Tap 3 DFE bias = 0 mV
x	x	x	0	0	0	0	1		Tap 3 DFE bias +1 Tap Step
x	x	x	0	0	0	1	0		Tap 3 DFE bias +2 Tap Steps
x	x	x	0	0	0	1	1		Tap 3 DFE bias +3 Tap Steps
x	x	x	0	0	1	0	0		Tap 3DFE bias +4 Tap Steps
x	x	x	0	0	1	0	1		Tap 3 DFE bias +5 Tap Steps
x	x	x	0	0	1	1	0		Tap 3 DFE bias +6 Tap Steps
x	x	x	0	0	1	1	1		Tap 3 DFE bias +7 Tap Steps
x	x	x	0	1	0	0	0		Tap 3 DFE bias +8 Tap Steps
x	x	x	0	1	0	0	1		Tap 3 DFE bias +9 Tap Steps
x	x	x	0	1	0	1	0		Tap 3 DFE bias +10 Tap Steps
x	x	x	0	1	0	1	1		Tap 3DFE bias +11 Tap Steps
x	x	x	0	1	1	0	0		Tap 3 DFE bias +12 Tap Steps
x	x	x	0	1	1	0	1		Tap 3DFE bias +13 Tap Steps
x	x	x	0	1	1	1	0		Tap 3 DFE bias +14 Tap Steps
x	x	x	0	1	1	1	1		Tap 3 DFE bias +15 Tap Steps
x	x	x	.....						.....
x	x	x	1	1	1	0	0		Tap 3 DFE bias +28 Tap Steps
x	x	x	1	1	1	0	1		Tap 3 DFE bias +29 Tap Steps
x	x	x	1	1	1	1	0		Tap 3 DFE bias +30 Tap Steps
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	
x	x	1	x	x	x	x	x	Reserved	
x	0	x	x	x	x	x	x	Reserved	
x	1	x	x	x	x	x	x	Reserved	
0	x	x	x	x	x	x	x	Tap 3 Coefficient Sign Bit	(Default) Positive Tap 3 DFE bias when Tap 3 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 3 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 3 DFE bias when Tap 3 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 3 post-cursor)

NOTE 1 Table 70 and Table 71 illustrate the assignment of each control word in the PG[5:4]RW[E3,EB,F3,FB] group to the corresponding input pin it controls.

NOTE 2 Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification

NOTE 3 Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 60, “DFE Gain and Tap Coefficient Step Parameters,”

NOTE 4 PG[5:4]RW[E3,EB,F3,FB] will be sticky, cleared by power cycle not reset.

### 11.17.5 PG[5:4]RW[E4,EC,F4,FC] DQ[7:0] and PG[F]RWF3 CRC Lane Receiver DFE Tap 4 Coefficients

**Table 161 — PG[5:4]RW[E4,EC,F4,FC] DQ[7:0] and PG[F]RWF3 CRC Lane Receiver DFE Tap 4 Coefficients<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Tap 4 DFE Coefficient <sup>2,3,4</sup>	(Default) Tap 4 DFE bias = 0 mV
x	x	x	0	0	0	0	1		Tap 4 DFE bias +1 Tap Steps
x	x	x	0	0	0	1	0		Tap 4 DFE bias +2 Tap Steps
x	x	x	0	0	0	1	1		Tap 4 DFE bias +3 Tap Steps
x	x	x	0	0	1	0	0		Tap 4 DFE bias +4 Tap Steps
x	x	x	0	0	1	0	1		Tap 4 DFE bias +5 Tap Steps
x	x	x	0	0	1	1	0		Tap 4 DFE bias +6 Tap Steps
x	x	x	0	0	1	1	1		Tap 4 DFE bias +7 Tap Steps
x	x	x	0	1	0	0	0		Tap 4 DFE bias +8 Tap Steps
x	x	x	0	1	0	0	1		Tap 4 DFE bias +9 Tap Steps
x	x	x	0	1	0	1	0		Tap 4 DFE bias +10 Tap Steps
x	x	x	0	1	0	1	1		Tap 4 DFE bias +11 Tap Steps
x	x	x	0	1	1	0	0		Tap 4 DFE bias +12 Tap Steps
x	x	x	0	1	1	0	1		Tap 4 DFE bias +13 Tap Steps
x	x	x	0	1	1	1	0		Tap 4 DFE bias +14 Tap Steps
x	x	x	0	1	1	1	1		Tap 4 DFE bias +15 Tap Steps
x	x	x	.....						.....
x	x	x	1	1	1	0	0		Tap 4 DFE bias +28 Tap Steps
x	x	x	1	1	1	0	1		Tap 4 DFE bias +29 Tap Steps
x	x	x	1	1	1	1	0		Tap 4 DFE bias +30 Tap Steps
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	
x	x	1	x	x	x	x	x	Reserved	
x	0	x	x	x	x	x	x	Reserved	
x	1	x	x	x	x	x	x	Reserved	
0	x	x	x	x	x	x	x	Tap 4 Coefficient Sign Bit	(Default) Positive Tap 4 DFE bias when Tap 4 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 4 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 4 DFE bias when Tap 4 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 4 post-cursor)

NOTE 1 Table 70 and Table 71 illustrate the assignment of each control word in the PG[5:4]RW[E4,EC,F4,FC] group to the corresponding input pin it controls.

NOTE 2 Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification.

NOTE 3 Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 60, “DFE Gain and Tap Coefficient Step Parameters.”

NOTE 4 PG[5:4]RW[E4,EC,F4,FC] will be sticky, cleared by power cycle not reset.

### 11.17.6 PG[5:4]RW[E5,ED,F5,FD] DQ[7:0] and PG[F]RWF4 CRC Lane Receiver DFE Tap 5 Coefficients

Table 162 — PG[5:4]RW[E5,ED,F5,FD] DQ[7:0] and PG[F]RWF4 CRC Lane Receiver DFE Tap 5 Coefficients<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Tap 5 DFE Coefficient <sup>2,3,4</sup>	(Default) Tap 5 DFE bias = 0 mV
x	x	x	0	0	0	0	1		Tap 5 DFE bias +1 Tap Steps
x	x	x	0	0	0	1	0		Tap 5 DFE bias +2 Tap Steps
x	x	x	0	0	0	1	1		Tap 5 DFE bias +3 Tap Steps
x	x	x	0	0	1	0	0		Tap 5 DFE bias +4 Tap Steps
x	x	x	0	0	1	0	1		Tap 5 DFE bias +5 Tap Steps
x	x	x	0	0	1	1	0		Tap 5 DFE bias +6 Tap Steps
x	x	x	0	0	1	1	1		Tap 5 DFE bias +7 Tap Steps
x	x	x	0	1	0	0	0		Tap 5 DFE bias +8 Tap Steps
x	x	x	0	1	0	0	1		Tap 5 DFE bias +9 Tap Steps
x	x	x	0	1	0	1	0		Tap 5 DFE bias +10 Tap Steps
x	x	x	0	1	0	1	1		Tap 5 DFE bias +11 Tap Steps
x	x	x	0	1	1	0	0		Tap 5 DFE bias +12 Tap Steps
x	x	x	0	1	1	0	1		Tap 5 DFE bias +13 Tap Steps
x	x	x	0	1	1	1	0		Tap 5 DFE bias +14 Tap Steps
x	x	x	0	1	1	1	1		Tap 5 DFE bias +15 Tap Steps
x	x	x	.....						.....
x	x	x	1	1	1	0	0		Tap 5 DFE bias +28 Tap Steps
x	x	x	1	1	1	0	1		Tap 5 DFE bias +29 Tap Steps
x	x	x	1	1	1	1	0		Tap 5 DFE bias +30 Tap Steps
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x	Reserved	Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x	Reserved	Reserved
0	x	x	x	x	x	x	x	Tap 5 Coefficient Sign Bit	(Default) Positive Tap 5 DFE bias when Tap 5 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 5 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 5 DFE bias when Tap 5 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 5 post-cursor)

NOTE 1 Table 70 and Table 71 illustrate the assignment of each control word in the PG[5:4]RW[E5,ED,F5,FD] group to the corresponding input pin it controls.

NOTE 2 Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification.

NOTE 3 Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 60, “DFE Gain and Tap Coefficient Step Parameters.”

NOTE 4 PG[5:4]RW[E5,ED,F5,FD] will be sticky, cleared by power cycle not reset.

### 11.17.7 PG[5:4]RW[E6,EE,F6,FE] DQ[7:0] and PG[F]RWF5 CRC Lane Receiver DFE Tap 6 Coefficients

Table 163 — PG[5:4]RW[E6,EE,F6,FE] DQ[7:0] and PG[F]RWF5 CRC Lane Receiver DFE Tap 6 Coefficients<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Tap 6 DFE Coefficient <sup>2,3,4</sup>	(Default) Tap 6 DFE bias = 0 mV
x	x	x	0	0	0	0	1		Tap 6 DFE bias +1 Tap Steps
x	x	x	0	0	0	1	0		Tap 6 DFE bias +2 Tap Steps
x	x	x	0	0	0	1	1		Tap 6 DFE bias +3 Tap Steps
x	x	x	0	0	1	0	0		Tap 6 DFE bias +4 Tap Steps
x	x	x	0	0	1	0	1		Tap 6 DFE bias +5 Tap Steps
x	x	x	0	0	1	1	0		Tap 6 DFE bias +6 Tap Steps
x	x	x	0	0	1	1	1		Tap 6 DFE bias +7 Tap Steps
x	x	x	0	1	0	0	0		Tap 6 DFE bias +8 Tap Steps
x	x	x	0	1	0	0	1		Tap 6 DFE bias +9 Tap Steps
x	x	x	0	1	0	1	0		Tap 6 DFE bias +10 Tap Steps
x	x	x	0	1	0	1	1		Tap 6 DFE bias +11 Tap Steps
x	x	x	0	1	1	0	0		Tap 6 DFE bias +12 Tap Steps
x	x	x	0	1	1	0	1		Tap 6 DFE bias +13 Tap Steps
x	x	x	0	1	1	1	0		Tap 6 DFE bias +14 Tap Steps
x	x	x	0	1	1	1	1		Tap 6 DFE bias +15 Tap Steps
x	x	x	.....						.....
x	x	x	1	1	1	0	0		Tap 6 DFE bias +28 Tap Steps
x	x	x	1	1	1	0	1		Tap 6 DFE bias +29 Tap Steps
x	x	x	1	1	1	1	0		Tap 6 DFE bias +30 Tap Steps
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x	Reserved	Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x	Reserved	Reserved
0	x	x	x	x	x	x	x	Tap 6 Coefficient Sign Bit	(Default) Positive Tap 6 DFE bias when Tap 6 post-cursor is Logic 1 (Negative bias for Logic 0 Tap6 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 6 DFE bias when Tap 6 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 6 post-cursor)

NOTE 1 Table 70 and Table 71 illustrate the assignment of each control word in the PG[5:4]RW[E6,EE,F6,FE] group to the corresponding input pin it controls.

NOTE 2 Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification.

NOTE 3 Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 60, “DFE Gain and Tap Coefficient Step Parameters.”

NOTE 4 PG[5:4]RW[E6,EE,F6,FE] will be sticky, cleared by power cycle not reset.

### 11.17.8 PG[6]RW[E0, E4, E8, EC, F0, F4, F8, FC] and PG[F]RWFB CRC Lane - DFE Error Counter Lower 8 Bits

Table 164 — PG[6]RW[E0, E4, E8, EC, F0, F4, F8, FC] and PG[F]RWFB CRC Lane - DFE Error Counter Lower 8 Bit

DFE Error Counter Lower 8 Bit Register <sup>1,2</sup>							
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

NOTE 1 Power on Default is OP[7:0] = 0.

NOTE 2 Read Only Register.

### 11.17.9 PG[6]RW[E1, E5, E9, ED, F1, F5, F9, FD] and PG[F]RWFC CRC Lane - DFE Error Counter Upper 8 Bits

Table 165 — PG[6]RW[E1, E5, E9, ED, F1, F5, F9, FD] and PG[F]RWFC CRC Lane - DFE Error Counter Upper 8 Bit

DFE Error Counter Upper 8 Bit Register <sup>1,2</sup>							
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
EC 15	EC 14	EC 13	EC 12	EC 11	EC 10	EC 9	EC 8

NOTE 1 Power on Default is OP[7:0] = 0.

NOTE 2 Read Only Register.

### 11.17.10 PG[6]RW[E2,E6,EA,EE,F2,F6,FA,FE] and PG[F]RWF9 CRC Lane - DFE\_Vref

Table 166 — PG[6]RW[E2,E6,EA,EE,F2,F6,FA,FE] and PG[F]RWF9 CRC Lane - DFE\_Vref<sup>1</sup>

PG[6]RW[E2, E6 ... FE]							DFE Training VREF in mV <sup>2,3,4</sup>							
OP7	OP6	OP5	OP4	OP3	OP2		PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF][0]= 1 (NEG Range)				PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF][0]= 0 (POS Range)			
							OP[1:0] = 00				OP[1:0] = 01			
							OP[1:0] = 00	OP[1:0] = 01	OP[1:0] = 10	OP[1:0] = 11	OP[1:0] = 00	OP[1:0] = 01	OP[1:0] = 10	OP[1:0] = 11
0	0	0	0	0	0		0.0	- 2.5	- 5.0	- 7.5	0.0	+ 2.5	+ 5.0	+ 7.5
0	0	0	0	0	1		- 10.0	- 12.5	- 15.0	- 17.5	+ 10.0	+ 12.5	+ 15.0	+ 17.5
0	0	0	0	1	0		- 20.0	- 22.5	- 25.0	- 27.5	+ 20.0	+ 22.5	+ 25.0	+ 27.5
0	0	0	0	1	1		- 30.0	- 32.5	- 35.0	- 37.5	+ 30.0	+ 32.5	+ 35.0	+ 37.5
0	0	0	1	0	0		- 40.0	- 42.5	- 45.0	- 47.5	+ 40.0	+ 42.5	+ 45.0	+ 47.5
0	0	0	1	0	1		- 50.0	- 52.5	- 55.0	- 57.5	+ 50.0	+ 52.5	+ 55.0	+ 57.5
0	0	0	1	1	0		- 60.0	- 62.5	- 65.0	- 67.5	+ 60.0	+ 62.5	+ 65.0	+ 67.5
0	0	0	1	1	1		- 70.0	- 72.5	- 75.0	- 77.5	+ 70.0	+ 72.5	+ 75.0	+ 77.5
0	0	1	0	0	0		- 80.0	- 82.5	- 85.0	- 87.5	+ 80.0	+ 82.5	+ 85.0	+ 87.5
0	0	1	0	0	1		- 90.0	- 92.5	- 95.0	- 97.5	+ 90.0	+ 92.5	+ 95.0	+ 97.5
0	0	1	0	1	0		- 100.0	- 102.5	- 105.0	- 107.5	+ 100.0	+ 102.5	+ 105.0	+ 107.5
0	0	1	0	1	1		- 110.0	- 112.5	- 115.0	- 117.5	+ 110.0	+ 112.5	+ 115.0	+ 117.5
0	0	1	1	0	0		- 120.0	- 122.5	- 125.0	- 127.5	+ 120.0	+ 122.5	+ 125.0	+ 127.5
0	0	1	1	0	1		- 130.0	- 132.5	- 135.0	- 137.5	+ 130.0	+ 132.5	+ 135.0	+ 137.5
0	0	1	1	1	0		- 140.0	- 142.5	- 145.0	- 147.5	+ 140.0	+ 142.5	+ 145.0	+ 147.5
0	0	1	1	1	1		- 150.0	- 152.5	- 155.0	- 157.5	+ 150.0	+ 152.5	+ 155.0	+ 157.5
0	1	0	0	0	0		- 160.0	- 162.5	- 165.0	- 167.5	+ 160.0	+ 162.5	+ 165.0	+ 167.5
0	1	0	0	0	1		- 170.0	- 172.5	- 175.0	- 177.5	+ 170.0	+ 172.5	+ 175.0	+ 177.5
0	1	0	0	1	0		- 180.0	- 182.5	- 185.0	- 187.5	+ 180.0	+ 182.5	+ 185.0	+ 187.5
0	1	0	0	1	1		- 190.0	- 192.5	- 195.0	- 197.5	+ 190.0	+ 192.5	+ 195.0	+ 197.5



Table 166 — PG[6]RW[E2,E6,EA,EE,F2,F6,FA,FE] and PG[F]RWF9 CRC Lane - DFE\_Vref<sup>1</sup> (cont'd)

PG[6]RW[E2, E6 ... FE]						DFE Training VREF in mV <sup>2,3,4</sup>							
OP7	OP6	OP5	OP4	OP3	OP2	PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF][0]=1 (NEG Range)				PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF][0]=0 (POS Range)			
						OP[1:0] = 00	OP[1:0] = 01	OP[1:0] = 10	OP[1:0] = 11	OP[1:0] = 00	OP[1:0] = 01	OP[1:0] = 10	OP[1:0] = 11
0	1	0	1	0	0	-200.0	-202.5	-205.0	-207.5	+200.0	+202.5	+205.0	+207.5
0	1	0	1	0	1	-210.0	-212.5	-215.0	-217.5	+210.0	+212.5	+215.0	+217.5
0	1	0	1	1	0	-220.0	-222.5	-225.0	-227.5	+220.0	+222.5	+225.0	+227.5
0	1	0	1	1	1	-230.0	-232.5	-235.0	-237.5	+230.0	+232.5	+235.0	+237.5
0	1	1	0	0	0	-240.0	-242.5	-245.0	-247.5	+240.0	+242.5	+245.0	+247.5
0	1	1	0	0	1	-250.0	-252.5	-255.0	-257.5	+250.0	+252.5	+255.0	+257.5
0	1	1	0	1	0	-260.0	-262.5	-265.0	-267.5	+260.0	+262.5	+265.0	+267.5
0	1	1	0	1	1	-270.0	-272.5	-275.0	-277.5	+270.0	+272.5	+275.0	+277.5
0	1	1	1	0	0	-280.0	-282.5	-285.0	-287.5	+280.0	+282.5	+285.0	+287.5
0	1	1	1	0	1	-290.0	-292.5	-295.0	-297.5	+290.0	+292.5	+295.0	+297.5
0	1	1	1	1	0	-300.0	-302.5	-305.0	-307.5	+300.0	+302.5	+305.0	+307.5
0	1	1	1	1	1	-310.0	-312.5	-315.0	-317.5	+310.0	+312.5	+315.0	+317.5
1	0	0	0	0	0	-320.0	-322.5	-325.0	-327.5	+320.0	+322.5	+325.0	+327.5
1	0	0	0	0	1	-330.0	-332.5	-335.0	-337.5	+330.0	+332.5	+335.0	+337.5
1	0	0	0	1	0	-340.0	-342.5	-345.0	-347.5	+340.0	+342.5	+345.0	+347.5
1	0	0	0	1	1	-350.0	-352.5	-355.0	-357.5	+350.0	+352.5	+355.0	+357.5
1	0	0	1	0	0	-360.0	-362.5	-365.0	-367.5	+360.0	+362.5	+365.0	+367.5
1	0	0	1	0	1	-370.0	-372.5	-375.0	-377.5	+370.0	+372.5	+375.0	+377.5
1	0	0	1	1	0	-380.0	-382.5	-385.0	-387.5	+380.0	+382.5	+385.0	+387.5
1	0	0	1	1	1	-390.0	-392.5	-395.0	-397.5	+390.0	+392.5	+395.0	+397.5
1	0	1	0	0	0	-400.0	-402.5	-405.0	-407.5	+400.0	+402.5	+405.0	+407.5
1	0	1	0	0	1	-410.0	-412.5	-415.0	-417.5	+410.0	+412.5	+415.0	+417.5
1	0	1	0	1	0	-420.0	-422.5	-425.0	-427.5	+420.0	+422.5	+425.0	+427.5
1	0	1	0	1	1	-430.0	-432.5	-435.0	-437.5	+430.0	+432.5	+435.0	+437.5
1	0	1	1	0	0	-440.0	-442.5	-445.0	-447.5	+440.0	+442.5	+445.0	+447.5
1	0	1	1	0	1	-450.0	-452.5	-455.0	-457.5	+450.0	+452.5	+455.0	+457.5
1	0	1	1	1	0	-460.0	-462.5	-465.0	-467.5	+460.0	+462.5	+465.0	+467.5
1	0	1	1	1	1	-470.0	-472.5	-475.0	-477.5	+470.0	+472.5	+475.0	+477.5
1	1	0	0	0	0	-480.0	-482.5	-485.0	-487.5	+480.0	+482.5	+485.0	+487.5
1	1	0	0	0	1	-490.0	-492.5	-495.0	-497.5	+490.0	+492.5	+495.0	+497.5
1	1	0	0	1	0	-500.0	Reserved	Reserved	Reserved	+500.0	Reserved	Reserved	Reserved
1	1	0	0	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	0	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	0	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	1	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	0	1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	0	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	0	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	1	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	0	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	0	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	1	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

NOTE 1 Table 72 illustrates the assignment of each control word in the PG[6]RW[E2,E6,EA,EE,F2,F6,FA,FE] group to the corresponding input pin it controls.

NOTE 2 These are target DFE\_Vref values. Acceptable actual values are determined based on tolerances defined in electrical section.

NOTE 3 The target DFE\_Vref values shown in this table are input referred.

NOTE 4 Each input receiver has a dedicated DFE\_Vref control word. Any number of DFE\_Vref monitors are allowed to be enabled at the same time in each sub-channel.

### 11.17.11 PG[6]RW[E3,E7,EB,EF,F3,F7,FB,FF] and PG[F]RWFA CRC Lane - Sign Bit Dn DFE\_Vref Control Word

**Table 167 — PG[6]RW[E3, E7, EB, EF, F3, F7, FB, FF] and PG[F]RWFA CRC Lane - Sign Bit Dn DFE\_Vref Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Dn Sign DFE_Vref	Positive
x	x	x	x	x	x	x	1		Negative
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 Table 72 illustrates the assignment of each control word in the PG[6][E3, E7, EB, EF, F3, F7, FB, FF] group to the corresponding input pin it controls.

### 11.17.12 PG[74,7]RW[EF:E0]- MDQ Error Counters Control Words

PG[7]RW[EF:E0] are for PS0 or {R0, R1} group and PG[74]RW[EF:E0] are for PS1 or {R2, R3} group

**Table 168 — PG[74,7]RW[EF:E0]:MDQ Error Counters Control Words<sup>1,2,3</sup>**

RW	Description	Encoding
PG[74,7]RW[E0,E2,E4,E6,E8,EA,EC,EE]	MDQ Read Error Counter Lower 8 Bits (Read Only)	Least Significant byte (bits[7:0] of the 16-bit MDQ Read Error Counter value)
PG[74,7]RW[E1,E3,E5,E7,E9,EB,ED,EF]	MDQ Read Error Counter Upper 8 Bits (Read Only)	Most Significant byte (bits[15:8] of the 16-bit MDQ Read Error Counter value)

NOTE 1 The MDQ read error counters are Enabled only with RW83 MRD or MWD are set.

NOTE 2 The counters maintain their state independent of MRD/MWD entry/exit.

NOTE 3 Table 73 and Table 88 illustrate the assignment of each control word in the PG[74,7]RW[EF:E0] group to the corresponding input pin it controls.

### 11.17.13 PG[7]RWF0 - MDQ Error Counters Reset Control Word

PG[7]RWF0[0] is for both PS0 and PS1 in Mux mode, or all ranks in Rank mode.

**Table 169 — PG[7]RWF0 - MDQ Error Counters Reset Control Word**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	MDQ Error counters Reset	All per-bit MDQ read error counters operate normally.
x	x	x	x	x	x	x	1		All per-bit MDQ read error counters are reset to zero. This bit is self-clearing in the next cycle
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

## 11.18 Paged Snooped Control Words PG[8]RW[ED:E0] - Snooped Control Words

Table 170 — PG[8]RW[ED:E0]- Snooped Control Word

Control Word	MR	Pseudo Channel or Rank Group	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PG[8]RWE0	MR0	Both	RFU	CAS Latency					Burst Length	
PG[8]RWE1	MR8	Both	DRAM WR Postamble	DRAMRD Postamble	RFU	DRAM Interface WR Preamble		DRAM Interface RD Preamble		
PG[8]RWE2	MR25	Encoded in bits	RFU	LFSR1 PS1 or {R2, R3} group	LFSR0 PS1 or {R2, R3} group	RD Training PS1 or {R2, R3} group	RFU	LFSR1 PS0 or {R0, R1} group	LFSR0 PS0 or {R0, R1} group	RD Training PS0 or {R0, R1} group
PG[8]RWE3	MR26	PS0 or {R0, R1} group	UI7	UI6	UI5	UI4	UI3	UI2	UI1	UI0
PG[8]RWE4	MR27	PS0 or {R0, R1} group	UI7	UI6	UI5	UI4	UI3	UI2	UI1	UI0
PG[8]RWE5	MR28	PS0 or {R0, R1} group	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
PG[8]RWE6	MR30	PS0 or {R0, R1} group	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
PG[8]RWE7	MR45	Both	DQS Interval Timer Run Time							
PG[8]RWE8	MR50	Both, for Rank mode only	RFU	RFU	Not Used	Not Used	Not Used	WR CRC Enable Upper nibble (x8 only)	WR CRC Enable Lower nibble (x4 and x8)	RD CRC Enable
PG[8]RWE9	MR26	PS1 or {R2, R3} group	UI7	UI6	UI5	UI4	UI3	UI2	UI1	UI0
PG[8]RWEA	MR27	PS1 or {R2, R3} group	UI7	UI6	UI5	UI4	UI3	UI2	UI1	UI0
PG[8]RWEB	MR28	PS1 or {R2, R3} group	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
PG[8]RWEC	MR30	PS1 or {R2, R3} group	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
PG[8]RWED	MR8	Both	Host Interface WR Postamble	Host Interface RD Postamble	RFU	Host Interface WR Preamble		Host Interface RD Preamble		

MRW commands to MR8 will update both PG[8]RWE1 and PG[8]RWED. For the MDB, PG[8]RWE1 provides the DRAM side preamble and postamble while PG[8]RWED provides the Host side preamble and postamble. A write to MR8 in the DRAM space will update BOTH of these registers. To change the Host side preamble and/or postamble, MDB PG[8]RWED must be written after the last DRAM MR8 MRW. The MDB does not support 1 t<sub>HDQS</sub> or 2 t<sub>HDQS</sub> preambles on the Host side regardless of Rank mode or Mux mode. If the DRAMs are configured to use 1- or 2-cycle preambles, resulting in invalid settings snooped into PG[8]RWED, the Host must reprogram PG[8]RWED and/or PG[70]RW[F5:F4][2:0] to use a minimum of 3 t<sub>HDQS</sub> preambles on the Host side. The behavior of the MDB when programmed to invalid settings for preamble length is undefined. It may, for example, use the minimum length of 3 t<sub>HDQS</sub>.

MR25, 26, 27, 28, and 30 have separate snoop registers or bits per pseudo-channel. The MRW BCOM command does not have the pseudo-channel information included. PG[70]RWE4 bits 3 and 4 determine which pseudo-channel(s) are the target of the MRW commands for these snoop values in the Mux mode. For the MDB to perform the MRW Snoop function in the Rank mode properly, the SOC Controller should 1). Set PG[70]RWE4[4:3]='11'; 2). Configure the same MR25~MR30 values for all the four ranks. Paged DFE Training Accelerator Control Words

### 11.18.1 PG[9]RWE0 - DFETA Training Mode Control Word

Table 171 — PG[9]RWE0 DFETA Training Mode Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DFE Training Accelerator	Stop DFE Training Accelerator (default)
x	x	x	x	x	x	x	1		Start DFE Training Accelerator
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	0	0	x	x	Select Inner Loop Parameter	Select Inner Loop Parameter - NULL <sup>1</sup>
x	x	x	x	0	1	x	x		Select Inner Loop Parameter - DFE Vref
x	x	x	x	1	0	x	x		Select Inner Loop Parameter - VrefDQ
x	x	x	x	1	1	x	x		Reserved
0	0	0	0	x	x	x	x	Select Outer Loop Parameter	Select Outer Loop Parameter - NULL
0	0	0	1	x	x	x	x		Select Outer Loop Parameter - Tap 1
0	0	1	0	x	x	x	x		Select Outer Loop Parameter - Tap 2
0	0	1	1	x	x	x	x		Select Outer Loop Parameter - Tap 3
0	1	0	0	x	x	x	x		Select Outer Loop Parameter - Tap 4
0	1	0	1	x	x	x	x		Select Outer Loop Parameter - Tap5
0	1	1	0	x	x	x	x		Select Outer Loop Parameter - Tap6
0	1	1	1	x	x	x	x		Select Outer Loop Parameter - Tap7
1	0	0	0	x	x	x	x		Select Outer Loop Parameter - Tap8
1	0	0	1	x	x	x	x		Reserved
1	.	.	.	x	x	x	x		Reserved
1	1	1	1	x	x	x	x		Reserved

NOTE 1 NULL parameter choice means no change. NULL parameter loop can have multiple iterations.

### 11.18.2 PG[9]RWE1 - DFETA Inner Loop Start Value Bit [7:0]Control Word

DFETA Inner Loop Start Value is a 9-bit field. The Lower bits 7:0 are in PG[9]RWE1 and the upper bit located in PG[9]RWE2.

Table 172 — PG[9]RWE1 - DFETA Inner Loop Start Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Start Value <sup>1</sup>	Inner Loop Start Value = 0x00
0	0	0	0	0	0	0	1		Inner Loop Start Value = 0x01
0	0	0	0	0	0	1	0		Inner Loop Start Value = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Start Value = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Start Value = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Start Value = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Start Value = 0xFF

NOTE 1 Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.

### 11.18.3 PG[9]RWE2 - DFETA Inner Loop Start Value Bit [8]Control Word

Table 173 — PG[9]RWE2 - DFETA Inner Loop Start Value Bit [8]Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Inner Loop Start Value <sup>1</sup>	Inner Loop Start Value = 0x0
x	x	x	x	x	x	x	1		Inner Loop Start Value = 0x1
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.

### 11.18.4 PG[9]RWE3- DFETA Outer Loop Start Value Control Word

Table 174 — PG[9]RWE3: DFETA Outer Loop Start Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Outer Loop Start Value <sup>1,2</sup>	Outer Loop Start Value = 0x00
0	0	0	0	0	0	0	1		Outer Loop Start Value = 0x01
0	0	0	0	0	0	1	0		Outer Loop Start Value = 0x02
...									...
1	1	1	1	1	1	0	0		Outer Loop Start Value = 0xFC
1	1	1	1	1	1	0	1		Outer Loop Start Value = 0xFD
1	1	1	1	1	1	1	0		Outer Loop Start Value = 0xFE
1	1	1	1	1	1	1	1		Outer Loop Start Value = 0xFF

NOTE 1 Depending on the Outer Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Outer Loop Parameter.

NOTE 2 Even though the tap setting parameter registers are defined as signed magnitude fields, this start value is a two's complement encoding. The MDB must convert this value to a signed magnitude format prior to updating the tap setting when Tap1, Tap2, Tap3, or Tap4 is chosen for the Outer Loop Parameter.

### 11.18.5 PG[9]RWE4- DFETA Inner Loop Current Value Bit [7:0] Control Word

Table 175 — PG[9]RWE4: DFETA Inner Loop Current Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Current Value. (Read Only)	Inner Loop Current Value = 0x00
0	0	0	0	0	0	0	1		Inner Loop Current Value = 0x01
0	0	0	0	0	0	1	0		Inner Loop Current Value = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Current Value = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Current Value = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Current Value = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Current Value = 0xFF

### 11.18.6 PG[9]RWE5- DFETA Inner Loop Current Value Bit [8]Control Word

Table 176 — PG[9]RWE5 - DFETA Inner Loop Current Value Bit [8]Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Inner Loop Current Value <sup>1</sup> (Read Only)	Inner Loop Current Value = 0x0
x	x	x	x	x	x	x	1		Inner Loop Current Value = 0x1
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.

### 11.18.7 PG[9]RWE6 - DFETA Outer Loop Current Value Control Word

Table 177 — RW[9]RWE6: DFETA Outer Loop Current Value Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Outer Loop Current Value. (Read Only)	Outer Loop Current Value = 0x00
0	0	0	0	0	0	0	1		Outer Loop Current Value = 0x01
0	0	0	0	0	0	1	0		Outer Loop Current Value = 0x02
...									...
1	1	1	1	1	1	0	0		Outer Loop Current Value = 0xFC
1	1	1	1	1	1	0	1		Outer Loop Current Value = 0xFD
1	1	1	1	1	1	1	0		Outer Loop Current Value = 0xFE
1	1	1	1	1	1	1	1		Outer Loop Current Value = 0xFF

## 11.18.8 PG[9]RWE7 - DFETA Inner and Outer Loop Step Size Control Word

Table 178 — PG[9]RWE7: DFETA Inner and Outer Loop Step Size Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Inner Loop Step Size <sup>1</sup>	Inner Loop Step Size = 1
x	x	x	x	0	0	0	1		Inner Loop Step Size = 2
x	x	x	x	0	0	1	0		Inner Loop Step Size = 3
x	x	x	x	0	0	1	1		Inner Loop Step Size = 4
x	x	x	x	0	1	0	0		Inner Loop Step Size = 5
x	x	x	x	0	1	0	1		Inner Loop Step Size = 6
x	x	x	x	0	1	1	0		Inner Loop Step Size = 7
x	x	x	x	0	1	1	1		Inner Loop Step Size = 8
x	x	x	x	1	0	0	0		Inner Loop Step Size = 9
x	x	x	x	1	0	0	1		Inner Loop Step Size = 10
x	x	x	x	1	0	1	0		Inner Loop Step Size = 11
x	x	x	x	1	0	1	1		Inner Loop Step Size = 12
x	x	x	x	1	1	0	0		Inner Loop Step Size = 13
x	x	x	x	1	1	0	1		Inner Loop Step Size = 14
x	x	x	x	1	1	1	0		Inner Loop Step Size = 15
x	x	x	x	1	1	1	1		Inner Loop Step Size = 16
0	0	0	0	x	x	x	x	Outer Loop Step Size <sup>1</sup>	Outer Loop Step Size = 1
0	0	0	1	x	x	x	x		Outer Loop Step Size = 2
0	0	1	0	x	x	x	x		Outer Loop Step Size = 3
0	0	1	1	x	x	x	x		Outer Loop Step Size = 4
0	1	0	0	x	x	x	x		Outer Loop Step Size = 5
0	1	0	1	x	x	x	x		Outer Loop Step Size = 6
0	1	1	0	x	x	x	x		Outer Loop Step Size = 7
0	1	1	1	x	x	x	x		Outer Loop Step Size = 8
1	0	0	0	x	x	x	x		Outer Loop Step Size = 9
1	0	0	1	x	x	x	x		Outer Loop Step Size = 10
1	0	1	0	x	x	x	x		Outer Loop Step Size = 11
1	0	1	1	x	x	x	x		Outer Loop Step Size = 12
1	1	0	0	x	x	x	x		Outer Loop Step Size = 13
1	1	0	1	x	x	x	x		Outer Loop Step Size = 14
1	1	1	0	x	x	x	x		Outer Loop Step Size = 15
1	1	1	1	x	x	x	x		Outer Loop Step Size = 16

NOTE 1 The step size is always positive, and thus the increment is always from lowest to highest value in the sweep. Note that the actual field setting indicates the Step Size – 1. The MDB must account for this in the increment logic.



### 11.18.9 PG[9]RWE8 - DFETA Inter Loop Number of Increments Bit [7:0]Control Word

Table 179 — PG[9]RWE8: DFETA Inter Loop Number of Increments Bit [7:0] Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Number of Increments <sup>1</sup>	Inner Loop Number of Increments = 0x00
0	0	0	0	0	0	0	1		Inner Loop Number of Increments = 0x01
0	0	0	0	0	0	1	0		Inner Loop Number of Increments = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Number of Increments = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Number of Increments = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Number of Increments = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Number of Increments = 0xFF

NOTE 1 Depending on the Inner Loop Parameter Selection and the Inner Loop Step Size, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter. When the Number of Increments = 0x00, the Start Value will be applied for a single iteration of the loop.

### 11.18.10 PG[9]RWE9 - DFETA Inter Loop Number of Increments Bit [8]Control Word

Table 180 — PG[9]RWE9 - DFETA Inner Loop Start Value Bit [8]Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Inner Loop Number of Increments <sup>1</sup>	Inner Loop Number of Increments = 0x0
x	x	x	x	x	x	x	1		Inner Loop Number of Increments = 0x1
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.

### 11.18.11 PG[9]RWEA - DFETA Outer Loop Number of Increments Control Word

Table 181 — PG[9]RWEA: DFETA Outer Loop Number of Increments Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Outer Loop Number of Increments <sup>1</sup>	Outer Loop Number of Increments = 0x00
0	0	0	0	0	0	0	1		Outer Loop Number of Increments = 0x01
0	0	0	0	0	0	1	0		Outer Loop Number of Increments = 0x02
...									...
1	1	1	1	1	1	0	0		Outer Loop Number of Increments = 0xFC
1	1	1	1	1	1	0	1		Outer Loop Number of Increments = 0xFD
1	1	1	1	1	1	1	0		Outer Loop Number of Increments = 0xFE
1	1	1	1	1	1	1	1		Outer Loop Number of Increments = 0xFF

NOTE 1 Depending on the Outer Loop Parameter Selection and the Outer Loop Step Size, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Outer Loop Parameter. When the Number of Increments = 0x00, the Start Value will be applied for a single iteration of the loop.

### 11.18.12 PG[9]RWEB - DFETA Inner Loop Current Increment Bit [7:0] Status Control Word

Table 182 — PG[9]RWEB: DFETA Inner Loop Current Increment Bit [7:0] Status Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Inner Loop Current Increment (Read Only)	Inner Loop Current Increment = 0x00
0	0	0	0	0	0	0	1		Inner Loop Current Increment = 0x01
0	0	0	0	0	0	1	0		Inner Loop Current Increment = 0x02
...									...
1	1	1	1	1	1	0	0		Inner Loop Current Increment = 0xFC
1	1	1	1	1	1	0	1		Inner Loop Current Increment = 0xFD
1	1	1	1	1	1	1	0		Inner Loop Current Increment = 0xFE
1	1	1	1	1	1	1	1		Inner Loop Current Increment = 0xFF

### 11.18.13 PG[9]RVEC - DFETA Inner Loop Current Increment Bit [8] Status Control Word

Table 183 — PG[9]RVEC - DFETA Inner Loop Current Increment Bit [8] Status Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Inner Loop Current Increment (Read Only) <sup>1</sup>	Inner Loop Current Increment = 0x0
x	x	x	x	x	x	x	1		Inner Loop Current Increment = 0x1
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 Depending on the Inner Loop Parameter Selection, the range may be limited. The DFE Accelerator will only apply the OP bits that are within range for the specific Inner Loop Parameter.

### 11.18.14 PG[9]RWED - DFETA Outer Loop Current Increment Status Control Word

Table 184 — PG[9]RWED: DFETA Outer Loop Current Increment Status Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	Outer Loop Current Increment (Read Only)	Outer Loop Current Increment = 0x00
0	0	0	0	0	0	0	1		Outer Loop Current Increment = 0x01
0	0	0	0	0	0	1	0		Outer Loop Current Increment = 0x02
...									...
1	1	1	1	1	1	0	0		Outer Loop Current Increment = 0xFC
1	1	1	1	1	1	0	1		Outer Loop Current Increment = 0xFD
1	1	1	1	1	1	1	0		Outer Loop Current Increment = 0xFE
1	1	1	1	1	1	1	1		Outer Loop Current Increment = 0xFF

**11.18.15 PG[9]RW[F1:EE] - DFETA Write Limit and Counter Control Words****Table 185 — PG[9]RW[F1:EE]- DFETA Write Limit and Counter Control Words**

Control Word	Definition	Encoding
RWEE[7:0]	Write Limit Value - Lower Byte	The write limit value is computed as $RW\_WriteLimitUpperByte[7:0] * 256 + RW\_WriteLimitLowerByte[7:0] + 1$
RWEF[7:0]	Write Limit Value - Upper Byte	The write limit value is computed as $RW\_WriteLimitUpperByte[7:0] * 256 + RW\_WriteLimitLowerByte[7:0] + 1$
RWF0[7:0]	Write Limit Counter Value Status - Lower Byte (Read Only)	The current value of the write limit counter's lower byte.
RWF1[7:0]	Write Limit Counter Value Status - Upper Byte (Read Only)	The current value of the write limit counter's upper byte.

## 11.19 Paged Periodic Update Registers

### 11.19.1 PG[A,71]RW[E7:E0] - Initial DRAM DQS Oscillator Counter Value

Table 186 — PG[71,A] RW[E7:E0] -Initial DRAM DQS Oscillator Counter Value<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
OC 07	OC 06	OC 05	OC 04	OC 03	OC 02	OC 01	OC 00	initial DRAM DQS oscillator counter value <sup>2</sup>	If DRAM tDQS2DQ tracking initialization mode is enabled, this register is written with the read data that is captured from the DRAM as a result of a DRAM-space MRR. Otherwise, it is unaltered. This register can also be written by a DB-space MRW operation and read by a DB-space MRR operation. This register defaults to 8'h00.

NOTE 1 Table 76 and Table 87 illustrate the assignment of each control word in the PG[A,71]RW[E7:E0] group to the corresponding rank and nibble it controls.

NOTE 2 PG[A,71]RW[E7:E0] will be sticky, cleared by power cycle, or RWB0[1], not reset.

### 11.19.2 PG[A,71]RW[EF:E8] - Initial DRAM DQS Clock Tree Delay Value

Table 187 — PG[71,A]RW[EF:E8] - Initial DRAM DQS Clock Tree Delay Value<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
OC 07	OC 06	OC 05	OC 04	OC 03	OC 02	OC 01	OC 00	Initial DRAM DQS clock tree delay value <sup>2</sup>	If DRAM tDQS2DQ tracking initialization mode is enabled, this register is written by the MDB hardware with the calculated DQS clock tree delay value for the DRAM. Otherwise, it is unaltered. This register can be read by a DB-space MRR operation. This register defaults to 8'h00.

NOTE 1 Table 76 and Table 87 illustrate the assignment of each control word in the PG[71,A]RW[EF:E8] group to the corresponding rank and nibble it controls.

NOTE 2 PG[71,A]RW[EF:E8] will be sticky, cleared by power cycle or RWB0[1], not reset.

### 11.19.3 PG[A,71]RW[F7:F0] - Current DRAM DQS Oscillator Counter

Table 188 — PG[71,A]RW[F7:F0] - Current DRAM DQS Oscillator Counter<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
OC 07	OC 06	OC 05	OC 04	OC 03	OC 02	OC 01	OC 00	The current DRAM DQS oscillator counter value <sup>2</sup>	This register is written with the read data that is captured from the DRAM as a result of a DRAM-space MRR to its DQS OSC Counter register in either of the tDQS2DQ tracking modes. Otherwise, it is unaltered. This register can also be written by a DB-space MRW operation and read by a DB-space MRR operation. This register defaults to 8'h00.

NOTE 1 Table 76 and Table 87 illustrate the assignment of each control word in the PG[A,71]RW[F7:F0] group to the corresponding rank and nibble it controls.

NOTE 2 PG[A,71]RW[F7:F0] will be sticky, cleared by power cycle or RWB0[1], not reset.

### 11.19.4 PG[A,71]RW[FF:F8] - Current DRAM DQS Clock Tree Delay Value

**Table 189 — PG[71,A]RW[FF:F8] - Current DRAM DQS Clock Tree Delay Value<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
OC 07	OC 06	OC 05	OC 04	OC 03	OC 02	OC 01	OC 00	The current DRAM DQS Clock Tree Delay. <sup>2</sup>	This register is written by the MDB hardware with the calculated DQS clock tree delay LSB value for the lower nibble, rank-0 DRAM in either of the tDQS2DQ tracking modes. Otherwise, it is unaltered. This register can be read by a DB-space MRR operation. This register defaults to 8'h00

NOTE 1 Table 76 and Table 87 illustrate the assignment of each control word in the PG[A,71]RW[FF:F8] group to the corresponding rank and nibble it controls.

NOTE 2 PG[A,71]RW[FF:F8] will be sticky, cleared by power cycle or RWB0[1], not reset.

## 11.20 Paged DCA Control Words

### 11.20.1 PG[C]RW[E0]: DCA Configuration Control Word

**Table 190 — PG[C]RW[E0]: DCA Configuration Control Word**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DCA (Duty Cycle Adjuster) Configuration (Read-Only)	DCA Configuration_0 is supported by the vendor. All registers listed in Table 77 are defined. PG[C]RW[F5:F0, FD:F8] are defined in Table 192
x	x	x	x	x	x	x	1		DCA Configuration_1 is supported by the vendor. All registers listed in Table 77 are defined except for PG[C]RW[E2, E4, F0, F1, F8, F9] which are reserved and have no function. PG[C]RW[F5:F2, FD:FA] are defined in Table 193
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

## 11.20.2 PG[C]RW[E4:E1]: Per-Nibble DCA Control Words

Table 191 — PG[C]RW[E4:E1]: Per-Nibble DCA Control Words

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	DCA Adjustment Steps <sup>1,2</sup>	DCA Adjustment = 0 (default)
x	x	x	x	0	0	0	1		DCA Adjustment = +1
x	x	x	x	0	0	1	0		DCA Adjustment = +2
x	x	x	x	0	0	1	1		DCA Adjustment = +3
x	x	x	x	...					...
x	x	x	x	0	1	1	1		DCA Adjustment = +7
x	x	x	x	1	0	0	0		DCA Adjustment = 0 (same as default)
x	x	x	x	1	0	0	1		DCA Adjustment = -1
x	x	x	x	1	0	1	0		DCA Adjustment = -2
x	x	x	x	...					...
x	x	x	x	1	1	1	1		DCA Adjustment = -7
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 PG[C]RW[E4:E1] will be sticky, cleared by power cycle not reset.

NOTE 2 When PG[C]RWE0[0] = 1, PG[C]RW[E1, E3] are active and functional, while PG[C]RW[E2, E4] have no function.

### 11.20.3 PG[C]RW[F5:F0,FD:F8]: Per-Pin DCA Control Words

#### 11.20.3.1 PG[C]RW[F5:F0,FD:F8]: Per-Pin DCA Control Words when PG[C]RWE0[0] = 0

Table 192 — PG[C]RW[F5:F0,FD:F8]: Per-Pin DCA Control Words when PG[C]RWE0[0] = 0

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	DCA Adjustment Steps PG[C]RWE0[0] = 0 <sup>1</sup>	DCA Adjustment = 0 (default)
x	x	x	x	x	0	0	1		DCA Adjustment = +1
x	x	x	x	x	0	1	0		DCA Adjustment = +2
x	x	x	x	x	0	1	1		DCA Adjustment = +3
x	x	x	x	x	1	0	0		DCA Adjustment = 0 (same as default)
x	x	x	x	x	1	0	1		DCA Adjustment = -1
x	x	x	x	x	1	1	0		DCA Adjustment = -2
x	x	x	x	x	1	1	1		DCA Adjustment = -3
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 PG[C]RW[F5:F0,FD:F8] will be sticky, cleared by power cycle not reset.



**11.20.3.2 PG[C]RW[F5:F2,FD:FA]: Per-Pin DCA Control Words when PG[C]RWE0[0] = 1**

When PG[C]RWE0[0] = 1, PG[C]RW[E2, E4, F0, F1, F8, F9] are reserved and have no function.

**Table 193 — PG[C]RW[F5:F2,FD:FA]: Per-Pin DCA Control Words when PG[C]RWE0[0] = 1**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	DCA Adjustment Steps when $PG[C]RWE0[0] = 1^1$	DCA Adjustment = 0 (default)
x	x	x	x	0	0	0	1		DCA Adjustment = +1
x	x	x	x	0	0	1	0		DCA Adjustment = +2
x	x	x	x	0	0	1	1		DCA Adjustment = +3
x	x	x	x	...					...
x	x	x	x	0	1	1	1		DCA Adjustment = +7
x	x	x	x	1	0	0	0		DCA Adjustment = 0 (same as default)
x	x	x	x	1	0	0	1		DCA Adjustment = -1
x	x	x	x	1	0	1	0		DCA Adjustment = -2
x	x	x	x	1	0	1	1		DCA Adjustment = -3
x	x	x	x	...					...
x	x	x	x	1	1	1	1		DCA Adjustment = -7
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x	Reserved	Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x	Reserved	Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x	Reserved	Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

NOTE 1 PG[C]RW[F5:F2, FD:FA] will be sticky, cleared by power cycle not reset.

## 11.21 Paged Control Words for Rx CTLE

### 11.21.1 PG[D]RWE0 Rx CTLE for DQ Control Words

Table 194 — PG[D]RWE0 Rx CTLE for DQ Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Rx CTLE Enable	(Default) CTLE feature Disabled
x	x	x	x	x	x	x	1		CTLE feature Enabled
x	x	x	x	x	x	0	x	Rx CTLE for DQ and DQS1 as CRC Broadcast Enable	(Default) Broadcast Disabled <sup>2</sup>
x	x	x	x	x	x	1	x		Broadcast Enabled <sup>3</sup>
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
0	0	0	x	x	x	x	x	CTLE Configuration Range Status <sup>4</sup> (Read Only Register)	Range A
0	0	1	x	x	x	x	x		Range B
0	1	0	x	x	x	x	x		Range C
0	1	1	x	x	x	x	x		Range D
1	0	0	x	x	x	x	x		Reserved
1	0	1	x	x	x	x	x		Reserved
1	1	0	x	x	x	x	x		Reserved
1	1	1	x	x	x	x	x		Reserved

NOTE 1 PG[D]RWE0[1:0] will be sticky, cleared by power cycle not reset.

NOTE 2 Rx CTLE for DQ and DQS1 as CRC Broadcast feature is disabled. In this case, the nine Rx CTLE setting control words, PG[D]RW[F8:F0], for all the DQ and DQS1 as CRC bits are configured separately by the corresponding Control Word Write to each control word address.

NOTE 3 Rx CTLE for DQ and DQS1 as CRC Broadcast feature is enabled. In this case, the nine Rx CTLE setting control words, PG[D]RW[F8:F0], for all the DQ and DQS1 as CRC bits are configured together by the Control Word Write to PG[D]RWF0. The Control Word Write to PG[D]RW[F8:F1] has no effect to the control word values.

NOTE 4 The device can only support one of the CTLE Configuration Ranges, A, B, C or D. The Host can read out the supported range from PG[D]RWE0[7:5].

## 11.21.2 PG[D]RWE1 - Per-Pin CTLE Disable Control Word

Table 195 — PG[D]RWE1 - Per-Pin CTLE Disable Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ0 CTLE Feature Disable	(Default) CTLE enabled in this pin <sup>2</sup>
x	x	x	x	x	x	x	1		CTLE disabled in this pin
x	x	x	x	x	x	0	x	DQ1 CTLE Feature Disable	(Default) CTLE enabled in this pin <sup>2</sup>
x	x	x	x	x	x	1	x		CTLE disabled in this pin
x	x	x	x	x	0	x	x	DQ2 CTLE Feature Disable	(Default) CTLE enabled in this pin <sup>2</sup>
x	x	x	x	x	1	x	x		CTLE disabled in this pin
x	x	x	x	0	x	x	x	DQ3 CTLE Feature Disable	(Default) CTLE enabled in this pin <sup>2</sup>
x	x	x	x	1	x	x	x		CTLE disabled in this pin
x	x	x	0	x	x	x	x	DQ4 CTLE Feature Disable	(Default) CTLE enabled in this pin <sup>2</sup>
x	x	x	1	x	x	x	x		CTLE disabled in this pin
x	x	0	x	x	x	x	x	DQ5 CTLE Feature Disable	(Default) CTLE enabled in this pin <sup>2</sup>
x	x	1	x	x	x	x	x		CTLE disabled in this pin
x	0	x	x	x	x	x	x	DQ6 CTLE Feature Disable	(Default) CTLE enabled in this pin <sup>2</sup>
x	1	x	x	x	x	x	x		CTLE disabled in this pin
0	x	x	x	x	x	x	x	DQ7 CTLE Feature Disable	(Default) CTLE enabled in this pin <sup>2</sup>
1	x	x	x	x	x	x	x		CTLE disabled in this pin

NOTE 1 PG[D]RWE1 will be sticky, cleared by power cycle not reset.

NOTE 2 CTLE will be enabled in the corresponding input pin provided that PG[D]RWE0[0] is set to 1.

### 11.21.3 PG[D]RWE2 - CTLE Disable Control for DQS1 as CRC Lane Control Word

**Table 196 — PG[D]RWE2 - CTLE Disable Control for DQS1 as CRC Lane Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQS1 as CRC lane CTLE Feature Disable	(Default) CTLE enabled in this pin <sup>2</sup>
x	x	x	x	x	x	x	1		CTLE disabled in this pin
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 PG[D]RWE2[0] will be sticky, cleared by power cycle not reset.

NOTE 2 CTLE will be enabled in the corresponding input pin provided that PG[D]RWE0[0] is set to 1.

### 11.21.4 PG[D]RW[F7:F0] Rx CTLE Settings for DQ[7:0] Control Words

**Table 197 — PG[D]RW[F7:F0] Rx CTLE Settings for DQ[7:0] Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Rx CTLE Configuration setting	Setting 0
x	x	x	x	0	0	0	1		Setting 1
x	x	x	x	0	0	1	0		Setting 2
x	x	x	x	0	0	1	1		Setting 3
x	x	x	x	0	1	0	0		Setting 4
x	x	x	x	0	1	0	1		Setting 5
x	x	x	x	0	1	1	0		Setting 6
x	x	x	x	0	1	1	1		Setting 7
x	x	x	x	1	0	0	0		Setting 8
x	x	x	x	1	0	0	1		Setting 9
x	x	x	x	1	0	1	0		Setting 10
x	x	x	x	1	0	1	1		Setting 11
x	x	x	x	1	1	0	0		Setting 12
x	x	x	x	1	1	0	1		Setting 13
x	x	x	x	1	1	1	0		Setting 14
x	x	x	x	1	1	1	1		Setting 15
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 PG[D]RW[F7:F0] will be sticky, cleared by power cycle not reset.

### 11.21.5 PG[D]RWF8 Rx CTLE Settings for DQS1 as CRC Lane Control Words

Table 198 — PG[D]RWF8 Rx CTLE Settings for DQS1 as CRC Lane Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Rx CTLE Configuration setting	Setting 0
x	x	x	x	0	0	0	1		Setting 1
x	x	x	x	0	0	1	0		Setting 2
x	x	x	x	0	0	1	1		Setting 3
x	x	x	x	0	1	0	0		Setting 4
x	x	x	x	0	1	0	1		Setting 5
x	x	x	x	0	1	1	0		Setting 6
x	x	x	x	0	1	1	1		Setting 7
x	x	x	x	1	0	0	0		Setting 8
x	x	x	x	1	0	0	1		Setting 9
x	x	x	x	1	0	1	0		Setting 10
x	x	x	x	1	0	1	1		Setting 11
x	x	x	x	1	1	0	0		Setting 12
x	x	x	x	1	1	0	1		Setting 13
x	x	x	x	1	1	1	0		Setting 14
x	x	x	x	1	1	1	1		Setting 15
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 PG[D]RWF8 will be sticky, cleared by power cycle not reset.

## 11.22 Device Equalization Self-Train Mode (DESTM) Control Words

### 11.22.1 PG[F]RWE0 - (DESTM) Control Word

Table 199 — PG[F]RWE0: (DESTM) Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Device Equalization Self-Train Mode Enable <sup>1</sup>	(Default) Disabled
x	x	x	x	x	x	x	1		Enabled
x	x	x	x	x	x	0	x	Training Start <sup>2</sup>	(Default) Stop Training
x	x	x	x	x	x	1	x		Start Training
x	x	x	x	x	0	x	x	Continuous Mode <sup>3</sup>	(Default) Disabled
x	x	x	x	x	1	x	x		Enabled <sup>4</sup>
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	0	0	0	x	x	x	x	Training pattern length select <sup>5</sup>	LFSR8 (Default)
x	0	0	1	x	x	x	x		LFSR16
x	0	1	0	x	x	x	x		Reserved for future use
x	0	1	1	x	x	x	x		Reserved for future use
x	1	0	0	x	x	x	x		Reserved for future use
x	1	0	1	x	x	x	x		Reserved for future use
x	1	1	0	x	x	x	x		Reserved for future use
x	1	1	1	x	x	x	x		Reserved for future use
0	x	x	x	x	x	x	x	LBTXDQ low assertion enabled <sup>6</sup>	(Default) Low assertion disabled
1	x	x	x	x	x	x	x		Low assertion enabled

NOTE 1 If this bit is set to the default “0”, then MDB will not start the DESTM even if the PG[F]RWE0[1] is set to “1”.

NOTE 2 Before the Host configures this bit to “1”, the LFSR patterns on the selected bits should already be running. When the Host configures this bit to “1”, the device will start the Self-Train on the selected DQ and DQS1 as CRC bits. When the training is finished, the device will clear this bit back to the default “0”. If the Host writes a “0” to this bit, the training will be stopped no matter if it is finished or not, and LBTXDQ will be driven back to HIGH.

NOTE 3 When this bit is configured to “0”, the continuous mode is disabled, and the device will self stop the internal training state machine when it is done. When this bit is configured to “1”, the continuous training mode is enabled, and the device will repeatedly run the internal training state machine until the Host configures PG[F]RWE0[1] = “0” to stop the training. When the continuous training mode is enabled, the LBTXDQ will not be asserted during the training procedure.

NOTE 4 Low assertion feature must be disabled PG[F]RWE0[7] = “0” prior to entering Continuous mode.

NOTE 5 If multiple DQ bits are selected for Self-Train, the LFSR patterns for these bits should be independent of one another. The LFSR seeds of these bit lanes should be staggered, with multiple steps away from each other. With dependent patterns for different bits, the crosstalk among these bits may be treated as ISI, therefore, the training results of DFE taps may be incorrect and suboptimal. For the unselected lanes, the Host should drive static HIGH.

NOTE 6 If PG[F]RWE0[7] is configured to “1”, LBTXDQ will be asserted during the Self-Train procedure, and will be de-asserted when the training procedure is finished. This is for the device to signal the MRCD the training status.

### 11.22.2 PG[F]RWE2 - DESTM CTLE Select Control Word

Table 200 — PG[F]RWE2: DESTM CTLE Select Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	CTLE select control	(Default) Selected to be trained during DESTM
x	x	x	x	x	x	x	1		Not selected to be trained during DESTM
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x	Reserved	Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x	Reserved	Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x	Reserved	Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x	Reserved	Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x	Reserved	Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

### 11.22.3 PG[F]RWE3 - DESTM DQS1 as CRC Select Control Word

Table 201 — PG[F]RWE3: DESTM DQS1 as CRC Select Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQS1 select	(Default) Not selected to be trained
x	x	x	x	x	x	x	1		Selected to be trained, when DQS1 is CRC
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x	Reserved	Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x	Reserved	Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x	Reserved	Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x	Reserved	Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x	Reserved	Reserved
0	x	x	x	x	x	x	x	DQS1 Fail Status Bit (Read Only) <sup>1,2</sup>	Executed normally
1	x	x	x	x	x	x	x		Failure occurred

NOTE 1 DESTM did not execute correctly. This register bit gets updated when DESTM training stops PG[F]RWE0[1] = 0, either by Host or MDB self-clear.

NOTE 2 The Fail Status bits self-clear on DESTM start.

### 11.22.4 PG[F]RWE4 - DESTM DQ Select Control Word

Table 202 — PG[F]RWE4: DESTM DQ Select Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ0 select	(Default) Not selected to be trained
x	x	x	x	x	x	x	1		Selected to be trained
x	x	x	x	x	x	0	x	DQ1 select	(Default) Not selected to be trained
x	x	x	x	x	x	1	x		Selected to be trained
x	x	x	x	x	0	x	x	DQ2 select	(Default) Not selected to be trained
x	x	x	x	x	1	x	x		Selected to be trained
x	x	x	x	0	x	x	x	DQ3select	(Default) Not selected to be trained
x	x	x	x	1	x	x	x		Selected to be trained
x	x	x	0	x	x	x	x	DQ4 select	(Default) Not selected to be trained
x	x	x	1	x	x	x	x		Selected to be trained
x	x	0	x	x	x	x	x	DQ5 select	(Default) Not selected to be trained
x	x	1	x	x	x	x	x		Selected to be trained
x	0	x	x	x	x	x	x	DQ6 select	(Default) Not selected to be trained
x	1	x	x	x	x	x	x		Selected to be trained
0	x	x	x	x	x	x	x	DQ7 select	(Default) Not selected to be trained
1	x	x	x	x	x	x	x		Selected to be trained

### 11.22.5 PG[F]RWE5 - DESTM DQ Status Control Word

Table 203 — PG[F]RWE5: DESTM DQ Status Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ0 Fail Status Bit (Read Only) <sup>1,2</sup>	Executed normally
x	x	x	x	x	x	x	1		Failure occurred
x	x	x	x	x	x	0	x	DQ1 Fail Status Bit (Read Only) <sup>2,3</sup>	Executed normally
x	x	x	x	x	x	1	x		Failure occurred
x	x	x	x	x	0	x	x	DQ2 Fail Status Bit (Read Only) <sup>2,3</sup>	Executed normally
x	x	x	x	x	1	x	x		Failure occurred
x	x	x	x	0	x	x	x	DQ3 Fail Status Bit (Read Only) <sup>2,3</sup>	Executed normally
x	x	x	x	1	x	x	x		Failure occurred
x	x	x	0	x	x	x	x	DQ4 Fail Status Bit (Read Only) <sup>2,3</sup>	Executed normally
x	x	x	1	x	x	x	x		Failure occurred
x	x	0	x	x	x	x	x	DQ6 Fail Status Bit (Read Only) <sup>2,3</sup>	Executed normally
x	x	1	x	x	x	x	x		Failure occurred
x	0	x	x	x	x	x	x	DQ6 Fail Status Bit (Read Only) <sup>2,3</sup>	Executed normally
x	1	x	x	x	x	x	x		Failure occurred
0	x	x	x	x	x	x	x	DQ7 Fail Status Bit (Read Only) <sup>2,3</sup>	Executed normally
1	x	x	x	x	x	x	x		Failure occurred

NOTE 1 DESTM did not execute correctly. This register bit gets updated when DESTM training stops, either by Host or MDB self-clear

NOTE 2 The Fail Status bits self-clear on DESTM start.



### 11.22.6 PG[F]RWFD - CRC Lane DFE Tap Enable Select Control Word

Table 204 — PG[F]RWFD: CRC Lane DFE Tap Enable Select Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Tap 1 Enable Bit for CRC lane	(Default) Tap 1 disabled
x	x	x	x	x	x	x	1		Tap 1 enabled
x	x	x	x	x	x	0	x	Tap 2 Enable Bit for CRC lane	(Default) Tap 2 disabled
x	x	x	x	x	x	1	x		Tap 2 enabled
x	x	x	x	x	0	x	x	Tap 3 Enable Bit for CRC lane	(Default) Tap 3 disabled
x	x	x	x	x	1	x	x		Tap 3 enabled
x	x	x	x	0	x	x	x	Tap 4 Enable Bit for CRC lane	(Default) Tap 4 disabled
x	x	x	x	1	x	x	x		Tap 4 enabled
x	x	x	0	x	x	x	x	Tap 5 Enable Bit for CRC lane	(Default) Tap 5 disabled
x	x	x	1	x	x	x	x		Tap 5 enabled
x	x	0	x	x	x	x	x	Tap 6 Enable Bit for CRC lane	(Default) Tap 6 disabled
x	x	1	x	x	x	x	x		Tap 6 enabled
x	0	x	x	x	x	x	x	Tap 7 Enable Bit for CRC lane	(Default) Tap 7 disabled
x	1	x	x	x	x	x	x		Tap 7 enabled
0	x	x	x	x	x	x	x	Tap 8 Enable Bit for CRC lane	(Default) Tap 8 disabled
1	x	x	x	x	x	x	x		Tap 8 enabled

## 11.23 Page 10 - Enhanced Training Registers

### 11.23.1 PG[10]RW[E3:E0] - Host Interface Error Counter Status Control Words

**Table 205 — PG[10]RW[E3:E0] - Host Interface Error Counter Status Control Words<sup>1,2,3,4</sup>**

RW	Description	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PG[10]RWE0	Host Interface Error Counter Bits 0-7 (Read Only Control word)	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
PG[10]RWE1	Host Interface Error Counter Bits 8-15 (Read Only Control word)	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8
PG[10]RWE2	Host Interface Error Counter Bits 16 -23 (Read Only Control word)	EC23	EC22	EC21	EC20	EC19	EC18	EC17	EC16
PG[10]RWE3	Host Interface Error Counter Bits 24 31 (Read Only Control word)	EC31	EC30	EC29	EC28	EC27	EC26	EC25	EC24

NOTE 1 Reports the total UI errors across all DQ and CRC lanes.

NOTE 2 The error counters are Enabled only in write direction.

NOTE 3 The counters maintain their state independent of EWTM entry/exit.

NOTE 4 This register is Read Only and is cleared by PG[10]RWF0[0]

### 11.23.2 PG[10]RWEA - CRC (DQS1) Training UI Phase Error Status Control Word

**Table 206 — PG[10]RWEA - CRC (DQS1) Training UI Phase Error Status Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0		
x	x	x	x	x	x	x	0	DQS1 Error - UI0 or UI4 or UI8 or UI12 or UI16, UI20 or UI24 or UI28	No errors occurred
x	x	x	x	x	x	x	1		Errors occurred
x	x	x	x	x	x	0	x	DQS1 Error - UI1 or UI5 or UI9 or UI13 or UI17, UI21 or UI25 or UI29	No errors occurred
x	x	x	x	x	x	1	x		Errors occurred
x	x	x	x	x	0	x	x	DQS1 Error - UI2 or UI6 or UI10 or UI14 or UI18, UI22 or UI26 or UI30	No errors occurred
x	x	x	x	x	1	x	x		Errors occurred
x	x	x	x	0	x	x	x	DQS1 Error - UI3 or UI7 or UI11 or UI15 or UI19, UI23 or UI27 or UI31	No errors occurred
x	x	x	x	1	x	x	x		Errors occurred
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x	Reserved	Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x	Reserved	Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x	Reserved	Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x	Reserved	Reserved

NOTE 1 This register is Read Only and is cleared by PG[10]RWF0[1]

### 11.23.3 PG[10]RWEB - DQ0 and DQ1 Training UI Phase Error Status Control Word

Table 207 — PG[10]RWEB - DQ0 and DQ1 Training UI Phase Error Status Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ0 Error UI0 or UI4 or UI8 or UI12 or UI16, UI20 or UI24 or UI28	No errors occurred
x	x	x	x	x	x	x	1		Errors occurred
x	x	x	x	x	x	0	x	DQ0 Error UI1 or UI5 or UI9 or UI13 or UI17, UI21 or UI25 or UI29	No errors occurred
x	x	x	x	x	x	1	x		Errors occurred
x	x	x	x	x	0	x	x	DQ0 Error UI2 or UI6 or UI10 or UI14 or UI18, UI22 or UI26 or UI30	No errors occurred
x	x	x	x	x	1	x	x		Errors occurred
x	x	x	x	0	x	x	x	DQ0 Error UI3 or UI7 or UI11 or UI15 or UI19, UI23 or UI27 or UI31	No errors occurred
x	x	x	x	1	x	x	x		Errors occurred
x	x	x	0	x	x	x	x	DQ1 Error UI0 or UI4 or UI8 or UI12 or UI16, UI20 or UI24 or UI28	No errors occurred
x	x	x	1	x	x	x	x		Errors occurred
x	x	0	x	x	x	x	x	DQ1 Error UI1 or UI5 or UI9 or UI13 or UI17, UI21 or UI25 or UI29	No errors occurred
x	x	1	x	x	x	x	x		Errors occurred
x	0	x	x	x	x	x	x	DQ1 Error UI2 or UI6 or UI10 or UI14 or UI18, UI22 or UI26 or UI30	No errors occurred
x	1	x	x	x	x	x	x		Errors occurred
0	x	x	x	x	x	x	x	DQ1 Error UI3 or UI7 or UI11 or UI15 or UI19, UI23 or UI27 or UI31	No errors occurred
1	x	x	x	x	x	x	x		Errors occurred

NOTE 1 This register is Read Only and is cleared by [PG\[10\]RWF0\[1\]](#)

### 11.23.4 PG[10]RVEC - DQ2 and DQ3 Training UI Phase Error Status Control Word

Table 208 — PG[10]RVEC - DQ2 and DQ3 Training UI Phase Error Status Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ2 Error - UI0 or UI4 or UI8 or UI12 or UI16, UI20 or UI24 or UI28	No errors occurred
x	x	x	x	x	x	x	1		Errors occurred
x	x	x	x	x	x	0	x	DQ2 Error - UI1 or UI5 or UI9 or UI13 or UI17, UI21 or UI25 or UI29	No errors occurred
x	x	x	x	x	x	1	x		Errors occurred
x	x	x	x	x	0	x	x	DQ2 Error - UI2 or UI6 or UI10 or UI14 or UI18, UI22 or UI26 or UI30	No errors occurred
x	x	x	x	x	1	x	x		Errors occurred
x	x	x	x	0	x	x	x	DQ2 Error - UI3 or UI7 or UI11 or UI15 or UI19, UI23 or UI27 or UI31	No errors occurred
x	x	x	x	1	x	x	x		Errors occurred
x	x	x	0	x	x	x	x	DQ3 Error - UI0 or UI4 or UI8 or UI12 or UI16, UI20 or UI24 or UI28	No errors occurred
x	x	x	1	x	x	x	x		Errors occurred
x	x	0	x	x	x	x	x	DQ3 Error - UI1 or UI5 or UI9 or UI13 or UI17, UI21 or UI25 or UI29	No errors occurred
x	x	1	x	x	x	x	x		Errors occurred
x	0	x	x	x	x	x	x	DQ3 Error - UI2 or UI6 or UI10 or UI14 or UI18, UI22 or UI26 or UI30	No errors occurred
x	1	x	x	x	x	x	x		Errors occurred
0	x	x	x	x	x	x	x	DQ3 Error - UI3 or UI7 or UI11 or UI15 or UI19, UI23 or UI27 or UI31	No errors occurred
1	x	x	x	x	x	x	x		Errors occurred

NOTE 1 This register is Read Only and is cleared by [PG\[10\]RWF0\[1\]](#)

### 11.23.5 PG[10]RWED - DQ4 and DQ5 Training UI Phase Error Status Control Word

Table 209 — PG[10]RWED - DQ4 and DQ5 Training UI Phase Error Status Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ4 Error - UI0 or UI4 or UI8 or UI12 or UI16, UI20 or UI24 or UI28	No errors occurred
x	x	x	x	x	x	x	1		Errors occurred
x	x	x	x	x	x	0	x	DQ4 Error - UI1 or UI5 or UI9 or UI13 or UI17, UI21 or UI25 or UI29	No errors occurred
x	x	x	x	x	x	1	x		Errors occurred
x	x	x	x	x	0	x	x	DQ4 Error - UI2 or UI6 or UI10 or UI14 or UI18, UI22 or UI26 or UI30	No errors occurred
x	x	x	x	x	1	x	x		Errors occurred
x	x	x	x	0	x	x	x	DQ4 Error - UI3 or UI7 or UI11 or UI15 or UI19, UI23 or UI27 or UI31	No errors occurred
x	x	x	x	1	x	x	x		Errors occurred
x	x	x	0	x	x	x	x	DQ5 Error - UI0 or UI4 or UI8 or UI12 or UI16, UI20 or UI24 or UI28	No errors occurred
x	x	x	1	x	x	x	x		Errors occurred
x	x	0	x	x	x	x	x	DQ5 Error - UI1 or UI5 or UI9 or UI13 or UI17, UI21 or UI25 or UI29	No errors occurred
x	x	1	x	x	x	x	x		Errors occurred
x	0	x	x	x	x	x	x	DQ5 Error - UI2 or UI6 or UI10 or UI14 or UI18, UI22 or UI26 or UI30	No errors occurred
x	1	x	x	x	x	x	x		Errors occurred
0	x	x	x	x	x	x	x	DQ5 Error - UI3 or UI7 or UI11 or UI15 or UI19, UI23 or UI27 or UI31	No errors occurred
1	x	x	x	x	x	x	x		Errors occurred

NOTE 1 This register is Read Only and is cleared by [PG\[10\]RWF0\[1\]](#)

### 11.23.6 PG[10]RWEE - DQ6 and DQ7 Training UI Phase Error Status Control Word

Table 210 — PG[10]RWEE - DQ6 and DQ7 Training UI Phase Error Status Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ6 Error - UI0 or UI4 or UI8 or UI12 or UI16, UI20 or UI24 or UI28	No errors occurred
x	x	x	x	x	x	x	1		Errors occurred
x	x	x	x	x	x	0	x	DQ6 Error - UI1 or UI5 or UI9 or UI13 or UI17, UI21 or UI25 or UI29	No errors occurred
x	x	x	x	x	x	1	x		Errors occurred
x	x	x	x	x	0	x	x	DQ6 Error - UI2 or UI6 or UI10 or UI14 or UI18, UI22 or UI26 or UI30	No errors occurred
x	x	x	x	x	1	x	x		Errors occurred
x	x	x	x	0	x	x	x	DQ6 Error - UI3 or UI7 or UI11 or UI15 or UI19, UI23 or UI27 or UI31	No errors occurred
x	x	x	x	1	x	x	x		Errors occurred
x	x	x	0	x	x	x	x	DQ7 Error - UI0 or UI4 or UI8 or UI12 or UI16, UI20 or UI24 or UI28	No errors occurred
x	x	x	1	x	x	x	x		Errors occurred
x	x	0	x	x	x	x	x	DQ7 Error - UI1 or UI5 or UI9 or UI13 or UI17, UI21 or UI25 or UI29	No errors occurred
x	x	1	x	x	x	x	x		Errors occurred
x	0	x	x	x	x	x	x	DQ7 Error - UI2 or UI6 or UI10 or UI14 or UI18, UI22 or UI26 or UI30	No errors occurred
x	1	x	x	x	x	x	x		Errors occurred
0	x	x	x	x	x	x	x	DQ7 Error - UI3 or UI7 or UI11 or UI15 or UI19, UI23 or UI27 or UI31	No errors occurred
1	x	x	x	x	x	x	x		Errors occurred

NOTE 1 This register is Read Only and is cleared by [PG\[10\]RWF0\[1\]](#)

### 11.23.7 PG[10]RWF0 - Error Counter and UI Status Clear Control Word

Table 211 — PG[10]RWF0 - Error Counter and UI Status Clear Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Clear Error Counters <sup>1</sup>	No Action
x	x	x	x	x	x	x	1		Clears Error Counter registers PG[10]RW[E3:E0] to default settings
x	x	x	x	x	x	0	x	Clear UI Error Status Registers <sup>1</sup>	No Action
x	x	x	x	x	x	1	x		Clears UI Error Counter Status registers PG[10]RW[EE:EA] to default settings.
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 This bit is Self clearing.

### 11.23.8 PG[10]RWF1- LFSR Pattern Control Word

Table 212 — PG[10]RWF1 - LFSR Pattern Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	PS0 and PS1 16 bit LFSR Pattern Control	Disabled - (Legacy 8 bit pattern generator in PG8) <sup>1</sup>
x	x	x	x	x	x	0	1		16 bit LFSR
x	x	x	x	x	x	1	0		16 bit Static Repeating <sup>2</sup>
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 HIW, ERTM and EWTM only support 16 bit.

NOTE 2 Static repeating, uses the LFSR seed register content as the pattern. For Serial Read Training Pattern Format mode, the following Mode Registers are programmed with the data pattern. There are two 8-bit registers to provide a 16 UI pattern length.

### 11.23.9 PG[10]RWF3 - Error Detect Threshold Control Word

Table 213 — PG[10]RWF3 - Error Detect Threshold Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Threshold for UI Status Registers	1 Error will modify UI status to be 1
x	x	x	0	0	0	0	1		2 Errors will modify UI status to be 1
x	x	x	0	0	0	1	0		3 Errors will modify UI status to be 1
x	x	x	0	0	0	1	1		4 Errors will modify UI status to be 1
x	x	x	0	0	1	0	0		5 Errors will modify UI status to be 1
x	x	x	0	0	1	0	1		6 Errors will modify UI status to be 1
x	x	x	0	0	1	1	0		7 Errors will modify UI status to be 1
x	x	x	....						....
x	x	x	....						....
x	x	x	....						....
x	x	x	1	1	1	0	0		29 Errors will modify UI status to be 1
x	x	x	1	1	1	0	1		30 Errors will modify UI status to be 1
x	x	x	1	1	1	1	0		31 Errors will modify UI status to be 1
x	x	x	1	1	1	1	1		32 Errors will modify UI status to be 1
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 Sets threshold for UI Phase Error Status in PG[10]RW[EE:EA].

### 11.23.10 PG[10]RWF4 - Error Mask DQ Lanes Control Word

Table 214 — PG[10]RWF4 - Error Mask DQ Lanes Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ0 Mask Enable	Disabled
x	x	x	x	x	x	x	1		Enabled
x	x	x	x	x	x	0	x	DQ1 Mask Enable	Disabled
x	x	x	x	x	x	1	x		Enabled
x	x	x	x	x	0	x	x	DQ2 Mask Enable	Disabled
x	x	x	x	x	1	x	x		Enabled
x	x	x	x	0	x	x	x	DQ3 Mask Enable	Disabled
x	x	x	x	1	x	x	x		Enabled
x	x	x	0	x	x	x	x	DQ4 Mask Enable	Disabled
x	x	x	1	x	x	x	x		Enabled
x	x	0	x	x	x	x	x	DQ5 Mask Enable	Disabled
x	x	1	x	x	x	x	x		Enabled
x	0	x	x	x	x	x	x	DQ6 Mask Enable	Disabled
x	1	x	x	x	x	x	x		Enabled
0	x	x	x	x	x	x	x	DQ7 Mask Enable	Disabled
1	x	x	x	x	x	x	x		Enabled

NOTE 1 Mask applies to Error Counter Registers PG[10]RW[E3:E0].

### 11.23.11 PG[10]RWF5 - Error Mask CRC Lanes Control Word

Table 215 — PG[10]RWF5 - Error Mask CRC Lanes Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQS1 Mask Enable <sup>1</sup>	Disabled
x	x	x	x	x	x	x	1		Enabled
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 Mask applies to Error Counter Registers PG[10]RW[E3:E0]

### 11.23.12 PG[10]RWF8 - PS0 16-bit UI Mask Lower Control Word

Table 216 — PG[10]RWF8 - PS0 16-bit UI Mask Lower Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	UI 0 Mask Enable	Disabled
x	x	x	x	x	x	x	1		Enabled
x	x	x	x	x	x	0	x	UI 1 Mask Enable	Disabled
x	x	x	x	x	x	1	x		Enabled
x	x	x	x	x	0	x	x	UI 2 Mask Enable	Disabled
x	x	x	x	x	1	x	x		Enabled
x	x	x	x	0	x	x	x	UI 3 Mask Enable	Disabled
x	x	x	x	1	x	x	x		Enabled
x	x	x	0	x	x	x	x	UI 4 Mask Enable	Disabled
x	x	x	1	x	x	x	x		Enabled
x	x	0	x	x	x	x	x	UI 5 Mask Enable	Disabled
x	x	1	x	x	x	x	x		Enabled
x	0	x	x	x	x	x	x	UI 6 Mask Enable	Disabled
x	1	x	x	x	x	x	x		Enabled
0	x	x	x	x	x	x	x	UI 7 Mask Enable	Disabled
1	x	x	x	x	x	x	x		Enabled

NOTE 1 UI Masks apply to UI phase registers PG[10]RW[EE:EA] and Error Counter Registers PG[10]RW[E3:E0].

## 11.23.13 PG[10]RWF9 - PS0 16-bit UI Mask Upper Control Word

Table 217 — PG[10]RWF9 - PS0 16-bit UI Mask Upper Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	UI 8 Mask Enable	Disabled
x	x	x	x	x	x	x	1		Enabled
x	x	x	x	x	x	0	x	UI 9 Mask Enable	Disabled
x	x	x	x	x	x	1	x		Enabled
x	x	x	x	x	0	x	x	UI 10 Mask Enable	Disabled
x	x	x	x	x	1	x	x		Enabled
x	x	x	x	0	x	x	x	UI 11 Mask Enable	Disabled
x	x	x	x	1	x	x	x		Enabled
x	x	x	0	x	x	x	x	UI 12 Mask Enable	Disabled
x	x	x	1	x	x	x	x		Enabled
x	x	0	x	x	x	x	x	UI 13 Mask Enable	Disabled
x	x	1	x	x	x	x	x		Enabled
x	0	x	x	x	x	x	x	UI 14 Mask Enable	Disabled
x	1	x	x	x	x	x	x		Enabled
0	x	x	x	x	x	x	x	UI 15 Mask Enable	Disabled
1	x	x	x	x	x	x	x		Enabled

NOTE 1 UI Masks apply to UI phase registers [PG\[10\]RW\[EE:EA\]](#) and Error Counter Registers [PG\[10\]RW\[E3:E0\]](#).

## 11.23.14 PG[10]RWFA- PS1 16-bit UI Mask Lower Control Word

Table 218 — PG[10]RWFA - PS1 16-bit UI Mask Lower Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	UI 0 Mask Enable	Disabled
x	x	x	x	x	x	x	1		Enabled
x	x	x	x	x	x	0	x	UI 1 Mask Enable	Disabled
x	x	x	x	x	x	1	x		Enabled
x	x	x	x	x	0	x	x	UI 2 Mask Enable	Disabled
x	x	x	x	x	1	x	x		Enabled
x	x	x	x	0	x	x	x	UI 3 Mask Enable	Disabled
x	x	x	x	1	x	x	x		Enabled
x	x	x	0	x	x	x	x	UI 4 Mask Enable	Disabled
x	x	x	1	x	x	x	x		Enabled
x	x	0	x	x	x	x	x	UI 5 Mask Enable	Disabled
x	x	1	x	x	x	x	x		Enabled
x	0	x	x	x	x	x	x	UI 6 Mask Enable	Disabled
x	1	x	x	x	x	x	x		Enabled
0	x	x	x	x	x	x	x	UI 7 Mask Enable	Disabled
1	x	x	x	x	x	x	x		Enabled

NOTE 1 UI Masks apply to UI phase registers [PG\[10\]RW\[EE:EA\]](#) and Error Counter Registers [PG\[10\]RW\[E3:E0\]](#).



### 11.23.15 PG[10]RWFB- PS1 16-bit UI Mask Upper Control Word

Table 219 — PG[10]RWFB - PS1 16-bit UI Mask Upper Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	UI 8 Mask Enable	Disabled
x	x	x	x	x	x	x	1		Enabled
x	x	x	x	x	x	0	x	UI 9 Mask Enable	Disabled
x	x	x	x	x	x	1	x		Enabled
x	x	x	x	x	0	x	x	UI 10 Mask Enable	Disabled
x	x	x	x	x	1	x	x		Enabled
x	x	x	x	0	x	x	x	UI 11 Mask Enable	Disabled
x	x	x	x	1	x	x	x		Enabled
x	x	x	0	x	x	x	x	UI 12 Mask Enable	Disabled
x	x	x	1	x	x	x	x		Enabled
x	x	0	x	x	x	x	x	UI 13 Mask Enable	Disabled
x	x	1	x	x	x	x	x		Enabled
x	0	x	x	x	x	x	x	UI 14 Mask Enable	Disabled
x	1	x	x	x	x	x	x		Enabled
0	x	x	x	x	x	x	x	UI 15 Mask Enable	Disabled
1	x	x	x	x	x	x	x		Enabled

NOTE 1 UI Masks apply to UI phase registers [PG\[10\]RW\[EE:EA\]](#) and Error Counter Registers [PG\[10\]RW\[E3:E0\]](#).

## 11.24 Page 11 - Host Interface PS0 16-bit LFSR Seed Registers

### 11.24.1 PG[11]RW[E0, E2, E4, E6, E8, EA, EC, EE, F0]: Host Interface PS0 16-bit LFSR Seed Lower Byte Control Word

**Table 220 — PG[11]RW[E0, E2, E4, E6, E8, EA, EC, EE, F0]: Host Interface PS0 16-bit LFSR Seed Lower Byte Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	PS0 16 bit LFSR Seed Lower Byte <sup>2</sup>	LFSR Seed - xx00h
0	0	0	0	0	0	0	1		LFSR Seed - xx01h
>>>>>>									
1	1	1	1	1	1	1	0		LFSR Seed - xxFEh
1	1	1	1	1	1	1	1		LFSR Seed - xxFFh

NOTE 1 This register is used for DQS1 and DQx signals used for LFSR or Static Repeating pattern.

NOTE 2 The 16 bit LFSR equation shown in Figure 87 is used for both Host Interface EWTM, ERTM and DQ DFE training.

### 11.24.2 PG[11]RW[E1, E3, E5, E7, E9, EB, ED, EF, F1]: Host Interface PS0 16-bit LFSR Seed Upper Byte Control Word

**Table 221 — PG[11]RW[E1, E3, E5, E7, E9, EB, ED, EF, F1]: Host Interface PS0 16 bit LFSR Seed Upper Byte Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	PS0 16 bit LFSR Seed Upper Byte <sup>2</sup>	LFSR Seed - 00xxh
0	0	0	0	0	0	0	1		LFSR Seed - 01xxh
>>>>>>									
1	1	1	1	1	1	1	0		LFSR Seed - FExxh
1	1	1	1	1	1	1	1		LFSR Seed - FFxxh

NOTE 1 This register is used for DQS1 and DQx signals used for LFSR or Static Repeating pattern.

NOTE 2 The 16 bit LFSR equation shown in Figure 87 is used for both Host Interface EWTM, ERTM and DQ DFE training.

## 11.25 Page 12 - Host Interface PS0 16 bit LFSR State

### 11.25.1 PG[12]RW[E0, E2, E4, E6, E8, EA, EC, EE, F0]: Host Interface PS0 16-bit LFSR State Training Mode Lower Byte Control Word

Table 222 — PG[12]RW[E0, E2, E4, E6, E8, EA, EC, EE, F0]: Host Interface PS0 16-bit LFSR State Training Mode Lower Byte Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	PS0 16 bit LFSR State Lower Byte (Read Only) <sup>1</sup>	LFSR State = 0x00*
0	0	0	0	0	0	0	1		LFSR State = 0x01
0	0	0	0	0	0	1	0		LFSR State = 0x02
...									...
1	1	1	1	1	1	0	0		LFSR State = 0xFC
1	1	1	1	1	1	0	1		LFSR State = 0xFD
1	1	1	1	1	1	1	0		LFSR State= 0xFE
1	1	1	1	1	1	1	1		LFSR State = 0xFF

NOTE 1 The LFSR State is the internal state of the Galois LFSR. This read only register is used for debug, and tracks the state of the LFSR Lower byte associated with the selected DQ or DQS signal for training.

### 11.25.2 PG[12]RW[E1, E3, E5, E7, E9, EB, ED, EF, F1]: Host Interface PS0 16-bit LFSR State Training Mode Upper Byte Control Word

Table 223 — PG[12]RW[E1, E3, E5, E7, E9, EB, ED, EF, F1]: Host Interface PS0 16-bit LFSR State Training Mode Upper Byte Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	PS1 16 bit LFSR State Upper Byte (Read Only) <sup>1</sup>	LFSR State = 0x00*
0	0	0	0	0	0	0	1		LFSR State = 0x01
0	0	0	0	0	0	1	0		LFSR State = 0x02
...									...
1	1	1	1	1	1	0	0		LFSR State = 0xFC
1	1	1	1	1	1	0	1		LFSR State = 0xFD
1	1	1	1	1	1	1	0		LFSR State= 0xFE
1	1	1	1	1	1	1	1		LFSR State = 0xFF

NOTE 1 The LFSR State is the internal state of the Galois LFSR. This read only register is used for debug, and tracks the state of the LFSR Upper byte associated with the selected DQ or DQS signal for training.

## 11.26 Page 13 - Host Interface PS1 16-bit LFSR Seed

### 11.26.1 PG[13]RW[E0, E2, E4, E6, E8, EA, EC, EE, F0]: Host Interface PS1 16-bit LFSR Seed Lower Byte Control Word

**Table 224 — PG[13]RW[E0, E2, E4, E6, E8, EA, EC, EE, F0]: Host Interface PS1 16-bit LFSR Seed Lower Byte Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	PS1 16 bit LFSR Seed Lower Byte <sup>2</sup>	LFSR Seed - xx00h
0	0	0	0	0	0	0	1		LFSR Seed - xx01h
>>>>>>									
1	1	1	1	1	1	1	0		LFSR Seed - xxFEh
1	1	1	1	1	1	1	1		LFSR Seed - xEFxh

NOTE 1 This register is used for DQS1 and DQx signals used for LFSR or Static Repeating pattern.

NOTE 2 The 16 bit LFSR equation shown in Figure 87 is used for both Host Interface EWTM, ERTM and DQ DFE training.

### 11.26.2 PG[13]RW[E1, E3, E5, E7, E9, EB, ED, EF, F1]: Host Interface PS1 16-bit LFSR Seed Upper Byte Control Word

**Table 225 — PG[13]RW[E1, E3, E5, E7, E9, EB, ED, EF, F1]: Host Interface PS1 16-bit LFSR Seed Upper Byte Control Word<sup>1</sup>**

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	PS1 16 bit LFSR Seed Upper Byte <sup>2</sup>	LFSR Seed - 00xxh
0	0	0	0	0	0	0	1		LFSR Seed - 01xxh
>>>>>>									
1	1	1	1	1	1	1	0		LFSR Seed - FExxx
1	1	1	1	1	1	1	1		LFSR Seed - FFxxx

NOTE 1 This register is used for DQS1 and DQx signals used for LFSR or Static Repeating pattern.

NOTE 2 The 16 bit LFSR equation shown in Figure 87 is used for both Host Interface EWTM, ERTM and DQ DFE training.

## 11.27 Page 14 Host Interface PS1 16 bit LFSR State

### 11.27.1 PG[14]RW[E0, E2, E4, E6, E8, EA, EC, EE, F0]: Host Interface PS1 16-bit LFSR State Training Mode Lower Byte Control Word

Table 226 — PG[14]RW[E0, E2, E4, E6, E8, EA, EC, EE, F0]: Host Interface 16-bit PS1 LFSR State Training Mode Lower Byte Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	PS1 16 bit LFSR State Lower Byte (Read Only) <sup>1</sup>	LFSR State = 0x00*
0	0	0	0	0	0	0	1		LFSR State = 0x01
0	0	0	0	0	0	1	0		LFSR State = 0x02
...									...
1	1	1	1	1	1	0	0		LFSR State = 0xFC
1	1	1	1	1	1	0	1		LFSR State = 0xFD
1	1	1	1	1	1	1	0		LFSR State= 0xFE
1	1	1	1	1	1	1	1		LFSR State = 0xFF

NOTE 1 The LFSR State is the internal state of the Galois LFSR. This read only register is used for debug, and tracks the state of the LFSR Lower byte associated with the selected DQ or DQS signal for training.

### 11.27.2 PG[14]RW[E1, E3, E5, E7, E9, EB, ED, EF, F1]: Host Interface PS1 16-bit LFSR State Training Mode Upper Byte Control Word

Table 227 — PG[14]RW[E1, E3, E5, E7, E9, EB, ED, EF, F1]: Host Interface PS1 16-bit LFSR State Training Mode Upper Byte Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
0	0	0	0	0	0	0	0	PS1 16 bit LFSR State Upper Byte (Read Only) <sup>1</sup>	LFSR State = 0x00*
0	0	0	0	0	0	0	1		LFSR State = 0x01
0	0	0	0	0	0	1	0		LFSR State = 0x02
...									...
1	1	1	1	1	1	0	0		LFSR State = 0xFC
1	1	1	1	1	1	1	0		LFSR State = 0xFD
1	1	1	1	1	1	1	1		LFSR State= 0xFE
1	1	1	1	1	1	1	1		LFSR State = 0xFF

NOTE 1 The LFSR State is the internal state of the Galois LFSR. This read only register is used for debug, and tracks the state of the LFSR Upper byte associated with the selected DQ or DQS signal for training.

## 11.28 MDB Feature Control Words

### 11.28.1 PG[60]RWE0: MDB Rank Mode Global Features

Table 228 — PG[60]RWE0: MDB Rank Mode Global Features

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Rank Operating Mode <sup>1</sup>	(Default) Rank mode disabled
x	x	x	x	x	x	x	1		Rank mode enabled
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 This bit is sticky, cleared by Power-on Reset not BRST\_n. MRW write to this CW requires tSTAB\_DB wait time. When the Rank mode is enabled, it shall not switch.

### 11.28.2 PG[60]RWE4: MDB Rank Mode Training Control Word

Table 229 — PG[60]RWE4: MDB Rank Mode Training Control Word

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	MDQS and MDQ Selection for Transparent Mode and DQ Pass-Through Mode <sup>1,2</sup>	(Default) A_MDQS and A_MDQ are selected
x	x	x	x	x	x	x	1		B_MDQS and B_MDQ are selected
x	x	x	x	x	x	0	x	Reserved	Reserved
x	x	x	x	x	x	1	x		Reserved
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 This bit applies only when the read direction is selected in Rank mode.

NOTE 2 This bit also applies to select which rank group is being trained in MRE, MRD, DWL and MWD training modes. The result of the selected rank group will be passed to the DQ pins.

### 11.28.3 PG[70]RWE0: MDB Global Features

Table 230 — PG[70]RWE0: MDB Global Features

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	0	0	Mux operating mode <sup>1</sup>	Reserved
x	x	x	x	x	x	0	1		(default) Mux Mode enabled <sup>2</sup>
x	x	x	x	x	x	1	0		Reserved
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	x	0	x	x	Read CRC Enable <sup>1</sup>	Disabled
x	x	x	x	x	1	x	x		Enabled
x	x	x	x	0	x	x	x	Write CRC Enable <sup>1</sup>	Disabled
x	x	x	x	1	x	x	x		Enabled <sup>3</sup>
x	x	x	0	x	x	x	x	Write CRC Error Status	Write 0 to clear
x	x	x	1	x	x	x	x		MDB set to 1 to indicate CRC Error
x	x	0	x	x	x	x	x	CRC Pin Training Mode	(default) Disabled
x	x	1	x	x	x	x	x		Enabled
x	0	x	x	x	x	x	x	Loopback select DQS1 as CRC	(default) DQS1 is not selected.
x	1	x	x	x	x	x	x		DQS1 is selected <sup>4</sup>
0	x	x	x	x	x	x	x	Link CRC LBTXDQ RON <sub>pu</sub>	(default) Normal Operation per RW8E[5:3]
1	x	x	x	x	x	x	x		LBTXDQ pull-up disabled <sup>5</sup>

NOTE 1 The bits are sticky, cleared by Power-on Reset not BRST<sub>n</sub>.

NOTE 2 The Mux mode is enabled only when Rank mode is disabled with PG[60]RWE0[0]="0". When Rank mode is enabled with PG[60]RWE0[0] configured to "1", the Mux mode in PG[70]RWE0[1:0] will be overridden and disabled.

NOTE 3 Before enabling the Write CRC via PG[70]RWE0[3] = 1, it is the Host's responsibility to disable the RTT<sub>Loopback</sub> in RW8E.

NOTE 4 When DQS1 as CRC is selected, DQS1 will be sent for loopback regardless of the DQ select settings.

NOTE 5 This bit must be set when WR CRC is enabled in PG[70]RWE0[3].

### 11.28.4 PG[70]RWE1: DRAM Interface Receiver Type

Table 231 — PG[70]RWE1: DRAM Interface Receiver Type

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DRAM Interface Receiver Type (Read Only Register)	Unmatched <sup>1</sup>
x	x	x	x	x	x	x	1		Matched <sup>2</sup>

NOTE 1 The Default Read Delay in PG[00,01,72,73]RW[E5:E4] will be  $(1 + \frac{1}{4}) * tBCK$ .

NOTE 2 The Default Read Delay in PG[00,01,72,73]RW[E5:E4] will be  $(\frac{1}{4}) * tBCK$ .

## 11.28.5 PG[70]RWE2: Host Interface DQS Driver Control Word

Table 232 — PG[70]RWE2: Host Interface DQS Driver

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Reserved	Reserved
x	x	x	x	x	x	x	1		Reserved
x	x	x	x	0	0	0	x	Host Interface DQS Output Driver Pull up Impedance control <sup>1</sup>	RZQ / 7 (34 $\Omega$ )
x	x	x	x	0	0	1	x		Reserved
x	x	x	x	0	1	0	x		RZQ / 5 (48 $\Omega$ )
x	x	x	x	0	1	1	x		RZQ / 4 (60 $\Omega$ ) optional
x	x	x	x	1	0	0	x		Reserved
x	x	x	x	1	0	1	x		Reserved
x	x	x	x	1	1	0	x		Reserved
x	x	x	x	1	1	1	x		Reserved
x	0	0	0	x	x	x	x	Host Interface DQS Output Driver Pull Down Impedance control <sup>1</sup>	RZQ / 7 (34 $\Omega$ )
x	0	0	1	x	x	x	x		Reserved
x	0	1	0	x	x	x	x		RZQ / 5 (48 $\Omega$ )
x	0	1	1	x	x	x	x		RZQ / 4 (60 $\Omega$ ) optional
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		Reserved
x	1	1	0	x	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 The bits are sticky, cleared by Power-on Reset not BRST\_n.

## 11.28.6 PG[70]RWE3: DRAM Interface MDQS Driver Control Word

Table 233 — PG[70]RWE3: DRAM Interface MDQS Driver

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Reserved	Reserved
x	x	x	x	x	x	x	1		Reserved
x	x	x	x	0	0	0	x	DRAM Interface MDQS Output Driver Pull up Impedance control <sup>1</sup>	RZQ / 7 (34 $\Omega$ )
x	x	x	x	0	0	1	x		RZQ / 6 (40 $\Omega$ )
x	x	x	x	0	1	0	x		RZQ / 5 (48 $\Omega$ )
x	x	x	x	0	1	1	x		RZQ / 4 (60 $\Omega$ ) optional
x	x	x	x	1	0	0	x		Reserved
x	x	x	x	1	0	1	x		Reserved
x	x	x	x	1	1	0	x		Reserved
x	x	x	x	1	1	1	x		Reserved
x	0	0	0	x	x	x	x	DRAM Interface MDQS Output Driver Pull Down Impedance control <sup>1</sup>	RZQ / 7 (34 $\Omega$ )
x	0	0	1	x	x	x	x		RZQ / 6 (40 $\Omega$ )
x	0	1	0	x	x	x	x		RZQ / 5 (48 $\Omega$ )
x	0	1	1	x	x	x	x		RZQ / 4 (60 $\Omega$ ) optional
x	1	0	0	x	x	x	x		Reserved
x	1	0	1	x	x	x	x		Reserved
x	1	1	0	x	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 The bits are sticky, cleared by Power-on Reset not BRST\_n.



## 11.28.7 PG[70]RWE4: MDB Training Mode Control Word

Table 234 — PG[70]RWE4: MDB Training Mode

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ Static Mux Mode for DQ	Disable
x	x	x	x	x	x	x	1	Pass Through and Transparent modes <sup>1</sup> .	Enable
x	x	x	x	x	x	0	x	Swizzle Discovery Static Mode	Disable
x	x	x	x	x	x	1	x		Enable
x	x	x	x	x	0	x	x	Pseudo Channel Selection for DQ Pass-Through Mode and Transparent Mode	Pseudo- Channel 0 (PS0)
x	x	x	x	x	1	x	x		Pseudo- Channel 1 (PS1)
x	x	x	x	0	x	x	x	Pseudo Channel 0 Target Enable for MRW Snoop <sup>2</sup>	Disable
x	x	x	x	1	x	x	x		Enable
x	x	x	0	x	x	x	x	Pseudo Channel 1 Target Enable for MRW Snoop <sup>2</sup>	Disable
x	x	x	1	x	x	x	x		Enable
x	x	0	x	x	x	x	x	DQ Pass Through and Transparent mode strobe select <sup>3</sup>	DQS[0] passed to MDQS[0]
x	x	1	x	x	x	x	x		DQS[1] passed to MDQS[0]
x	0	x	x	x	x	x	x	DQ Pass Through Mode in write direction Strobe Divide by 2 for PDA Enumeration	Disabled
x	1	x	x	x	x	x	x		Enabled. Divides the strobes by two when in the Host to DRAM direction.
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 When this bit is set, PS selection for each DQ is done through PG[70]RWE5 OP[7:0]. When this bit is cleared, DQ Pass through mode and transparent mode PS selection is determined by PG70RWE4[2] and applies to all DQ bits and DQS.

NOTE 2 Bits 3 and 4 determine which pseudo-channel(s) are being targeted by MRWs as far as MRW snooping is concerned. The encoding of PG70RWE4[4:3] is as follows:

00: No snooping, no update.

01: PS0 populates PG8RW[E6:E3] with MR30 ~ MR26, and PG8RWE2[2:0] with MR25.

10: PS1 populates PG8RW[EC:E9] with MR30 ~ MR26, and PG8RWE2[6:4] with MR25.

11: populates both PG8RW[E6:E3] and PG8RW[EC:E9] with MR30 ~ MR26, and PG8RWE2[6:4,2:0] with MR25.

NOTE 3 When x8 strobing is used for the memory side and x4 strobing is used on the Host side, this bit determines which DQS from the Host is passed to the MDQS[0] strobe pair.

### 11.28.8 PG[70]RWE5: MDB Static Mux Select for DQ Pass Through and Transparent Modes Control Word

Table 235 — PG[70]RWE5: MDB Static Mux Select for DQ Pass Through and Transparent Modes<sup>1,2</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ0 Mux Select for Static DQ Pass Through Mode and Transparent modes	PS0
x	x	x	x	x	x	x	1		PS1
x	x	x	x	x	x	0	x	DQ1 Mux Select for Static DQ Pass Through Mode and Transparent modes	PS0
x	x	x	x	x	x	1	x		PS1
x	x	x	x	x	0	x	x	DQ2 Mux Select for Static DQ Pass Through Mode and Transparent modes	PS0
x	x	x	x	x	1	x	x		PS1
x	x	x	x	0	x	x	x	DQ3 Mux Select for Static DQ Pass Through Mode and Transparent modes	PS0
x	x	x	x	1	x	x	x		PS1
x	x	x	0	x	x	x	x	DQ4 Mux Select for Static DQ Pass Through Mode and Transparent modes	PS0
x	x	x	1	x	x	x	x		PS1
x	x	0	x	x	x	x	x	DQ5 Mux Select for Static DQ Pass Through Mode and Transparent modes	PS0
x	x	1	x	x	x	x	x		PS1
x	0	x	x	x	x	x	x	DQ6 Mux Select for Static DQ Pass Through Mode and Transparent modes	PS0
x	1	x	x	x	x	x	x		PS1
0	x	x	x	x	x	x	x	DQ7 Mux Select for Static DQ Pass Through Mode and Transparent modes	PS0
1	x	x	x	x	x	x	x		PS1

NOTE 1 This register is significant for DQ Pass Through and Transparent modes only if the DQ Static Mux Mode for DQ Pass Through is enabled in the MDB Training Mode register [PG\[70\]RWE4\[0\]](#)=1.

NOTE 2 This register is also significant in MRD, MWD, DWL, and MRE modes to select corresponding pseudo-channel feedback back to the Host regardless of the setting of [PG\[70\]RWE4\[0\]](#).

### 11.28.9 PG[70]RWE6: MDB Static Mux Select for Swizzle Discovery Control Word

Table 236 — PG[70]RWE6: MDB Static Mux Select for Swizzle Discovery

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DQ0 Output in Swizzle Discovery Static Mode	0
x	x	x	x	x	x	x	1		1
x	x	x	x	x	x	0	x	DQ1 Output in Swizzle Discovery Static Mode	0
x	x	x	x	x	x	1	x		1
x	x	x	x	x	0	x	x	DQ2 Output in Swizzle Discovery Static Mode	0
x	x	x	x	x	1	x	x		1
x	x	x	x	0	x	x	x	DQ3 Output in Swizzle Discovery Static Mode	0
x	x	x	x	1	x	x	x		1
x	x	x	0	x	x	x	x	DQ4 Output in Swizzle Discovery Static Mode	0
x	x	x	1	x	x	x	x		1
x	x	0	x	x	x	x	x	DQ5 Output in Swizzle Discovery Static Mode	0
x	x	1	x	x	x	x	x		1
x	0	x	x	x	x	x	x	DQ6 Output in Swizzle Discovery Static Mode	0
x	1	x	x	x	x	x	x		1
0	x	x	x	x	x	x	x	DQ7 Output in Swizzle Discovery Static Mode	0
1	x	x	x	x	x	x	x		1

### 11.28.10 PG[70]RWE8: DFE Taps 5, 6, 7, and 8 Control Word

Table 237 — PG[70]RWE8: DFE Taps 5, 6, 7, and 8 Control Word<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DFE Tap 5 Enable	Disable
x	x	x	x	x	x	x	1		Enable
x	x	x	x	x	x	0	x	DFE Tap 6 Enable	Disable
x	x	x	x	x	x	1	x		Enable
x	x	x	x	x	0	x	x	DFE Tap 7 Enable	Disable
x	x	x	x	x	1	x	x		Enable
x	x	x	x	0	x	x	x	DFE Tap 8 Enable	Disable
x	x	x	x	1	x	x	x		Enable
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 PG[70]RWE8[3:0] will be sticky, cleared by power cycle not reset.

### 11.28.11 PG[70]RW[EF:EC]: PS1 or {R2, R3} Group Read Training Mode Setting Status Control Word

Table 238 — PG[70]RW[EF:EC]: PS1 or {R2, R3} Group Read Training Mode Setting Status

RW	Definition	Encoding
PG70 RVEC	Read LFSR0 State Monitor (Read Only)	The Current State of READ LFSR0
PG70 RWED	Read LFSR1 State Monitor (Read Only)	The Current State of READ LFSR1
PG70 RWEE	Write LFSR0 State Monitor (Read Only)	The Current State of WRITE LFSR0
PG70 RWEF	Write LFSR1 State Monitor (Read Only)	The Current State of WRITE LFSR1

### 11.28.12 PG[70]RWF0: DQS / MDQS Strobe Mode Control Word

Table 239 — PG[70]RWF0: DQS / MDQS Strobe Mode<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	DRAM Interface x4 or x8 mode	Disabled (Used for x4 DRAMs)
x	x	x	x	x	x	x	1		Enabled (Used for x8 DRAMs)
x	x	x	x	x	x	0	x	Host Strobe Mode <sup>2</sup>	x4 Mode (default)
x	x	x	x	x	x	1	x		x8 Mode
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

NOTE 1 PG[70]RWF0[1:0] will be sticky, cleared by power cycle not reset.

NOTE 2 The Host Strobe Mode setting is independent of the DRAM Interface x4 or x8 mode setting. The Host Strobe mode can be configured the same as or different from the DRAM Interface. See “Host Interface Strobe Modes”

### 11.28.13 PG[70]RWF4 - Extended Read Preamble Modes for Host to MDB

Table 240 — PG[70]RWF4: Extended Read Preamble modes

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Extended Read Preamble Mode	(default) Normal Operation - No change to Read Preamble
x	x	x	x	x	0	0	1		Extended Mode - 5tHDQS Read Preamble enabled
x	x	x	x	x	0	1	0		Extended Mode - 6tHDQS Read Preamble enabled
x	x	x	x	x	0	1	1		Extended Mode - 7tHDQS Read Preamble enabled
x	x	x	x	x	1	0	0		Extended Mode - 8tHDQS Read Preamble enabled
x	x	x	x	x	1	0	1		Reserved
x	x	x	x	x	1	1	0		Reserved
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	1.5-tHDQS Read Static	(default) Disabled
1	x	x	x	x	x	x	x	Postamble Mode	Enabled

### 11.28.14 PG[70]RWF5: Extended Write Preamble Modes for Host to MDB

Table 241 — PG[70]RWF5: Extended Write Preamble modes

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	0	0	0	Extended Write Preamble Mode	(default) Normal Operation - No change to Write Preamble
x	x	x	x	x	0	0	1		Extended Mode - 5tHDQS Write Preamble enabled
x	x	x	x	x	0	1	0		Extended Mode - 6tHDQS Write Preamble enabled
x	x	x	x	x	0	1	1		Extended Mode - 7tHDQS Write Preamble enabled
x	x	x	x	x	1	0	0		Reserved
x	x	x	x	x	1	0	1		Reserved
x	x	x	x	x	1	1	0		Reserved
x	x	x	x	x	1	1	1		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

### 11.28.15 PG[70]RWF6: Continuous DQS Toggle during Interamble between Host and MDB

Table 242 — PG[70]RWF6: Continuous DQS Toggle Mode

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	x	x	x	0	Continuous DQS Toggle Mode for Reads	(default) Normal operation - Follows normal interamble behavior
x	x	x	x	x	x	x	1		Continuous Toggle Mode for Reads Enabled
x	x	x	x	x	x	0	x	Continuous DQS Toggle Mode for Writes	(default) Normal operation - Follows normal interamble behavior
x	x	x	x	x	x	1	x		Continuous Toggle Mode for Writes Enabled
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x		Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x		Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x		Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x		Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x		Reserved
1	x	x	x	x	x	x	x		Reserved

## 11.28.16 PG[70]RWF9: Programmable Read Delay Control Word

Table 243 — PG[70]RWF9: Programmable Read Delay Control Word<sup>1,2</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	x	0	0	0	0	Programmable Read Delay n Steps of (1/8) * t <sub>HDQS</sub> /2	Delay timing by (0/8) * t <sub>HDQS</sub> /2
x	x	x	x	0	0	0	1		Delay timing by (1/8) * t <sub>HDQS</sub> /2
x	x	x	x	0	0	1	0		Delay timing by (2/8) * t <sub>HDQS</sub> /2
x	x	x	x	0	0	1	1		Delay timing by (3/8) * t <sub>HDQS</sub> /2
x	x	x	x	0	1	0	0		Delay timing by (4/8) * t <sub>HDQS</sub> /2
x	x	x	x	0	1	0	1		Delay timing by (5/8) * t <sub>HDQS</sub> /2
x	x	x	x	0	1	1	0		Delay timing by (6/8) * t <sub>HDQS</sub> /2
x	x	x	x	0	1	1	1		Delay timing by (7/8) * t <sub>HDQS</sub> /2
x	x	x	x	1	0	0	0		Delay timing by (8/8) * t <sub>HDQS</sub> /2
x	x	x	x	1	0	0	1		Reserved
x	x	x	x	.....					Reserved
x	x	x	x	1	1	1	0		Reserved
x	x	x	x	1	1	1	1		Reserved
x	x	x	0	x	x	x	x	Reserved	
x	x	x	1	x	x	x	x	Reserved	
x	x	0	x	x	x	x	x	Reserved	
x	x	1	x	x	x	x	x	Reserved	
0	x	x	x	x	x	x	x	Programmable Read Delay	
1	x	x	x	x	x	x	x	Enable	

NOTE 1 Applies to DQS0, DQS1, DQS1 as CRC and DQ[7:0].

NOTE 2 PG[70]RWF9[7] and PG[70]RWF9[3:0] will be sticky, cleared by power cycle, not Reset.

### 11.28.17 PG[7B]RW[E0,E4,E8,EC,F0,F4,F8,FC] DQ[7:0] and PG[F]RWF6 CRC Lane Receiver DFE Tap 7 Coefficients

Table 244 — PG[7B]RW[E0,E4,E8,EC,F0,F4,F8,FC] DQ[7:0] and PG[F]RWF6 CRC Lane Receiver DFE Tap 7 Coefficients<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Tap 7 DFE Coefficient <sup>2,3,4</sup>	(Default) Tap 7 DFE bias = 0 mV
x	x	x	0	0	0	0	1		Tap 7 DFE bias +1 Tap Steps
x	x	x	0	0	0	1	0		Tap 7 DFE bias +2 Tap Steps
x	x	x	0	0	0	1	1		Tap 7 DFE bias +3 Tap Steps
x	x	x	0	0	1	0	0		Tap 7 DFE bias +4 Tap Steps
x	x	x	0	0	1	0	1		Tap 7 DFE bias +5 Tap Steps
x	x	x	0	0	1	1	0		Tap 7 DFE bias +6 Tap Steps
x	x	x	0	0	1	1	1		Tap 7 DFE bias +7 Tap Steps
x	x	x	0	1	0	0	0		Tap 7 DFE bias +8 Tap Steps
x	x	x	0	1	0	0	1		Tap 7 DFE bias +9 Tap Steps
x	x	x	0	1	0	1	0		Tap 7 DFE bias +10 Tap Steps
x	x	x	0	1	0	1	1		Tap 7 DFE bias +11 Tap Steps
x	x	x	0	1	1	0	0		Tap 7 DFE bias +12 Tap Steps
x	x	x	0	1	1	0	1		Tap 7 DFE bias +13 Tap Steps
x	x	x	0	1	1	1	0		Tap 7 DFE bias +14 Tap Steps
x	x	x	0	1	1	1	1		Tap 7 DFE bias +15 Tap Steps
x	x	x	.....						.....
x	x	x	1	1	1	0	0		Tap 7 DFE bias +28 Tap Steps
x	x	x	1	1	1	0	1		Tap 7 DFE bias +29 Tap Steps
x	x	x	1	1	1	1	0		Tap 7 DFE bias +30 Tap Steps
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Tap 7 Coefficient Sign Bit	(Default) Positive Tap 7 DFE bias when Tap 7 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 7 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 7 DFE bias when Tap 7 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 7 post-cursor)

NOTE 1 Table 79 and Table 89 illustrate the assignment of each control word in the PG[F]RWF6 and PG[7B]RW[E0,E4,E8,EC,F0,F4,F8,FC] group to the corresponding input pin it controls.

NOTE 2 Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification.

NOTE 3 Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 60, “DFE Gain and Tap Coefficient Step Parameters.”

NOTE 4 PG[F]RWF6 and PG[7B]RW[E0,E4,E8,EC,F0,F4,F8,FC] will be sticky, cleared by power cycle not reset.



### 11.28.18 PG[7B]RW[E1,E5,E9,ED,F1,F5,F9,FD] DQ[7:0] and PG[F]RWF7 CRC Lane Receiver DFE Tap 8 Coefficients

Table 245 — PG[7B]RW[E1,E5,E9,ED,F1,F5,F9,FD] DQ[7:0] and PG[F]RWF7 CRC Lane Receiver DFE Tap 8 Coefficients<sup>1</sup>

Setting								Definition	Encoding
OP 7	OP 6	OP 5	OP 4	OP 3	OP 2	OP 1	OP 0		
x	x	x	0	0	0	0	0	Tap 8 DFE Coefficient <sup>2,3,4</sup>	(Default) Tap 8 DFE bias = 0 mV
x	x	x	0	0	0	0	1		Tap 8 DFE bias +1 Tap Steps
x	x	x	0	0	0	1	0		Tap 8 DFE bias +2 Tap Steps
x	x	x	0	0	0	1	1		Tap 8 DFE bias +3 Tap Steps
x	x	x	0	0	1	0	0		Tap 8 DFE bias +4 Tap Steps
x	x	x	0	0	1	0	1		Tap 8 DFE bias +5 Tap Steps
x	x	x	0	0	1	1	0		Tap 8 DFE bias +6 Tap Steps
x	x	x	0	0	1	1	1		Tap 8 DFE bias +7 Tap Steps
x	x	x	0	1	0	0	0		Tap 8 DFE bias +8 Tap Steps
x	x	x	0	1	0	0	1		Tap 8 DFE bias +9 Tap Steps
x	x	x	0	1	0	1	0		Tap 8 DFE bias +10 Tap Steps
x	x	x	0	1	0	1	1		Tap 8 DFE bias +11 Tap Steps
x	x	x	0	1	1	0	0		Tap 8 DFE bias +12 Tap Steps
x	x	x	0	1	1	0	1		Tap 8 DFE bias +13 Tap Steps
x	x	x	0	1	1	1	0		Tap 8 DFE bias +14 Tap Steps
x	x	x	0	1	1	1	1		Tap 8 DFE bias +15 Tap Steps
x	x	x	.....						.....
x	x	x	1	1	1	0	0		Tap 8 DFE bias +28 Tap Steps
x	x	x	1	1	1	0	1		Tap 8 DFE bias +29 Tap Steps
x	x	x	1	1	1	1	0		Tap 8 DFE bias +30 Tap Steps
x	x	x	1	1	1	1	1		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Tap 8 Coefficient Sign Bit	(Default) Positive Tap 8 DFE bias when Tap 8 post-cursor is Logic 1 (Negative bias for Logic 0 Tap 8 post-cursor)
1	x	x	x	x	x	x	x		Negative Tap 8 DFE bias when Tap 8 post-cursor is Logic 1 (Positive bias for Logic 0 Tap 8 post-cursor)

NOTE 1 Table 79 and Table 89 illustrate the assignment of each control word in the PG[F]RWF7 and PG[7B]RW[E1,E5,E9,ED,F1,F5,F9,FD] group to the corresponding input pin it controls.

NOTE 2 Tap coefficient values shown are verified by design and the measurement from device pins is defined in a separate specification.

NOTE 3 Allowable Differential nonlinearity (DNL) and the allowable Integral nonlinearity (INL) are defined in Table 60, “DFE Gain and Tap Coefficient Step Parameters.”

NOTE 4 PG[F]RWF7 and PG[7B]RW[E1,E5,E9,ED,F1,F5,F9,FD] will be sticky, cleared by power cycle not reset.

## 12 Timing Requirements

### 12.1 Input and Output Timing Requirements

Table 246 — Input Timing Requirements

Symbol	Parameter	Conditions	DDR5-3200 to 12800		Unit
			Min	Max	
$f_{\text{CLOCK}}$	BCK Input clock frequency <sup>1</sup>	Application frequency <sup>2</sup> in Mux mode	1400	3248	MHz
		Application frequency <sup>3</sup> in Rank mode	1400	3248	MHz
$f_{\text{TEST}}$	BCK Input clock frequency	Test frequency	280	1400	MHz
$t_{\text{MRD}}$	Control word to control word delay	Number of clock cycles between two control word accesses or one control word access and the following DRAM command.	12	-	$t_{\text{BCK}}$
$t_{\text{MRD\_L}}$	Control word to control word delay	Number of clock cycles between an access to <a href="#">RW86</a> , <a href="#">RW87</a> , <a href="#">RW8A</a> , <a href="#">RW8B</a> , <a href="#">RW8C</a> , <a href="#">RW8E</a> , <a href="#">RW90</a> , <a href="#">RWA0[3:2]</a> , <a href="#">PG[2]RW[FA, F3:F0, E7:E0]</a> <sup>4</sup> , <a href="#">RWDF</a> <sup>5</sup> , <a href="#">PG[70]RW[E3:E2]</a> and the next control word access or DRAM command.	24	-	$t_{\text{BCK}}$
$t_{\text{MRD\_L2}}$	Control word to control word delay	Number of clock cycles between an access to <a href="#">RW80</a> , <a href="#">RW81</a> , <a href="#">RW82</a> , <a href="#">RW83</a> , <a href="#">RW84</a> <sup>6</sup> , <a href="#">RW85</a> <sup>6</sup> , <a href="#">RW8D</a> , <a href="#">RW97</a> , <a href="#">RWA1[2:1]</a> , <a href="#">RWB0[1:0]</a> , <a href="#">PG[0,1,72,73]RW[F1:E0]</a> , <a href="#">RW8F</a> , <a href="#">PG[8]RWE0</a> , <a href="#">PG[8]RWE1</a> , <a href="#">PG[8]RW[E8,ED]</a> , <a href="#">PG[9]RW[EF:EE, EA:E7, E3:E0]</a> , <a href="#">PG[A,71]RW[EF:E8, FF:F8]</a> , <a href="#">PG[70]RW[F0,F4,F5,F6]</a> , and the next control word access or DRAM command. Number of clock cycles between all PBA related control words ( <a href="#">RW81</a> , <a href="#">RW92</a> , <a href="#">RW93</a> ).	48	-	$t_{\text{BCK}}$
$t_{\text{MRD\_L3}}$	Control word to DRAM Command delay for DFE Gain Adjustment	Waiting time between an access to <a href="#">RWA1[0]</a> , <a href="#">PG[5:4]RW[F8, F0, E8, E0]</a> , <a href="#">PG[F]RWF8</a> , <a href="#">RWA2[7:0]</a> and the next DRAM command <sup>7</sup> .	300 in Rank mode; 800 in Mux mode	-	ns
$t_{\text{MRD\_L4}}$	Control word to DRAM Command delay for DFE Vref Settling Time for $16 \leq n < 32$ , where $n$ = number of steps <sup>8</sup>	Waiting time between an access to <a href="#">RWA0[1:0]</a> , <a href="#">PG[6]RW[FF, FE, FB, FA, F7, F6, F3, F2, EF, EE, EB, EA, E7, E6, E3, E2]</a> and the next DRAM command <sup>7</sup> .	300	-	ns
$t_{\text{MRD\_DFE\_Tap}}$	Control word to control word delay	Number of clock cycles between an access to <a href="#">RWA0[7:4]</a> , <a href="#">PG[5:4]RW[FE:F9, F6:F1, EE:E9, E6:E1]</a> , <a href="#">PG[F]RW[FD, F7:F0]</a> , <a href="#">PG[70]RWE8</a> , <a href="#">PG[7B]RW[FD:FC, F9:F8, F5:F4, F1:F0, ED:EC, E9:E8, E5:E4, E1:E0]</a> (Rx DFE Tap enable and coefficients) and the next control word access or DRAM command	64	-	$t_{\text{BCK}}$
$t_{\text{MRD\_CTLE}}$	The Control word to DRAM Command delay for CTLE control and setting updates	The number of clock cycles between an access to <a href="#">PG[D]RW[E2:E0, F8:F0]</a> and the next DRAM command	64	-	$t_{\text{BCK}}$

Table 246 — Input Timing Requirements (cont'd)

Symbol	Parameter	Conditions	DDR5-3200 to 12800		Unit
			Min	Max	
$t_{MRD\_RDCRC}$	The Control word to DRAM Command delay after enabling RD CRC	The number of clock cycles between an access to PG[70]RWE0[2] and the next DRAM command	100	-	ns
$t_{ErrCnt\_Rst}$	Control word to control word delay for Error Counter Reset	Waiting time between Write access to RWA1[3], PG[7]RWF0[0], PG[10]RWF0[1:0] and the next control word access.	32	-	$t_{BCK}$
$t_{TM\_Entry}$	Transparent Mode Entry Time	Delay from MRW that sets RW82[0] = 1 to Transparent Mode features enabled in MDB.	-	250	ns
$t_{MRR}$	Mode Register Read Pattern to Mode Register Read Pattern Command Spacing	Back-to-back MRRs to Data Buffer or Back-to-Back MRRs to DRAM	8	-	$t_{BCK}$
$t_{MRROD1}$	Delay from MRR data postamble to next valid command	MRR from Data Buffer address space to any next valid command or MRR from DRAM address space to any next valid command	8	-	$t_{BCK}$
$t_{MRROD2}$	Delay from WR or RD data postamble to MRR to Data Buffer address space, and delay from the last WR postamble to the subsequent RD to collect the phase error status in HIW/EWTM training mode.	DRAM WR or RD data postamble to MRR to Data Buffer address space during normal operation or training modes, and the last WR data postamble to the subsequent RD to collect the phase error status in HIW/EWTM training mode.	8	-	$t_{BCK}$
$t_{Strap\_Setup}$	BCOM Strap Setup time from BCOM[2:0] stable to BRST_n HIGH-to-LOW transition <sup>9</sup>	Before BRST_n HIGH-to-LOW transition <sup>9</sup>	32	-	$t_{BCK}$
$t_{Strap\_Hold}$	BCOM Strap Hold time from BRST_n LOW-to-HIGH transition to BCOM[2:0] changes	After BRST_n LOW-to-HIGH transition <sup>10</sup>	32	-	$t_{BCK}$
$t_{Strap\_Pulse}$	Minimum BRST_n assertion time for BCOM Strap command		64	-	$t_{BCK}$
$t_{BCOMTM\_Entry}$	Registration of BCOMTM entry from BRST_n LOW-to-HIGH transition to start of training samples time.	After BRST_n LOW-to-HIGH transition <sup>10</sup>	-	64	$t_{BCK}$
$t_{BCOMTM\_Exit}$	Registration of BCOMTM exit from BRST_n LOW-to-HIGH transition to end of training mode.	After BRST_n LOW-to-HIGH transition <sup>10</sup>	-	64	$t_{BCK}$
$t_{BCOM\_1N}$	Time for the Data Buffer to change CMD timing from BRST_n LOW-to-HIGH transition.	After BRST_n LOW-to-HIGH transition <sup>10</sup>	-	64	$t_{BCK}$
$t_{BCOM\_Vref}$	Time for the BVref to settle from BRST_n LOW-to-HIGH transition.	After BRST_n LOW-to-HIGH transition <sup>10</sup>	-	500	ns
$t_{PBA\_Delay}$	Minimum delay from PBA SET ID to PBA SET ID or from PBA SET ID to PBA Exit		$t_{PBA\_DQS\_Delay(max)} + BL/2 + 19ns$	-	ns
$t_{PBA\_DQS\_Delay}$	Delay to rising strobe edge used for sampling DQ during PBA operation <sup>11</sup>		5	18	ns
$t_{PBA\_S}$	DQ Setup Time during PBA Enumerate Programming mode		3	-	$t_{BCK}$

Table 246 — Input Timing Requirements (cont'd)

Symbol	Parameter	Conditions	DDR5-3200 to 12800		Unit
			Min	Max	
$t_{PBA\_H}$	DQ Hold Time during PBA Enumerate Programming mode		3	-	$t_{BCK}$
$t_{WLE}$	The time from the MRWDAT0 cycle to the Data Buffer being in DWL and HWL training modes.		-	32	$t_{BCK}$
$t_{DFETA\_Entry}$	Time from enabling DFETA to when the first Write command can occur		32	-	$t_{BCK}$
$t_{DFETA\_LoopUpdateWait}$	Minimum time from the last Write for a particular iteration to the first Write of the next iteration		$DB\_WL - t_{PDM\_WR} + BL/2 + 64$	-	$t_{BCK}$
$t_{DFETA\_Exit}$	Time from disabling DFETA to when the next valid command can occur		32	-	$t_{BCK}$
$t_{XS}$	DRAM Exit Self Refresh to next valid command not requiring DLL		See DDR5 DRAM Specification		
$t_{RINIT1}$	Minimum BRST_n LOW time after completion of voltage ramp		200	-	$\mu s$
	Minimum BRST_n LOW time with stable power		1	-	$\mu s$
$t_{ACT}$	Delay from BCK Clock Stop condition to Valid BCK Clock that has reached steady phase and frequency	MDB Power-up Initialization (Figure 10), Reset with Stable Power and Stopped Clock (Figure 11), Self Refresh with Clock Stop (Figure 58)	-	10	ns
$t_{CPDED\_DB}$	Minimum time of valid BCK clock after received SRE command for Self Refresh		$\max(8 \cdot t_{BCK}, 5ns)$	-	ns
$t_{CSSR\_DB}$	Minimum time of stopped BCK clock		$\max(32 \cdot t_{BCK}, 20ns)$	-	ns
$t_{CPDED2SR\_X\_DB}$	Minimum time between SRE for Self Refresh and BCS_n LOW pulse signaling Self Refresh Exit if BCK clock does not stop		$\max(16 \cdot t_{BCK}, 10ns)$	-	ns
$t_{ZQCAL}$	ZQ Calibration Time		1	-	$\mu s$
$t_{ZQLAT}$	ZQ Calibration Latch Time		$\max(8 \cdot t_{BCK}, 30ns)$	-	ns
$t_{Cont\_Exit\_Delay}$	Registration of MRW Continuous Burst Mode Exit to next valid command delay		128	-	$t_{BCK}$
$t_{Cont\_Exit}$	Registration of MRW Continuous Burst Mode Exit to end of training mode		-	128	$t_{BCK}$
$t_{TrkCalcInit}$	During $t_{DQS2DQ}$ tracking initialization mode, this is the time from the end of latest DRAM data burst for the second DRAM-space MRR of a pair to the end of the corresponding calculation period <sup>12</sup>		-	256	$t_{BCK}$

Table 246 — Input Timing Requirements (cont'd)

Symbol	Parameter	Conditions	DDR5-3200 to 12800		Unit
			Min	Max	
$t_{TrkCalcCur}$	During tDQS2DQ tracking mode, this is the time from the end of latest DRAM data burst for the second DRAM-space MRR of a pair to the end of the corresponding calculation period. This parameter includes $t_{TrkUpdate8}$ . <sup>13</sup>	-	-	256	$t_{BCK}$
$t_{TrkUpdate}$	The time for the MDB to update MDQ to MDQS delay	-	-	32	$t_{BCK}$
$t_{DESTM}$	Max time required for MDB to complete Self Train after receiving Start Training Command	-	-	2500	ms

NOTE 1 Including SSC according Section 15.5, “RX Spread Spectrum Clocking (SSC) Capability,” on page 283.

NOTE 2 All specified timing parameters apply.

NOTE 3 All specified timing parameters apply.

NOTE 4 When Vref settings are updated, it is necessary to meet the Vref settling times defined in Table 287, “Internal Vref [M]DQ and BVref Specifications,” in addition to meeting  $t_{MRD\_L}$ .

NOTE 5 Applies to the timing between MRW that updates the CW Page Control Word and the following MRW or MRR command targeting the paged control word address space (i.e., [RWE0](#) to [RWFF](#)).

NOTE 6 A  $t_{STAB}$  waiting time is required when changing the setting in [RW84\[3:0\]](#) (RDIMM Operating Speed) and [RW85](#) (Fine Granularity Operating Speed).

NOTE 7 For other commands, a waiting time  $t_{MRD\_L2}$  applies for any control word listed in this set.

NOTE 8 For other cases of n, see Table 288, “DFE\_Vref Specification.”

NOTE 9 Measured to  $BRST\_n$  HIGH-to-LOW crossing of  $VIH(DC)\_BRST$  as defined in Table 258, “CMOS Rail-to-Rail Input Levels for  $BRST\_n$ ,” and Figure 112, “ $BRST\_n$  Input Slew Rate Definition” on page 280.

NOTE 10 Measured from  $BRST\_n$  LOW-to-HIGH crossing of  $VIH(AC)\_BRST$  as defined in Table 258, “CMOS Rail-to-Rail Input Levels for  $BRST\_n$ ,” and Figure 112, “ $BRST\_n$  Input Slew Rate Definition” on page 280.

NOTE 11 The range of  $tPBA\_DQS\_DELAY$  specifies the full range of when the minimum of 16 strobe edges can be sent by the Host.

NOTE 12 This parameter also applies when Periodic Update registers, [PG\[A\]RW\[E1, E3, E5, E7\]](#), are written directly by MRW command, and it is measured from the last cycle of the MRW sequence on the BCOM[2:0] bus.

NOTE 13 This parameter also applies when Periodic Update registers, [PG\[A\]RW\[F1, F3, F5, F7\]](#), are written directly by MRW command, and it is measured from the last cycle of the MRW sequence on the BCOM[2:0] bus.

## 12.1 Input and Output Timing Requirements (cont'd)

Table 247 — Output Timing Requirements<sup>1</sup>

Symbol	Parameter	Conditions	DDR5-3200 to 12800		Unit
			Min	Max	
$t_{PDM\_RD}^2$	MDQS to DQS Propagation Delay with DQ Bus Read CRC feature disabled	1.1 V Operation with DRAM interface matched receivers <sup>3,4</sup>	$1.1 + (1/4) * t_{BCK}$	$1.87 + (1/4) * t_{BCK}$	ns
		1.1 V Operation with DRAM interface unmatched receivers <sup>3,4</sup>	$1.1 + (1+1/4) * t_{BCK}$	$1.87 + (1+1/4) * t_{BCK}$	
$t_{PDM\_RD\_CRC}^2$	MDQS to DQS Propagation Delay with DQ Bus Read CRC feature enabled	1.1 V Operation with DRAM interface matched receivers <sup>3,4</sup>	$1.1 + (1/4) * t_{BCK}$	$2.4 + (1/4) * t_{BCK}$	ns
		1.1 V Operation with DRAM interface unmatched receivers <sup>3,4</sup>	$1.1 + (1+1/4) * t_{BCK}$	$2.4 + (1+1/4) * t_{BCK}$	
$t_{PDM\_WR}^5$	DQS to MDQS Propagation Delay with DQ Bus Write CRC feature enabled or disabled	1.1 V Operation <sup>1,3</sup>	$1.1 + (1/4) * t_{BCK}$	$1.87 + (1/4) * t_{BCK}$	ns
$t_{TPM\_DQD}$	MDQ/MDQS to DQ/DQS and DQ/DQS to MDQ/MDQS Propagation Delay in Transparent Mode <sup>6</sup>	1.1 V Operation <sup>1,3</sup>	0.3	1.25	ns
$D_{TPM\_DQ}$	Delta between shortest and longest propagation delays within each DQx/DQSx and MDQx/MDQSx nibble in Transparent Mode <sup>6</sup>	1.1 V Operation <sup>1,3</sup>	-	0.4	ns
$D_{TPM\_DQS\_DIV}$	Additional propagation delay incurred by DQS in DQ Pass Through mode with divider mode	1.1 V Operation <sup>1,3</sup>	-	0.4	ns
$D_{TPM\_DQS\_x4x8}$	Additional propagation delay incurred by DQS in Transparent Mode or DQ Pass Through mode when forwarded from a x8 strobe to an upper x4 strobe	1.1 V Operation <sup>1,3</sup>	-	0.4	ns
$t_{MRD\_TM}$	Delay between data direction changes in Transparent Mode	Number of clock cycles between Read to Write or Write to Read transactions in Transparent Mode	8	-	tBCK
$t_{CMP\_MRD\_DLY}$	DRAM Read data comparator output delay in MRD training mode. <sup>7</sup>		-	16	tBCK
$t_{CMP\_MRD\_PW}$	Comparator output pulse width for each MRR operation in MRD training mode. <sup>8</sup>		4	-	tBCK
$t_{RCEN2DQ}$	Delay from internal MDB Receive Enable to DQ response in MRE Training Mode		-	5	ns
$t_{STAB\_DB}$	Stabilization time for BCK_t/ BCK_c <sup>9</sup>	BCK_t/BCK_c stable	-	3.5	μs
$t_{STAB\_DBVLD}$	Stabilization time for commands requiring use of data path <sup>10</sup>	BCK_t/BCK_c stable	-	4.14	μs

Table 247 — Output Timing Requirements<sup>1</sup> (cont'd)

Symbol	Parameter	Conditions	DDR5-3200 to 12800		Unit
			Min	Max	
$t_{\text{STAB\_DBCMD}}$	MRDIMM stabilization time for commands not requiring use of data path <sup>11,12</sup>	MRCD DCK_t/DCK_c stable	-	3.532	$\mu\text{s}$
$t_{\text{STAB\_DBDATA}}$	MRDIMM stabilization time for commands requiring use of data path <sup>13,12</sup>	MRCD DCK_t/DCK_c stable	-	4.3	$\mu\text{s}$
$t_{\text{SR\_PARKoff}}$	Delay to RTT_PARK disabled by the MDB	RTT_PARK disable triggered by SRE for Self Refresh	-	32	tBCK
		RTT_PARK disable triggered by Clock Stop condition	-	24	ns
$t_{\text{SR\_PARKon}}$	Delay to RTT_PARK enabled by the MDB	RTT_PARK enable triggered by first NOP after exit from Clock Stop	-	32	tBCK
		RTT_PARK enable triggered by exit from Clock Stop	-	3	$\mu\text{s}$
$t_{\text{RST\_PARKon}}$	Delay to RTT_PARK enabled by the MDB	RTT_PARK enable triggered by BRST_n rising edge	-	3.5	$\mu\text{s}$
$t_{\text{BCOMTM\_Valid}}$	Time from sample evaluation to output on DQ pins.		-	20	ns
$t_{\text{BCOMTM\_DQ\_Window}}$	Time output is available on DQ pins.		2	-	tBCK
$t_{\text{WLO\_DB}}$	The MDQx to DQx propagation delay during DWL training mode		0.3	1.25	ns
$t_{\text{WLOE\_DB}}$	Delay error between the earliest and the latest DQx during DWL training mode		-	0.4	ns
$t_{\text{SDOn}}$	Delay from MRW command to DQS driven		-	max(48*tBCK, 20ns)	ns
$t_{\text{SDOff}}$	Delay from MRW command to DQS disabled		-	max(48*tBCK, 20ns)	ns
$t_{\text{LB\_Entry}}$	Loopback Mode Entry Time	Delay from MRW that sets RW8D[0] = 1 to valid data driven on LBTXDQ, LBTXDQS.	-	64	tBCK
$t_{\text{LB\_Exit}}$	Loopback Mode Exit Time	Delay from MRW that sets RW8D[0] = 0 to RTT_Loopback applied on LBTXDQ, LBTXDQS.	-	64	tBCK
$t_{\text{DOUT\_LB\_A}}$	Rising edge of DQS to rising edge of LBTDQS for phase A		-	10	ns
$t_{\text{DOUT\_LB\_B}}$	Falling edge of DQS to rising edge of LBTXDQS for phase B		-	10	ns
$t_{\text{DOUT\_LB\_C}}$	Rising edge of DQS to rising edge of LBTXDQS for phase C		-	10	ns
$t_{\text{DOUT\_LB\_D}}$	Falling edge of DQS to rising edge of LBTXDQS for phase D		-	10	ns
$t_{\text{LBTXDQ\_Set}}$	LBDQ_TX Setup time		0.6	-	tHDQS
$t_{\text{HW\_LBTXDQS}}$	LBTXDQS HIGH Pulse width		0.8	1.2	tHDQS
$t_{\text{LW\_LBTXDQS}}$	LBTXDQS LOW Pulse width		0.8	1.2	tHDQS
$t_{\text{LBTXDQ\_Hld}}$	LBTXDQ Hold time		0.6	-	tHDQS
$t_{\text{LBTXDQ\_VW}}$	Data Valid Window of LBTXDQ		1.6	-	tHDQS
$t_{\text{Static\_MRR\_Entry}}$	Delay from MRW that sets RWC2 to DQ being driven		-	64	tBCK

**Table 247 — Output Timing Requirements<sup>1</sup> (cont'd)**

Symbol	Parameter	Conditions	DDR5-3200 to 12800		Unit
			Min	Max	
tStatic_MRR_Exit	Delay from MRW that sets RWC2 to DQ park		-	64	tBCK
tCRC_ALERT_PW	Write CRC Alert Pulse Width		12	20	tBCK
tALERT_MDB	Output LBTXDQ delay to send WR CRC error pulse		-	2	ns
tCRC_Calc_WR	Write CRC calculation time		-	1	ns
tCRC_Calc_RD	Read CRC calculation time		-	1	ns
tRD_VAR	MDQS Trained Read Timing Variance <sup>14</sup>	1.1 V Operation	-	500	ps
tWR_VAR	MDQS Trained Write Timing Variance <sup>15</sup>	1.1 V Operation	-	500	ps

NOTE 1 See diagram (Figure 160, “Reference Load for Output Timing and Output Slew Rate”).

NOTE 2 In Mux mode, (1/4)\*tBCK in the Min/Max values apply to PS0 only. For PS1, (1/2)\*tBCK is applied.

tPDM\_RD\_CRC includes tCRC\_Calc\_RD.

NOTE 3 These parameters are only guaranteed after the correct speed range has been programmed in [RW84\[3:0\]](#) and [RW85](#).

NOTE 4 These values are defined for the OP[4:0] bits of the lower and upper nibble Read delay a control words [PG\[1:0\]RW\[E5:E4\]](#) at their power on default of ‘00\_0000’. The tPDM\_RD values are defined for DQS pre-launch settings in [RW8F](#) all cleared to zero.

NOTE 5 In Mux mode, (1/4)\*tBCK in the Min/Max values apply to PS1 only. For PS0, (1/2)\*tBCK is applied.

NOTE 6 This parameter also applies to DQ Pass Through, as well as HWL and DWL training modes.

NOTE 7 Measured from when the last bits of the data burst reach the DDR5MDB02 MDQ pins to the last DQ output toggling for a valid comparison result value.

NOTE 8 DQ LOW pulses are only allowed in case of data comparison mismatch. For a sequence of MRR operations without any data comparison mismatch, the DQ output must remain stable HIGH (i.e., without LOW glitches).

NOTE 9 This parameter also applies to control word writes to [RW84/RW85](#). At lower data rate, a longer stabilization time is required. At down-bin data rate, the stabilization time is up to 10us. At the test frequency range, the stabilization time is up to 50 μs.

NOTE 10 Applies only to Self Refresh Exit with Clock Stop and frequency change.

NOTE 11 Measured from start of MRCD DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the MRDIMM BCOM bus interface but does not require the use of data path (e.g., SRX, NOP, etc.).

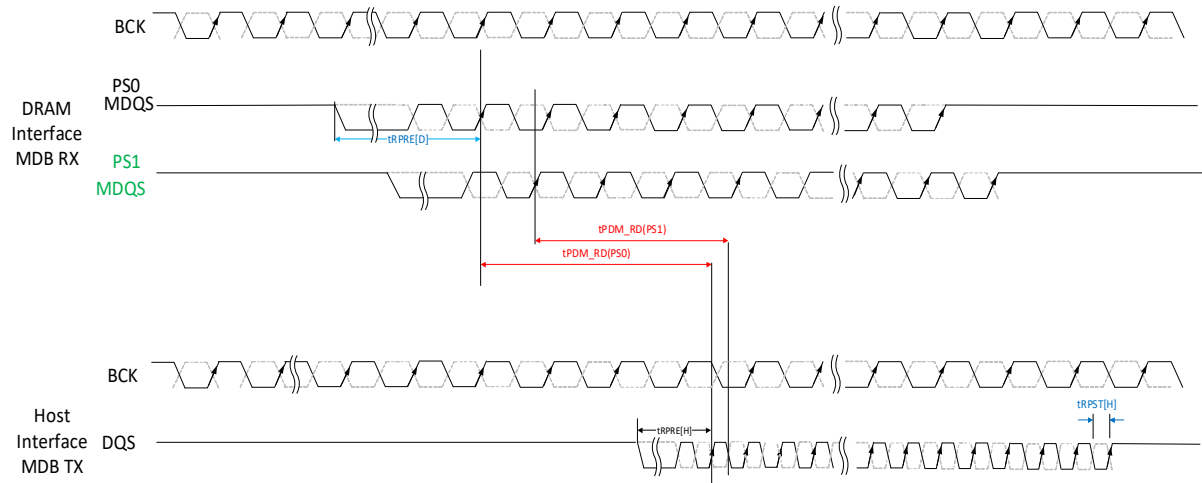
NOTE 12 Applies only to Self Refresh Exit with Clock Stop but without frequency change.

NOTE 13 Measured from start of MRCD DCK after Exit from Self Refresh with Clock Stop to the first DCA Command that gets forwarded to the MRDIMM BCOM bus interface and requires the use of data path (e.g., WR, RD).

NOTE 14 Rank, Nibble, and Pseudo-channel alignment is always active in the MDB due to the common Host clock.

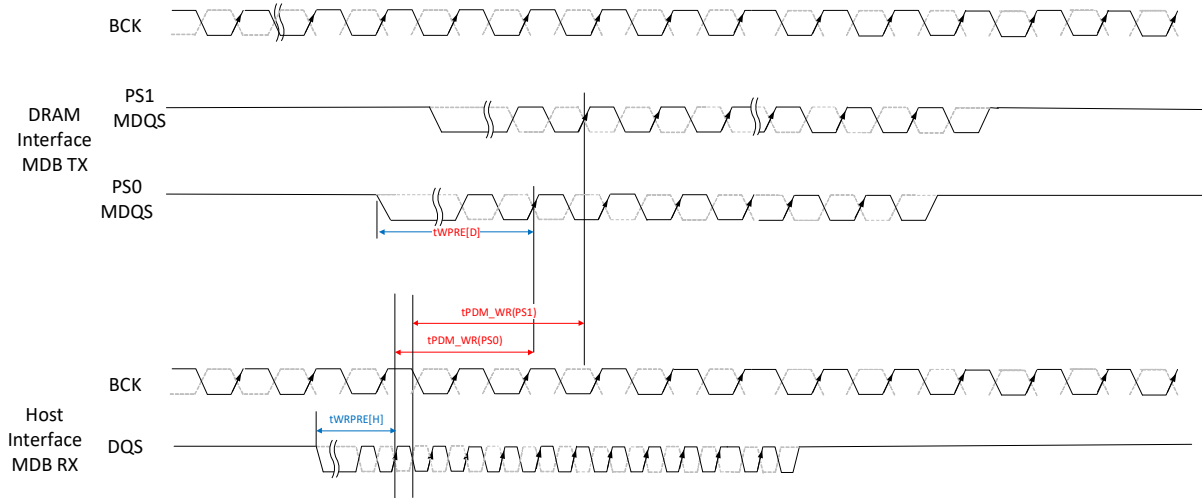


## 12.1 Input and Output Timing Requirements (cont'd)



NOTE: Measured at MDQS cross point to DQS Cross point

**Figure 94 —  $t_{PDM\_RD}$  Latency Measurement**



NOTE: Measured at DQS cross point to MDQS Cross point

**Figure 95 —  $t_{PDM\_WR}$  Latency Measurement**

## 12.2 Operating Specification for Different Package Ranks

### 12.2.1 Operating Specification for Different Package Ranks in Mux Mode

**Table 248 — DDR5MDB02 Operating Specification for Different Package Ranks (from Rx to Ry) in Mux Mode**

Type	Symbol	Parameter	DDR5 - 3200 to 12800		Units
			Min <sup>1, 2, 3</sup>	Max	
RD-RD <sup>4</sup>	$t_{\text{RDRD\_MDQS}}$	Read to Read Command Spacing MDQS Interface of the same PS	$BL/2 + 2*t_{\text{BCK}} + t_{\text{RPRE(D)}} + (t_{\text{RPST(D)}} - 0.5*t_{\text{BCK}}) + (MRE(Rx) - MRE(Ry))$	-	$t_{\text{DCK (avg)}}$
	$t_{\text{RDRD\_MDQ}}$	Read to Read Command Spacing MDQ Interface of the same PS	$BL/2 + 2*t_{\text{BCK}} + (MRE(Rx) - MRE(Ry)) + (MDQS\_RD\_Dly(Rx) - (MDQS\_RD\_Dly(Ry)))$		
WR-WR <sup>4</sup>	$t_{\text{WRWR\_MDQS}}$	Write to Write Command Spacing MDQS Interface of the same PS	$BL/2 + 2*t_{\text{BCK}} + t_{\text{WPST(D)}} + (t_{\text{WPST(D)}} - 0.5*t_{\text{BCK}}) + (DWL(Rx) - DWL(Ry))$	-	$t_{\text{DCK (avg)}}$
	$t_{\text{WRWR\_MDQ}}$	Write to Write Command Spacing MDQ Interface of the same PS	$BL/2 + 2*t_{\text{BCK}} + (DWL(Rx) - DWL(Ry)) + (t_{\text{FinalWriteDelay(Rx)}} - t_{\text{FinalWriteDelay(Ry)}})$		
RD-WR <sup>5</sup>	$t_{\text{RDWR\_DQS}}$	Read to Write Command Spacing DQS Interface of the same or different PS	$(MRE(Rx) - DWL(Ry) + 2*t_{\text{BCK}}) + (t_{\text{PDM\_RD(Rx)}} + t_{\text{PDM\_WR(Ry)}}) + t_{\text{WPST(H)}} + BL/2 + (t_{\text{RPST(H)}} - 0.5*t_{\text{HDQS}}) + 2*t_{\text{BCK}} - \text{DQS\_Prelaunch}$	-	$t_{\text{DCK (avg)}}$
	$t_{\text{RDWR\_DQ}}$	Read to Write Command Spacing DQ Interface of the same or different PS	$(MRE(Rx) - DWL(Ry) + 2*t_{\text{BCK}}) + (t_{\text{PDM\_RD(Rx)}} + t_{\text{PDM\_WR(Ry)}}) + BL/2 + 2*t_{\text{BCK}} + 0.25*t_{\text{HDQS}} - t_{\text{Rx\_dqs2dq(Ry)}}$	-	
WR-RD <sup>6</sup>	$t_{\text{WRRD\_MDQS}}$	Write to Read Command Spacing MDQS interface of the same PS	$(DWL(Rx) - MRE(Ry) - 2*t_{\text{BCK}}) + t_{\text{RPRE(D)}} + BL/2 + (t_{\text{WPST(D)}} - 0.5*t_{\text{BCK}}) + 2*t_{\text{BCK}}$	-	$t_{\text{DCK(avg)}}$
	$t_{\text{WRRD\_MDQ}}$	Write to Read Command Spacing MDQ interface of the same PS	$(DWL(Rx) - MRE(Ry) - 2*t_{\text{BCK}}) + t_{\text{FinalWriteDelay(Rx)}} + BL/2 + 2*t_{\text{BCK}} + 0.25*t_{\text{BCK}} - t_{\text{MDQ\_RD\_Dly(Ry)}}$		
	$t_{\text{WRRD\_DQS}}$	Write to Read Command Spacing DQS interface of the same or different PS	$(DWL(Rx) - MRE(Ry) - 2*t_{\text{BCK}}) - t_{\text{PDM\_WR(Rx)}} - t_{\text{PDM\_RD(Ry)}} + t_{\text{RPRE(H)}} + \text{DQS\_Prelaunch} + BL/2 + (t_{\text{WPST(H)}} - 0.5*t_{\text{HDQS}}) + 2*t_{\text{BCK}}$	-	$t_{\text{DCK (avg)}}$

NOTE 1 The Host is required to meet all of the minimum values in this table.

NOTE 2 For each equation, Rx and Ry must be selected so that the equation is maximized.

NOTE 3 The result of each equation is rounded up to the nearest tDCK. The tPDM\_RD and tPDM\_WR in these equations are vendor specific, and are equal to the calibrated values after training by Host.

NOTE 4 DQS/DQ interface no constraint.

NOTE 5 MDQS/MDQ interface of the same or different PS: no constraint.

NOTE 6 MDQS/MDQ of different PS: no constraint.

### 12.2.1 Operating Specification for Different Package Ranks in Mux Mode (cont'd)

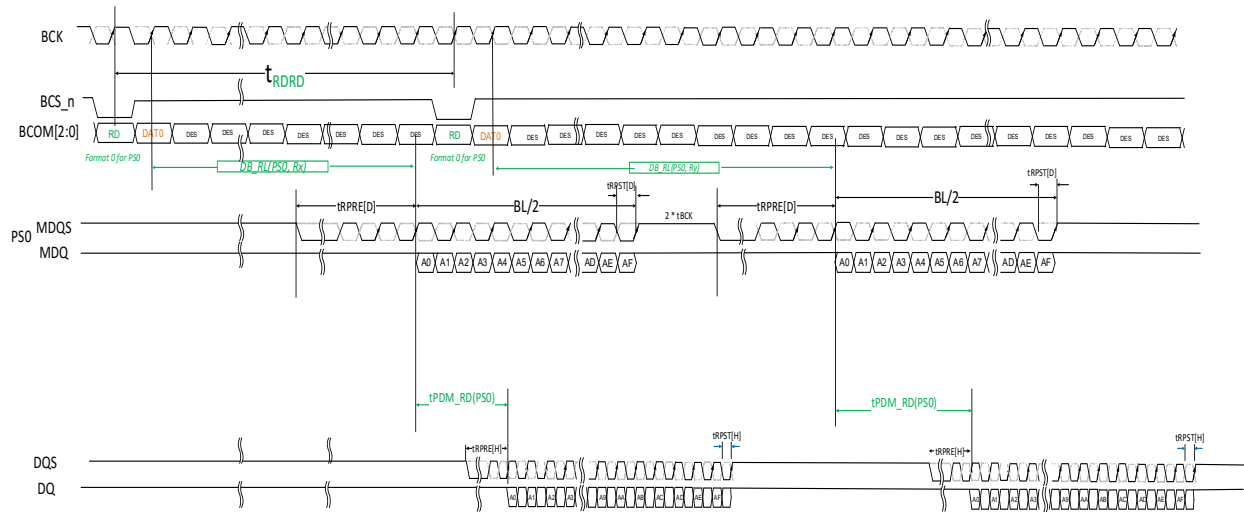


Figure 96 —  $t_{RDRD}$  Example for 2 and 4 Rank

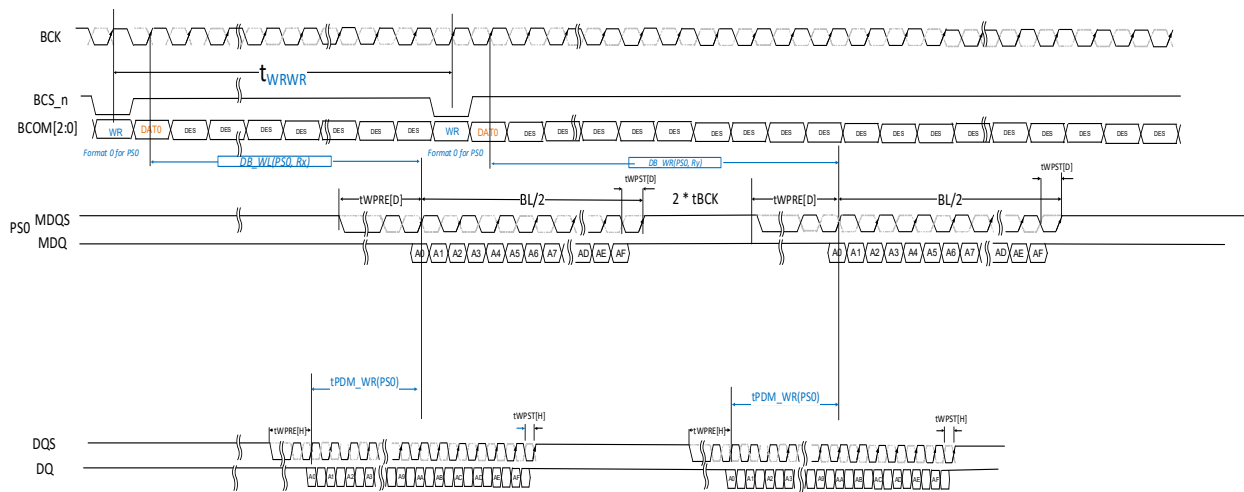


Figure 97 —  $t_{WRWR}$  Example for 2 and 4 Rank

12.2.1 Operating Specification for Different Package Ranks in Mux Mode (cont'd)

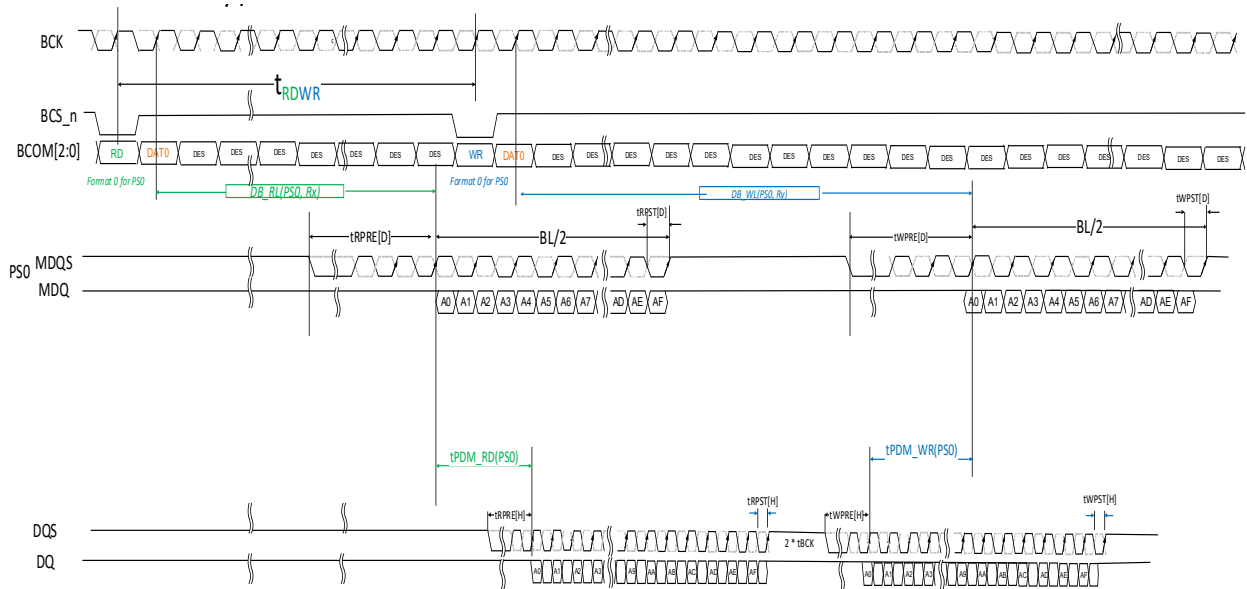


Figure 98 —  $t_{RDWR}$  Example for 2 and 4 Rank

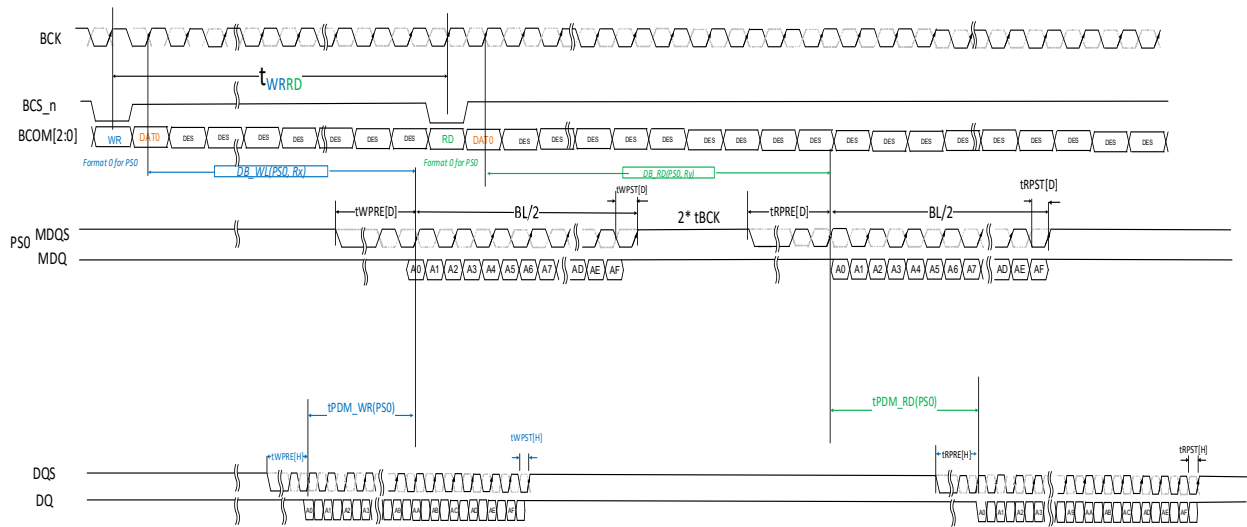


Figure 99 —  $t_{WRRD}$  Example for 2 and 4 Rank

### 12.2.2 Operating Specification for Different Package Ranks in Rank Mode

**Table 249 — DDR5MDB02 Operating Specification for Different Package Ranks  
(from Rx to Ry) in Rank Mode**

Type	Symbol	Parameter	DDR5 - 3200-6400		Units
			Min <sup>1, 2, 3</sup>	Max	
RD-RD	$t_{RDRD}$	Read to Read Command Spacing	$t_{RPRE} + BL/2 + [t_{RPST} - 0.5]$ + max [MRE(Rx) – MRE(Ry), [MRE(Rx) + MDQS_RD_Dly(Rx) – MRE(Ry) – MDQS_RD_Dly(Ry)] ] + 2	-	tDCK (avg)
WR-WR	$t_{WRWR\_MDQS}$	Write to Write Command Spacing	$t_{WPRE} + BL/2 + [t_{WPST} - 0.5]$ + [DWL(Rx) – DWL(Ry)] + 2	-	tDCK (avg)
	$t_{WRWR\_MDQ}$	Write to Write Command Spacing	$BL/2$ + [DWL(Rx) + tFinalWriteDelay(Rx) <sup>4</sup> ] – [DWL(Ry) + tFinalWriteDelay(Ry) <sup>4</sup> ] + 2	-	tDCK (avg)
RD-WR	$t_{RDWR\_DQS}$	Read to Write Command Spacing	$t_{PDM\_RD(max)}^5 + t_{PDM\_WR(max)} + t_{WPRE} + BL/2$ + 2 + [t <sub>RPST</sub> – 0.5] – DQS_Prelaunch + [MRE(Rx) – DWL(Ry)] + 2	-	tDCK (avg)
	$t_{RDWR\_DQ}$	Read to Write Command Spacing	$t_{PDM\_RD(max)}^5 + t_{PDM\_WR(max)} + BL/2 + 2$ + [0.25 – tRx_DQS2DQ(max) <sup>6</sup> ] + [MRE(Rx) – DWL(Ry)] + 2	-	tDCK (avg)
WR-RD	$t_{WRRD\_MDQS}$	Write to Read Command Spacing	$t_{RPRE} + BL/2 - 2 + [t_{WPST} - 0.5]$ + [DWL(Rx) – MRE(Ry)] + 2	-	tDCK (avg)
	$t_{WRRD\_DQS}$	Write to Read Command Spacing	$t_{RPRE} - t_{PDM\_RD(min)}^5 - t_{PDM\_WR(min)}$ + $BL/2 - 2 + [t_{WPST} - 0.5] + DQS\_Prelaunch$ + [DWL(Rx) – MRE(Ry)] + 2	-	tDCK (avg)
	$t_{WRRD\_MDQ}$	Write to Read Command Spacing	$BL/2 - 2 + t_{FinalWriteDelay}(Rx)^4$ + [0.25 – tMDQS_RD_Dly <sup>7</sup> ] + [DWL(Rx) – MRE(Ry)] + 2	-	tDCK (avg)

NOTE 1 The Host is required to meet all of the minimum values in this table.

NOTE 2 For each equation, Rx and Ry must be selected so that the equation is maximized.

NOTE 3 The result of each equation is rounded up to the nearest tDCK.

NOTE 4 Note: tFinalWriteDelay(Rx) = tMdqWriteBaselineDelay(Rx) + tDram\_DqsDelay\_Change(Rx) + Per-bit\_MDQ\_Write\_Delay. tDram\_DqsDelay\_Change can be positive or negative, can vary between periodic updates, and it is constrained by tDQS2DQ\_temp and tDQS2DQ\_volt parameters defined in the DDR5 SDRAM .

NOTE 5 In some implementations, t<sub>PDM\_RD</sub> may include adjustment for PG[1:0]RW[E5:E4].

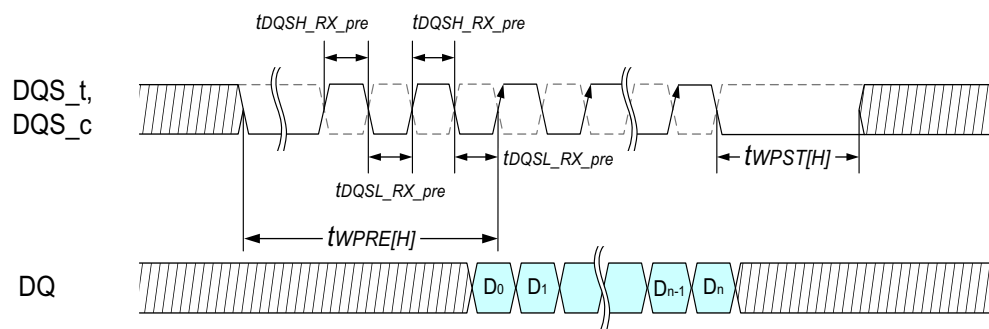
NOTE 6 Refer to Table 265, “Rx [M]DQS Jitter Sensitivity Specification for DDR5-3200 to 12800,”.

NOTE 7 MDQ Read timing offset from PG[1:0]RW[E5:E4].

## 12.3 Preamble and Postamble Timings

### 12.3.1 RX Preamble and Postamble Timings

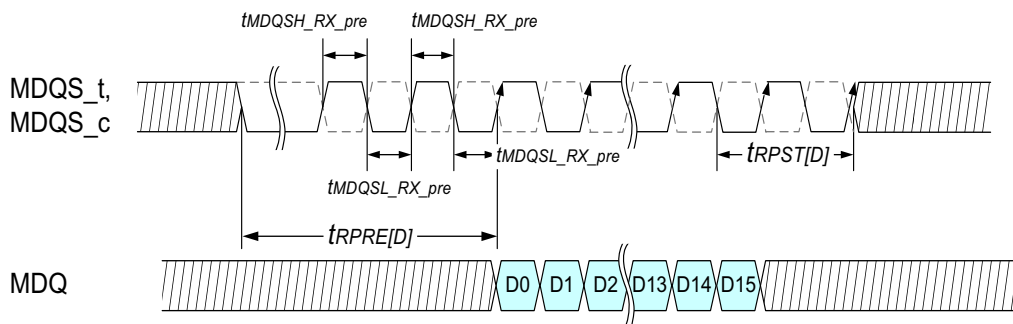
During Write and Read operations, input receiver aligns the strobe with [M]DQ according to the preamble settings, and strobe should meet timing requirements ( $t_{DQSH\_RX\_pre}$ ,  $t_{DQSL\_RX\_pre}$ ) to guarantee enough timing margin by setting the window for strobe during the preamble time frame. On the Host DQ interface of the DDR5MDB02 device, this timing requirement is applied to all configurations of preamble set by PG[8]RWED and PG[70]RWF5, which is 3 cycle, 4 cycle and more Write preamble, for Write to Write operations as well as normal Write operations. On the DRAM MDQ interface of the DDR5MDB02 device, this timing requirement also applies to all configurations of preamble set by PG[8]RWE1[2:0], which are 1 cycle, 2 cycle(0010 Pattern), 2 cycle (1110 pattern), 3 cycle, and 4 cycle Read preamble, for Read to Read operations as well as normal Read operations.



NOTES:

1. BL = 16, 4tHDQS Preamble
2.  $t_{DQSH\_RX\_pre}$  and  $t_{DQSL\_RX\_pre}$  are shown, and they apply to all toggles during preamble.
3. A second preamble during Write-to-Write operation will follow same requirement.

**Figure 100 — DQS Timing for Input Preamble during Write Operations**



NOTES:

1. BL = 16, 4tBCK Preamble, 1.5tBCK Toggling Postamble.
2.  $t_{MDQSH\_RX\_pre}$  and  $t_{MDQSL\_RX\_pre}$  are shown, and they apply to all toggles during preamble.
3. A second preamble during Read-to-Read operation will follow same requirement.

**Figure 101 — MDQS Timing for Input Preamble during Read Operations**

### 12.3.1 RX Preamble and Postamble Timings (cont'd)

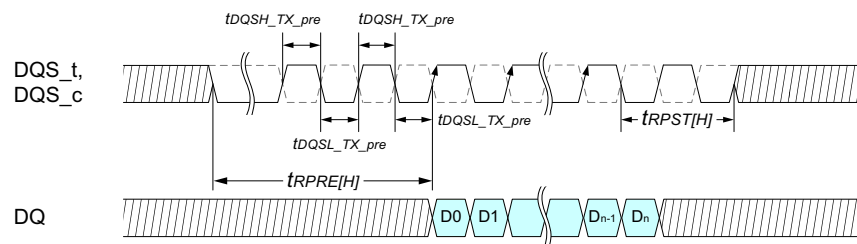
**Table 250 — Input Strobe Preamble and Postamble Timing Parameters**

Symbol	Parameter	DDR5-3200 to 12800		
		Min	Max	Unit <sup>1</sup>
$t_{DQSL\_RX\_pre}$	Strobe's window of differentially LOW during Input preamble	0.43	0.57	tHDQS
$t_{DQSH\_RX\_pre}$	Strobe's window of differentially HIGH during Input preamble	0.43	0.57	tHDQS
$t_{WPREH3}$	Duration of DQS input Preamble (3 tHDQS Preamble)	2.7	-	tHDQS
$t_{WPREH4}$	Duration of DQS input Preamble (4 tHDQS Preamble)	3.6	-	tHDQS
$t_{WPREH5}$	Duration of DQS input Preamble (5 tHDQS Preamble)	4.5	-	tHDQS
$t_{WPREH6}$	Duration of DQS input Preamble (6 tHDQS Preamble)	5.4	-	tHDQS
$t_{WPREH7}$	Duration of DQS input Preamble (7 tHDQS Preamble)	6.3	-	tHDQS
$t_{MDQSL\_RX\_pre}$	Strobe's window of differentially LOW during Input preamble	0.43	0.57	tBCK
$t_{MDQSH\_RX\_pre}$	Strobe's window of differentially HIGH during Input preamble	0.43	0.57	tBCK
$t_{RPRED2}$	Duration of MDQS input Preamble (2 tBCK Preamble)	1.8	-	tBCK
$t_{RPRED3}$	Duration of MDQS input Preamble (3 tBCK Preamble)	2.7	-	tBCK
$t_{RPRED4}$	Duration of MDQS input Preamble (4 tBCK Preamble)	3.6	-	tBCK
$t_{WPSTH0.5}$	Duration of DQS Input postamble (0.5 tHDQS Postamble)	0.45	-	tHDQS
$t_{WPSTH1.5}$	Duration of DQS Input postamble (1.5 tHDQS Postamble)	1.2	-	tHDQS
$t_{MDQSL\_RX\_post}$	Strobe's window of differentially LOW during Input postamble	0.43	0.57	tBCK
$t_{MDQSH\_RX\_post}$	Strobe's window of differentially HIGH during Input postamble	0.43	0.57	tBCK
$t_{RPSTD0.5}$	Duration of MDQS Input postamble (0.5 tBCK Postamble)	0.45	-	tBCK
$t_{RPSTD1.5}$	Duration of MDQS Input postamble (1.5 tBCK Postamble)	1.2	-	tBCK

NOTE 1 Host UI = tHDQS(avg)min/2, DRAM UI = tBCK(avg)min/2, DQS is up to DDR5-12800, and MDQS is up to DDR5-6400.

### 12.3.2 TX Preamble and Postamble Timings

During Write and Read operations, the transmitted output strobe will meet timing requirements ( $t_{DQSH\_TX\_pre}$ ,  $t_{DQSL\_TX\_pre}$ ) to guarantee enough timing margin by setting the window for strobe during the preamble time frame. On the Host DQ interface of the DDR5MDB02 device, this timing requirement is applied to all configurations of preamble set by PG[8]RWED and PG[70]RWF4, which are 3 cycle, 4 cycle and more Read preamble, for Read to Read operations as well as normal Read operations. On the DRAM MDQ interface of the DDR5MDB02 device, this timing requirement also applies to all configurations of preamble set by PG[8]RWE1[4:3], which is 2 cycle, 3 cycle, and 4 cycle Write preamble, for Write to Write operations as well as normal Write operations.

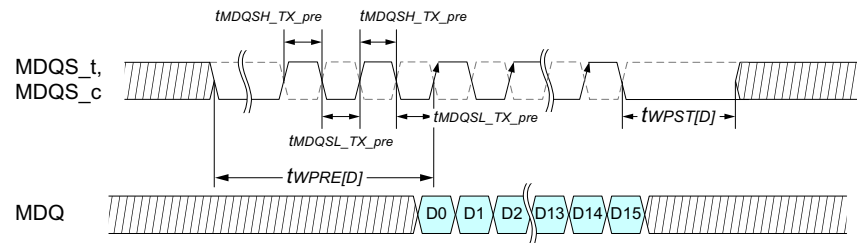


NOTES:

1. BL = 16, 4tHDQS Preamble
2.  $t_{DQSH\_TX\_pre}$  and  $t_{DQSL\_TX\_pre}$  are shown, and they apply to all toggles during preamble.
3. A second preamble during Read-to-Read operation will follow same requirement.

**Figure 102 — DQS Timing for Output Preamble during Read Operations**

### 12.3.2 TX Preamble and Postamble Timings (cont'd)



#### NOTES:

1. BL = 16, 4tBCK Preamble
2. tMDQSH\_TX\_pre and tMDQSL\_TX\_pre are shown, and they apply to all toggles during preamble.
3. A second preamble during Write-to-Write operation will follow same requirement.

**Figure 103 — MDQS Timing for Output Preamble during Write Operations**

**Table 251 — Output Strobe Preamble and Postamble Timing Parameters**

Symbol	Parameter	DDR5-3200 to 12800		Unit <sup>1</sup>
		Min	Max	
t <sub>DQSL_TX_pre</sub>	Strobe's window of differentially LOW during Output preamble	0.45	0.55	tHDQS
t <sub>DQSH_TX_pre</sub>	Strobe's window of differentially HIGH during Output preamble	0.45	0.55	tHDQS
t <sub>RPREH3</sub>	Duration of DQS output Preamble (3 tHDQS Preamble)	2.7	-	tHDQS
t <sub>RPREH4</sub>	Duration of DQS output Preamble (4 tHDQS Preamble)	3.6	-	tHDQS
t <sub>RPREH5</sub>	Duration of DQS output Preamble (5 tHDQS Preamble)	4.5	-	tHDQS
t <sub>RPREH6</sub>	Duration of DQS output Preamble (6 tHDQS Preamble)	5.4	-	tHDQS
t <sub>RPREH7</sub>	Duration of DQS output Preamble (7 tHDQS Preamble)	6.3	-	tHDQS
t <sub>RPREH8</sub>	Duration of DQS output Preamble (8 tHDQS Preamble)	7.2	-	tHDQS
t <sub>MDQSL_TX_pre</sub>	Strobe's window of differentially LOW during Output preamble	0.45	0.55	tBCK
t <sub>MDQSH_TX_pre</sub>	Strobe's window of differentially HIGH during Output preamble	0.45	0.55	tBCK
t <sub>WPRED2</sub>	Duration of MDQS output Preamble (2 tBCK Preamble)	1.8	-	tBCK
t <sub>WPRED3</sub>	Duration of MDQS output Preamble (3 tBCK Preamble)	2.7	-	tBCK
t <sub>WPRED4</sub>	Duration of MDQS output Preamble (4 tBCK Preamble)	3.6	-	tBCK
t <sub>DQSL_TX_post</sub>	Strobe's window of differentially LOW during Output 1.5 tHDQS Toggling postamble	0.45	0.55	tHDQS
t <sub>DQSH_TX_post</sub>	Strobe's window of differentially HIGH during Output 1.5 tHDQS Toggling postamble	0.45	0.55	tHDQS
t <sub>RPSTH0.5</sub>	Duration of DQS output Postamble (0.5 tHDQS Postamble)	0.45	-	tHDQS
t <sub>RPSTH1.5</sub>	Duration of DQS output Postamble (1.5 tHDQS Postamble)	1.2	-	tHDQS
t <sub>WPSTD0.5</sub>	Duration of MDQS output postamble (0.5 tBCK postamble)	0.45	-	tBCK
t <sub>WPSTD1.5</sub>	Duration of MDQS output postamble (1.5 tBCK postamble)	1.2	-	tBCK

NOTE 1 Host UI = tHDQS(avg)min/2, DRAM UI = tBCK(avg)min/2, DQS is up to DDR5-12800, and MDQS is up to DDR5-6400.



## 13 Electrical - Absolute Maximum Ratings

### 13.1 Absolute Maximum Ratings

**Table 252 — Absolute Maximum Ratings over Operating Free-air Temperature Range**

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
$V_{DD}$	Supply voltage		- 0.3	1.4	V	1
$V_{IN}$	Receiver input voltage	See Note 2 and 3	- 0.3	$V_{DD} + 0.5$	V	1, 2, 3
$V_{OUT}$	Driver output voltage	See Note 2 and 3	- 0.3	$V_{DD} + 0.5$	V	1, 2, 3
$I_{IK}$	Input clamp current	$V_{IN} < 0$ or $V_{IN} > V_{DD}$	-	-50	mA	1
$I_{OK}$	Output clamp current	$V_{OUT} < 0$ or $V_{OUT} > V_{DD}$	-	$\pm 50$	mA	1
$I_{OUT}$	Continuous output current	$0 < V_{OUT} < V_{DD}$	-	$\pm 50$	mA	1
$I_{CCC}$	Continuous current through each $V_{DD}$ or $V_{SS}$ pin		-	$\pm 100$	mA	1
$T_{stg}$	Storage temperature		- 55	+ 100	°C	1

NOTE 1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 3 This value is limited to 1.4 V maximum.

### 13.2 Operating Electrical Characteristics

The DDR5MDB02 parametric values are specified for the device default control word settings, unless otherwise stated.

**Table 253 — Operating Electrical Characteristics**

Symbol	Parameter	Condition	Min	Nom	Max	Unit	Notes
$V_{DD}$	DC Supply voltage	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V	
$T_j$	Junction temperature		0	-	125	°C	
$T_{case}$	Case temperature	Measurement procedure JESD51-2	0	-	103	°C	

NOTE 1 DC bandwidth limited to 20 MHz.

NOTE 2 For operation beyond  $T_j$  min and max datasheet values are not guaranteed and may de-rate. For operation above  $T_j$  max lifetime could be affected. All parametric measurements are performed at 0 °C, 25 °C, and 95 °C.

NOTE 3 This spec is meant to guarantee a  $T_j$  of 125 °C by the DDR5MDB02. Since  $T_j$  cannot be measured or observed by users,  $T_{case}$  is specified instead. Under all thermal condition, the  $T_j$  of a DDR5MDB02 shall not be higher than 125 °C.

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## 14 AC and DC Global Definitions

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### 14.1 Transmitter (Tx), Receiver (Rx) and Channel Definitions

**Transmitter (Tx):** Input to the transmitter is the data from the logical portion of the MDB Core and output is at the package pins. The normal components contained in the transmitter are, but not limited to, the pre-driver and the output driver with the transmitter package. The DDR5 MDB uses a differential forwarded strobe-source synchronous system, and single-ended data. The transmitter for a forwarded-strobe-based source synchronous system must include specification and test methodology for low and high frequency random and deterministic jitter and duty cycle error and must consider Bounded Uncorrelated Jitter (BUJ), Duty cycle error etc. For single ended signaling cases, crosstalk and Simultaneous switching noise often impact the measurement of the Transmitter. Therefore, the Transmitter's decimated jitter component parameters and the BER must be specified.

**Receiver (Rx):** The normal components contained in the strobe receiver are: (1) receiver package, (2) input amplifier (to receive the strobe), and (3) optionally, a DLL and time adjustment circuitry, although these are typically not present in the DRAM or the MDB, and distribution circuitry to distribute the strobe to all the receivers. The data input receives the single ended data and measures it against a reference voltage. The difference between the received signal and reference voltage is then sampled. However, the link may need some form of receiver equalization at the speeds that the DDR5 link needs to operate. Since there may not be input eye margin at the receiver pin, the receiver equalization specification may be defined based on a virtual receive sampler/slicer. This means that components of the receiver, which have nothing to do with inter symbol interference (ISI), will have to be specified in such a way as to avoid the impact of ISI. Hence items like receiver jitter, receiver jitter sensitivity, receiver amplitude sensitivity, which are typically orthogonal to ISI, will have to be specified in an ISI free environment. Either the infrastructure, or the test methodology will ensure that the correct amount of ISI, or no ISI, as the case might be, for that specific Rx parameter is used. The validation of the receiver is also dependent on either loopback of data being enabled or restricting to receiver testing to be dependent on a pre-specified set of patterns and the accompanying pattern checker and error counters. The Receiver equalization will be evaluated in the presence of a set of pre-specified receiver testing golden channels. These receiver testing golden channels will attempt to span the ISI range to which the receiver needs to be designed. The key measurement parameter in this test is the stressed eye and the receiver's error sensitivity to the stressed eye. The requirements for these test features are described in APPENDIX - Clock, DQS and DQ Validation Methodology.

**Channel:** The channel is defined from the transmitter package pin to the receiver package pin and includes all the interconnect topology components included in the channel definition (connectors, sockets, and so on). However, this spec will not specify system platform level channel models and it will restrict itself to specifying the Golden Reference Transmitter and Receiver evaluation channels.

## 14.2 Bit Error Rate Introduction

This section provides an overview of the Bit Error Rate (BER) and the desired Statistical Level of Confidence.

### 14.2.1 General Equation

$$n = \left( \frac{1}{BER} \right) \left[ -\ln(1 - SLC) + \ln \left( \sum_{k=0}^N \frac{(n \cdot BER)^k}{k!} \right) \right]$$

Where:

$n$  = number of bits in a trial

$SLC$  = statistical level of confidence

$BER$  = Bit Error Rate

$k$  = intermediate number of specific errors found in trial

$N$  = number of errors recorded during trial

If no errors are assumed in a given test period, the second term drops out and the equation becomes:

$$n = \left( \frac{1}{BER} \right) [-\ln(1 - SLC)]$$

Testing to 99.5% confidence levels is recommended. However, one may choose a number that is viable for their own manufacturing levels. To determine how many bits of data should be sent (again, assuming zero errors, or  $N=0$ ), using  $BER=10^{-9}$  and confidence level  $SLC=99.5\%$ , the result is  $n=(1/BER)(-\ln(1-0.995)) = 5.298 \times 10^9$ .

Results for commonly used confidence levels of 99.5% down to 70% are shown in Table 254.

**Table 254 — Estimated Number of Transmitted Bits (n) for Confidence Level of 70% to 99.5%**

Number of Error	$n = \ln(1 - SLC)/BER$							
	99.5%	99%	95%	90%	85%	80%	75%	70%
0	5.298/BER	4.61/BER	2.99/BER	2.3/BER	1.90/BER	1.61/BER	1.39/BER	1.20/BER

### 14.2.2 Minimum Bit Error Rate (BER) Requirements

Table specifies the  $UI_{AVG}$  and Bit Error Rate requirements over which certain receiver timing and voltage specifications need to be validated assuming a 99.5% confidence level at  $BER = E^{-9}$ .

**Table 255 — Minimum BER Requirements for RX Timing and Voltage Tests**

Symbol	Parameter	DDR5-3200 - 12800			Unit	NOTE
		Min	Nom	Max		
$UI_{AVG}$	Average UI	0.999* nominal	1.000/f	1.001* nominal	ps	1
$N_{MIN\_UI\_Validation}$	Number of UI (min)	$5.3 \times 10^9$		-	UI	2
$BER_{Lane}$	Bit Error Rate	-		$E^{-16}$	Events	3, 4, 5, 6
<p>NOTE 1 Average UI size, “f” is data rate.</p> <p>NOTE 2 # of UI over which certain Rx/Tx timing and voltage specifications need to be validated assuming a 99.5% confidence level at <math>BER = E^{-9}</math>.</p> <p>NOTE 3 This is a system parameter. It is the raw bit error rate for every lane before any logical PHY or link-layer-based correction. It may not be possible to have a validation methodology for this parameter for a standalone transmitter or standalone receiver; therefore, this parameter must be validated in selected systems using a suitable methodology as deemed by the platform.</p> <p>NOTE 4 Bit Error Rate per lane. This is a raw bit error rate before any correction. This parameter is primarily used to determine electrical margins during electrical analysis and measurements that are located between two interconnected devices.</p> <p>NOTE 5 This is the minimum BER requirements for testing timing and voltage parameters listed in Input Clock Jitter, Rx DQ/MDQ Voltage Sensitivity, Rx Clock Jitter Sensitivity, Rx DQ/MDQ Stressed Eye, Tx DQ/MDQ Jitter, and Tx DQ/MDQ Stressed EH/EW specifications.</p> <p>NOTE 6 The BER for DDR5 during normal operation is <math>E^{-16}</math>. For validation purposes, the BER used is <math>E^{-9}</math>.</p>						

### 14.2.3 Unit Interval and Jitter Definitions

This standard describes the UI and NUI Jitter definitions associated with the Jitter parameters specified in Rx Stressed Eye, Tx DQS Jitter, Tx DQ Jitter and Input Clock Jitter specifications.

### 14.2.4 Unit Interval

The times at which the differential crossing points of the clock occur are defined at  $t_1, t_2, \dots, t_{n-1}, t_n, \dots, t_K$ .

The UI at index “n” is defined as shown in Figure 104 (with  $n = 1, 2, \dots$ ) from an arbitrary time in steady state, where  $n = 0$  is chosen as the starting crossing point.

Mathematical definition of UI is shown in Figure 104 and Figure 105.

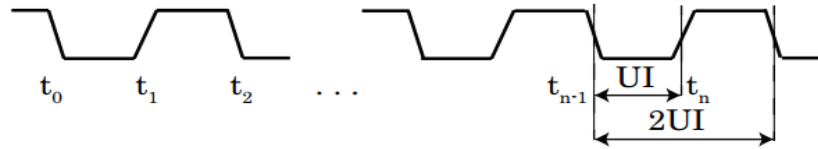
$$UI_n = t_n - t_{n-1}$$

**Figure 104 — UI Definition in Terms of Adjacent Edge Timings**

For the Single-Ended data, the unit interval time starts when the signal crosses a pre-specified reference voltage. For the differential clock, the unit interval time starts when the BCK\_t and BCK\_c intersect (see Figure 105).

#### 14.2.4 Unit Interval (cont'd)

UI Jitter Definition:



**Figure 105 — UI definition Using Clock Waveforms**

If a number of UI edges are computed or measured at times  $t_1, t_2, \dots, t_{n-1}, t_n, \dots, t_K$ , where  $K$  is the maximum number of samples, then the UI jitter at any instance “ $n$ ” is defined in Figure 106, where  $T$  = the ideal UI size.

$$UI_{(jit)n} = (t_n - t_{n-1}) - T; n = 1, 2, 3, \dots, K$$

**Figure 106 — UI Jitter of the “nth” UI Definition (in Terms of Ideal UI)**

In a large sample with random Gaussian-like jitter (therefore, very close to symmetric distribution), the average of all UI sizes usually turns out to be very close to the ideal UI size.

The equation described in Figure 106 assumes starting from an instant of steady state, where  $n=0$  is chosen as the starting point. 1 UI = one bit, which means 2 UI = one full cycle or time period of the forwarded strobe. Example: For 6.4 GT/s signaling, the forwarded strobe frequency is 3.2 GHz, or 1 UI = 156.25 ps.

Deterministic jitter is analyzed in terms of the peak-to-peak value and in terms of specific frequency components present in the jitter, isolating the causes for each frequency. Random jitter is unbounded and analyzed in terms of statistical distribution to convert to a bit error rate (*BER*) for the link.

#### 14.2.5 UI-UI Jitter Definition

UI-UI (read as “UI to UI”) jitter is defined to be the jitter between two consecutive UI as shown in Figure 107.

$$UI_n = UI_n - UI_{n-1}; n = 2, 3, \dots, K$$

**Figure 107 — UI - UI Jitter Definitions**

### 14.2.6 Accumulated Jitter (Over “N” UI)

Accumulated jitter is defined as the jitter accumulated over any consecutive “N” UI as shown in Figure 108.

$$T_{\text{acc}}^N = \sum_{p=m}^{m+N-1} (UI_p - \overline{UI}), \text{ where } m = 1, 2, \dots, K-N$$

**Figure 108 — Definition of Accumulated Jitter (over “N” UI)**

where UI is defined in the equation shown in Figure 109.

$$\overline{UI} = \frac{\sum_{p=1}^K UI_p}{K}, \text{ where } p = 1, 2, \dots, N, \dots, K$$

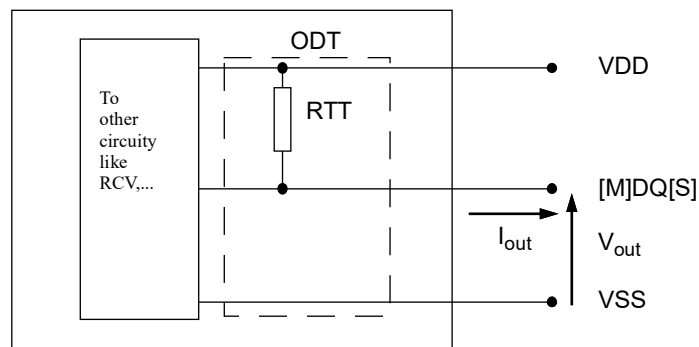
**Figure 109 — Definition of UI**

## 15 Rx Input Specification

### 15.1 [M]DQ/[M]DQS On Die Termination DC Electrical Characteristics

A functional representation of the on-die termination is shown in Figure 110.

$$R_{TT} = \frac{V_{DD} - V_{OUT}}{|I_{OUT}|}$$



**Figure 110 — On Die Termination**

On Die Termination effective R<sub>tt</sub> values supported are 240, 120, 80, 60, 48, 40, and 34 ohms (in addition to R<sub>TT\_OFF</sub>).

### 15.1 [M]DQ/[M]DQS On Die Termination DC Electrical Characteristics (cont'd)

The values in Table 256 are valid for the entire operating temperature range after proper ZQ calibration and assume  $R_{ZQ} = 240\ \Omega \pm 1\%$ .

**Table 256 — ODT Electrical Characteristics  $R_{ZQ}=240\ \Omega \pm 1\%$  Entire Temperature Operation Range; after Proper ZQ Calibration**

RTT	Vout	Min	Nom	Max	Unit	NOTE
240 $\Omega$	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/1	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/1	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/1	1,2
120 $\Omega$	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/2	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/2	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/2	1,2
80 $\Omega$	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/3	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/3	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/3	1,2
60 $\Omega$	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/4	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/4	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/4	1,2
48 $\Omega$	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/5	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/5	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/5	1,2
40 $\Omega$	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/6	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/6	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/6	1,2
34 $\Omega$	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/7	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/7	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/7	1,2
[M]DQ-[M]DQ Mismatch Within Device	VOMdc = 0.8 * VDD	0	-	8	%	1,2,3,4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see Clause 16.5.

NOTE 2 Pull-up ODT resistors are recommended to be calibrated at 0.8 \* VDD. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.5 \* VDD and 0.95 \* VDD.

NOTE 3 [M]DQ to [M]DQ mismatch within device variation for a given component including [M]DQS\_t and [M]DQS\_c (characterized).

NOTE 4 RTT variance range ratio to RTT nominal value in a given component, including [M]DQS\_t and [M]DQS\_c.

$$\text{DQ-DQ Mismatch in a Device} = \frac{RTT_{MAX} - RTT_{MIN}}{RTT_{NOM}} \times 100$$

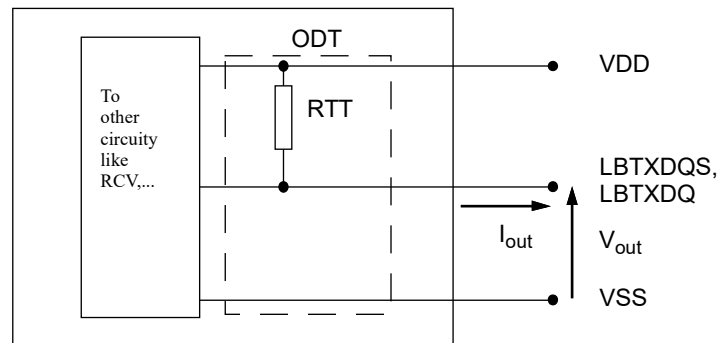


## 15.2 LBTXDQ/LBTXDQS On Die Termination DC Electrical Characteristics

The DDR5MDB02 device includes On-Die Termination resistance for the Loopback signals LBTXDQS and LBTXDQ. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to turn on and off termination resistance for any target DDR5MDB02 devices via Control Word setting.

A functional representation of the on-die termination is shown in Figure 111.

$$R_{TT} = \frac{V_{DD} - V_{OUT}}{|I_{OUT}|}$$



**Figure 111 — Functional Representation of Loopback On Die Termination**

DDR5MDB02 supports an effective Rtt On Die Termination value of 48 ohms (in addition to RTT\_OFF) for Loopback signals.

The values in Table 257 are valid for the entire operating temperature range after proper ZQ calibration and assume RZQ = 240 Ω +/- 1%.

**Table 257 — Loopback ODT Electrical Characteristics RZQ=240Ω +/-1% Entire Temperature Operation Range; after Proper ZQ Calibration**

RTT	Vout	Min	Nom	Max	Unit	NOTE
48Ω	VOLdc= 0.5 * VDD	0.9	1	1.25	RZQ/5	1,2
	VOMdc= 0.8 * VDD	0.9	1	1.1	RZQ/5	1,2
	VOHdc= 0.95 * VDD	0.8	1	1.1	RZQ/5	1,2
Mismatch LBTXDQS - LBTXDQ Within Device	VOMdc = 0.8 * VDD	0	-	8	%	1,2,3,4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see Clause 16.5.

NOTE 2 Pull-up ODT resistors are recommended to be calibrated at 0.8 \* VDD. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at 0.5 \* VDD and 0.95 \* VDD.

NOTE 3 Loopback ODT mismatch within device variation for a given component including LBTXDQS and LBTXDQ (characterized).

NOTE 4 RTT variance range ratio to RTT nominal value in a given component, including LBTXDQS and LBTXDQ.

$$\text{LBTXDQS-LBTXDQ Mismatch in a Device} = \frac{R_{TT_{MAX}} - R_{TT_{MIN}}}{R_{TT_{NOM}}} \times 100$$

### 15.3 Input CMOS Rail-to-Rail Levels for BRST\_n

Table 258 — CMOS Rail-to-Rail Input Levels for BRST\_n

Symbol	Parameter	Min	Max	Unit	NOTE
VIH(AC)_BRST	AC Input HIGH Voltage	$0.8 * V_{DD}$	$V_{DD}$	V	4
VIH(DC)_BRST	DC Input HIGH Voltage	$0.7 * V_{DD}$	VDD	V	2
VIL(DC)_BRST	DC Input LOW Voltage	VSS	$0.3 * V_{DD}$	V	1
VIL(AC)_BRST	AC Input LOW Voltage	VSS	$0.2 * V_{DD}$	V	5
TR_BRST	Rise Time	-	1	$\mu s$	
tPW_BRST	Minimum BRST_n pulse width	$t_{Strap\_Pulse(min)}$	-	tBCK	3, 6

NOTE 1 After BRST\_n is registered LOW, BRST\_n level shall be maintained below VIL(DC)\_BRST during tPW\_BRST.

NOTE 2 Once BRST\_n is registered HIGH, BRST\_n level must be maintained above VIH(DC)\_BRST.

NOTE 3 This definition is applied only in BCOM Strap Command sequences (see Figure 72).

NOTE 4 Overshoot may occur. It should be limited by the Absolute Maximum DC Ratings.

NOTE 5 Undershoot may occur. It should be limited by Absolute Maximum DC Ratings.

NOTE 6 tPW\_BRST is the minimum LOW pulse width supported by the BRST\_n input buffer based on parameter  $t_{Strap\_Pulse}$  at the maximum operating frequency. See Table 246.

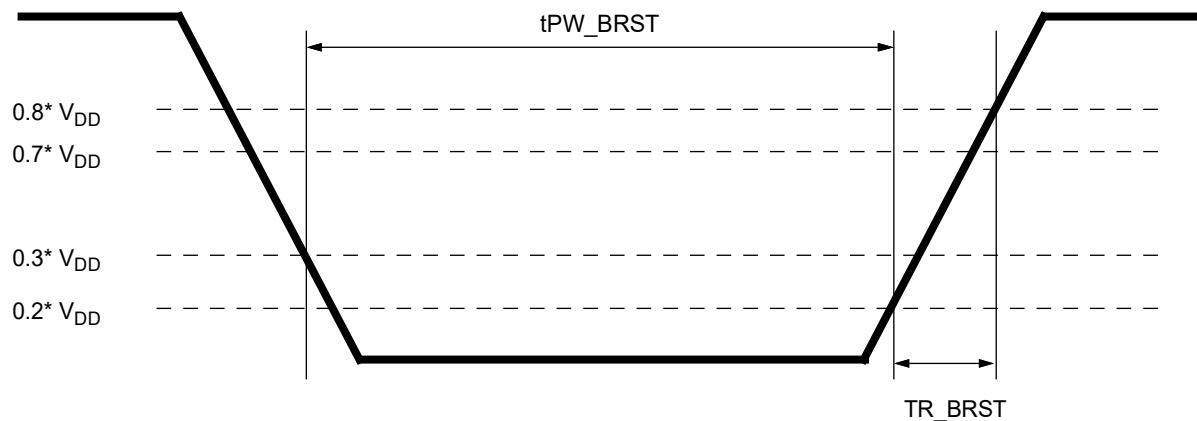


Figure 112 — BRST\_n Input Slew Rate Definition

## 15.4 RX BCOM Input Receiver Specifications

Note: The following draft assumes internal BVref.

The BCS\_n and BCOM input receiver mask for voltage and timing is shown in Figure 113. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DDR5MDB02 input receiver to successfully capture a valid input signal. The mask is a receiver property for each pin, and it is not the valid data eye.

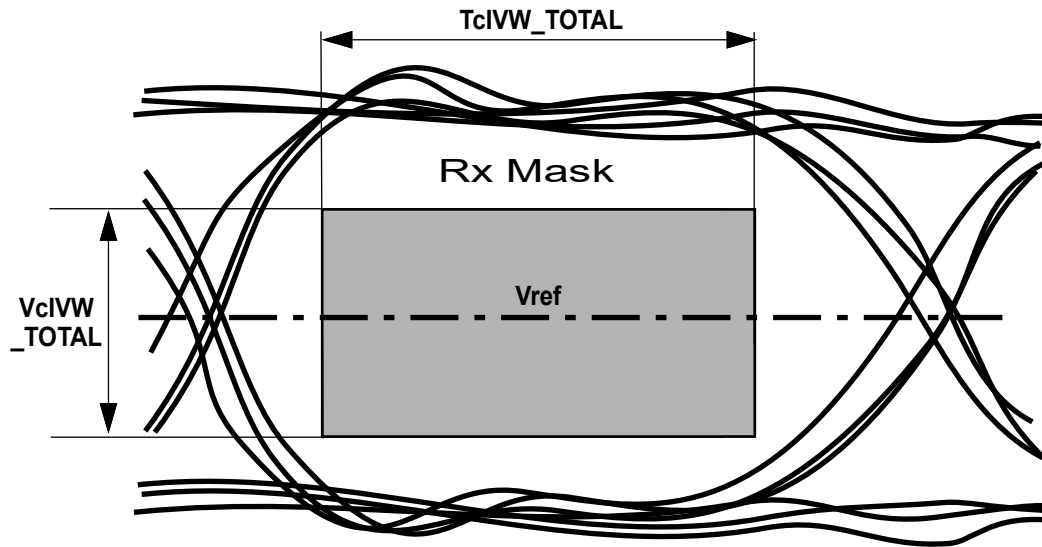


Figure 113 — BCS\_n and BCOM Receiver Mask

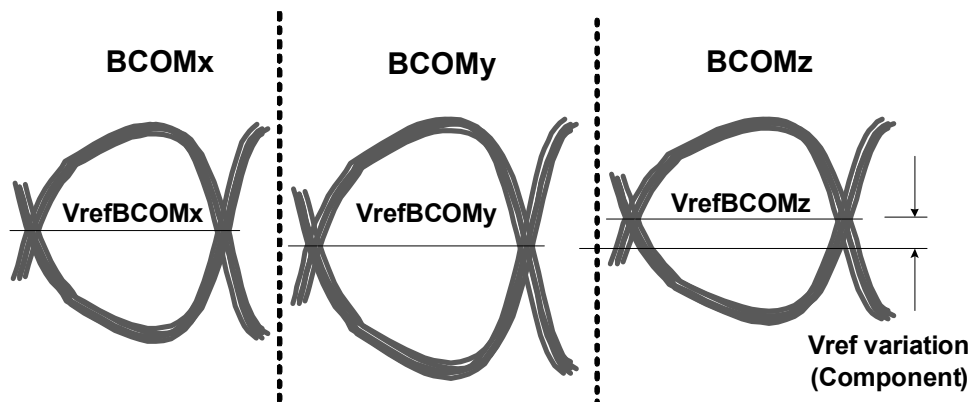
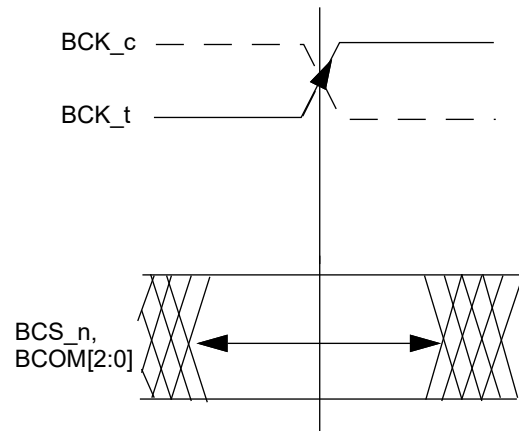


Figure 114 — Across Pin BCOM Voltage Variation

## 15.4 RX BCOM Input Receiver Specifications (cont'd)

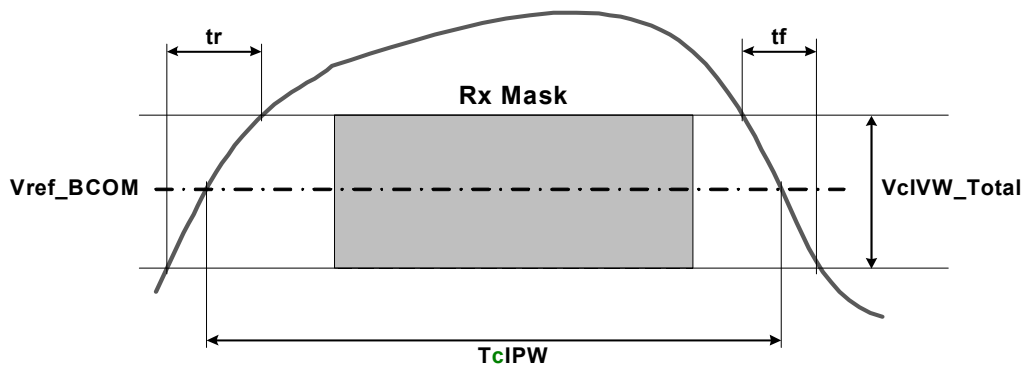
### BCS\_n, BCOM Data-in at MDB Pin

Minimum BCOM Eye center aligned



TcIVW for all BCOM signals is defined as centered on the BCK\_t/BCK\_c crossing at the MDB pin

**Figure 115 — BCOM Timings at the Data Buffer**



NOTE 1  $SRIN\_cIVW = VcIVW\_TOTAL / (tr \text{ or } tf)$

**Figure 116 — BCOM TcIPW and SRIN\_cIVW Definition (for each Input Pulse)**

## 15.4 RX BCOM Input Receiver Specifications (cont'd)

**Table 259 — CTRL RX Receiver Voltage Margin and AC Timing by Speed Bin for DDR5 3200 to 6400**

Speed		DDR5-3200 to 6400		Unit	Note
Symbol	Parameter	Min	Max		
Data Voltage and Timing					
VcIVW_TOTAL	Rx Mask p-p voltage total	-	70	mV	1,2, 3, 4
TcIVW_TOTAL	Rx timing window total	-	0.145	UI	1, 4
TcIPW	CTRL input pulse width	0.36	-	UI	5
tBCK2CTRL	BCK to CTRL offset	-0.1	0.1	UI	6
tCTRLCTRL	CTRL to CTRL offset	-	0.1	UI	7
SRIN_cIVW	Input Slew Rate over VcIVW_TOTAL	1	10	V/ns	8
* UI=tBCK(avg)min					
NOTE 1 CTRL Rx mask voltage and timing total input valid window where VcIVW is centered around BVref. The CTRL Rx mask is applied per bit and includes voltage and temperature drift terms.					
NOTE 2 Rx mask voltage AC swing peak-peak requirement over TcIVW_TOTAL with at least half of VcIVW_TOTAL(max) above BVref and at least half of VcIVW_TOTAL(max) below BVref.					
NOTE 3 The VcIVW voltage levels are centered around BVref.					
NOTE 4 Overshoot and Undershoot should be limited by the Absolute Maximum DC Ratings.					
NOTE 5 CTRL minimum input pulse width defined at the BVref (default value).					
NOTE 6 BCK to CTRL is defined as the input offset for each CTRL input in the DDR5MDB02 device measured at the package balls. Includes all DDR5MDB02 process, voltage and temperature variation.					
NOTE 7 CTRL to CTRL offset is defined as the magnitude of difference between the min and max BCK to CTRL offset at the DDR5MDB02 package balls for a given component. Includes all DDR5MDB02 voltage and temperature variation.					
NOTE 8 Input slew rate over VcIVW Mask centered at BVref. For a given measurement, under the same conditions, the applied slew rate for all transition edges (slowest to fastest) must be within 2 V/ns of each other. This single-ended slew rate also applies to BCK_t and BCK_c.					

## 15.5 RX Spread Spectrum Clocking (SSC) Capability

The system platform uses a reference clock, which is used to synthesize the Data Buffer clock. Spread Spectrum Clock (SSC) with up to – 0.5% down spread in frequency must be supported by the clocking system. The frequency of the reference clock and bit rate can be modulated from 0% to –0.5% of the nominal data rate/frequency, at a modulation rate in the range of 30 kHz to 33 kHz. The modulation profile of SSC must provide optimal or close to optimal EMI reduction. Typical profiles include a triangular profile. The DDR5MDB02 must ensure that it functions normally even in the presence of SSC and truthfully lets SSC related components pass through to its output signals.

15.6 Input Slew Rate for Differential Signals (BCK\_t, BCK\_c, [M]DQS\_t, [M]DQS\_c)

Input slew rate for differential signals BCK\_t/BCK\_c and [M]DQS\_t/[M]DQS\_c are defined and measured as shown in Table 260.

Table 260 — Differential Input Slew Rate Definition for BCK\_t/BCK\_c and [M]DQS\_t/[M]DQS\_c

Symbol	Parameter	Measured		Units	Notes
		Min	Max		
V <sub>IHdiff</sub>	Differential Input HIGH	0.75 * V <sub>DIFFpp</sub>	-	mV	1, 2, 3, 4
V <sub>ILdiff</sub>	Differential input LOW	-	0.25 * V <sub>DIFFpp</sub>	mV	1, 2, 3, 4

- NOTE 1 V<sub>DIFFpp</sub>, V<sub>ILdiff</sub> and V<sub>IHdiff</sub> are defined in Figure 117.
- NOTE 2 V<sub>DIFFpp</sub> is the mean HIGH voltage minus the mean LOW voltage over 1e6 samples.
- NOTE 3 Differential signal rising edge from V<sub>ILdiff</sub> to V<sub>IHdiff</sub> must be monotonic slope.
- NOTE 4 Differential signal falling edge from V<sub>IHdiff</sub> to V<sub>ILdiff</sub> must be monotonic slope.

Table 261 — Differential Input Slew Rate BCK\_t/BCK\_c/[M]DQS\_t/[M]DQS\_c

Symbol	Parameter	Measured		Units	Notes
		Min	Max		
SRIdiff	Differential Input Slew Rate	2	30	V/ns	1

- NOTE 1 All parameters are defined over the entire clock common mode range.

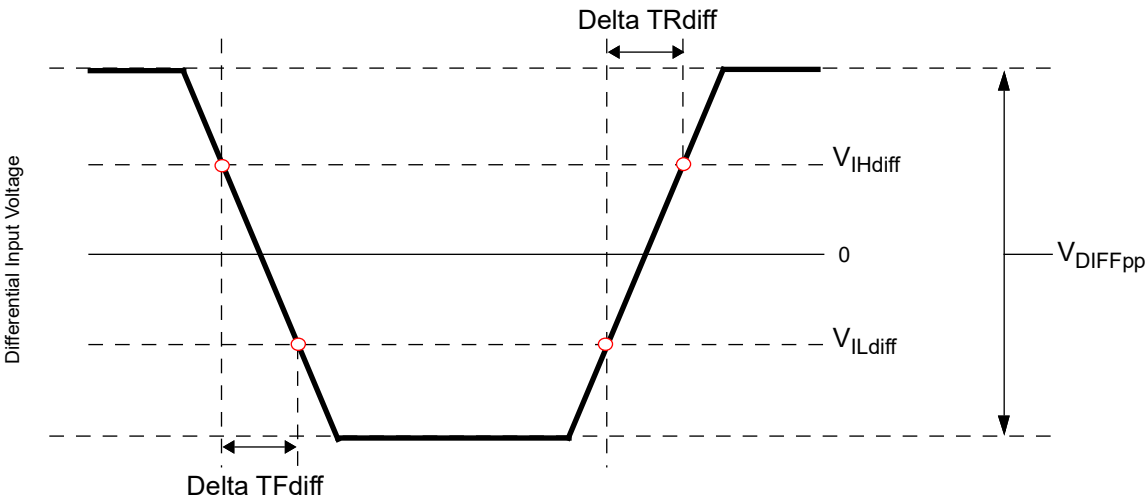


Figure 117 — Differential Input Slew Rate Definition for BCK\_t/BCK\_c and [M]DQS\_t/[M]DQS\_c

## 15.7 Input Differential Cross Point Voltage

To achieve input BCOM[2:0]/BCS\_n requirements as well as output skew parameters with respect to clock, the cross point voltage of differential input clock signals (BCK\_t, BCK\_c) must meet the requirements in Figure 118. The cross point voltage of differential input [M]DQS\_t and [M]DQS\_c must meet the requirements in Figure 118. The differential input cross point voltage VIX (VIX\_FR and VIX\_RF) is measured from the actual cross point of BCK\_t and BCK\_c, or [M]DQS\_t and [M]DQS\_c, relative to the  $V_{\text{swing}}/2$  of the BCK\_t and BCK\_c, or [M]DQS\_t and [M]DQS\_c signals.

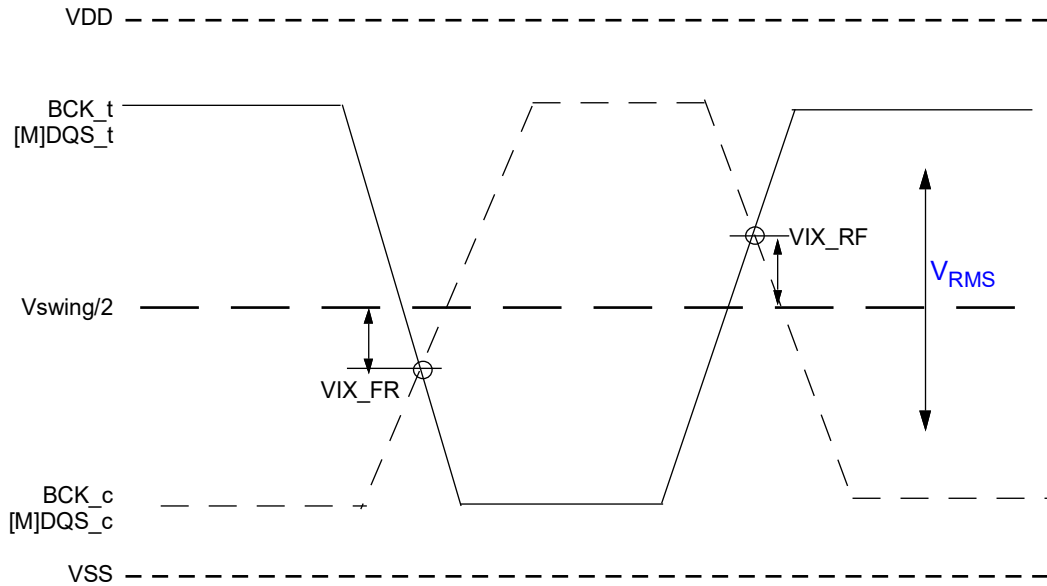


Figure 118 — Vix Definition

Table 262 — Cross Point Voltage (VIX) for Differential Input Signals (BCK)

Symbol	Parameter	DDR5-3200 to 6400		DDR5-3200 to 12800		Unit	NOTE
		Min	Max	Min	Max		
VIX_BCK_Ratio	Clock differential input crosspoint voltage ratio	-	50	N/A	N/A	%	1, 2, 5
VIX_DQS_Ratio	DQS differential input crosspoint voltage ratio	N/A	N/A	-	50	%	3, 4, 5
VIX_MDQS_Ratio	MDQS differential input crosspoint voltage ratio	-	50	N/A	N/A	%	3, 4, 5

NOTE 1 The VIX\_BCK voltage is referenced to  $V_{\text{swing}}/2(\text{mean}) = (\text{BCK}_t \text{ voltage} + \text{BCK}_c \text{ voltage}) / 2$ , where the mean is over 8 UI.

NOTE 2  $\text{VIX\_BCK\_Ratio} = (|\text{VIX\_BCK}| / |V_{\text{RMS}}|) * 100\%$ , where  $V_{\text{RMS}} = \text{RMS}(\text{BCK}_t \text{ voltage} - \text{BCK}_c \text{ voltage})$ .

NOTE 3 The VIX\_[M]DQS voltage is referenced to  $V_{\text{swing}}/2(\text{mean}) = ([\text{M}]DQS_t \text{ voltage} + [\text{M}]DQS_c \text{ voltage}) / 2$ , where the mean is over 8 UI.

NOTE 4  $\text{VIX\_}[M]DQS\_Ratio = (|\text{VIX\_}[M]DQS| / |V_{\text{RMS}}|) * 100\%$ , where  $V_{\text{RMS}} = \text{RMS}([\text{M}]DQS_t \text{ voltage} - [\text{M}]DQS_c \text{ voltage})$ .

NOTE 5 Only applies when both BCK\_t/[M]DQS\_t and BCK\_c/[M]DQS\_c are transitioning.

## 15.8 RX - Receiver Statistical Parameters

### 15.8.1 RX BCK Input Clock Jitter - BCOM Interface

The clock is being driven from the MRCD for MRDIMM modules, Figure 119.

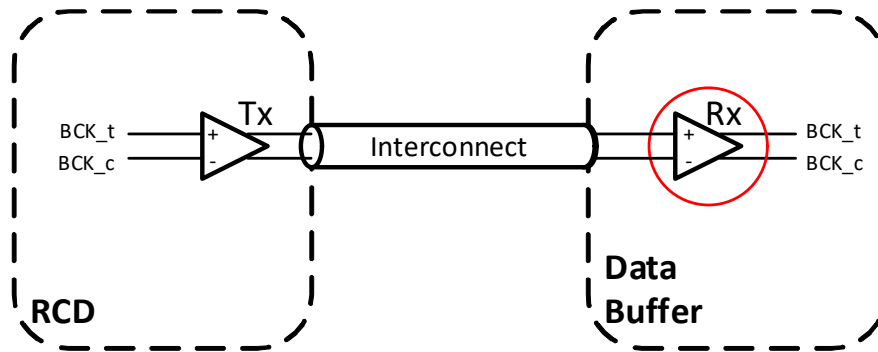


Figure 119 — MRCD Driving Clock Signals to the Data Buffer



### 15.8.1 RX BCK Input Clock Jitter - BCOM Interface (cont'd)

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. Input clock violating the min/max jitter values may result in malfunction of the DDR5MRCD02 device.

**Table 263 — Input Clock BCK Differential Jitter Parameters**

[BUJ=Bounded Uncorrelated Jitter; DCD=Duty Cycle Distortion; Dj=Deterministic Jitter; Rj=Random Jitter; Tj=Total jitter; pp=Peak-to-Peak]

Symbol	Parameter	DDR5-3200 to 6400		Unit	NOTE
		Min	Max		
tBCK	MRCD Reference clock frequency	0.9999*f0	1.0001*f0	MHz	1, 12
tBCK_Duty_UI_Error	Duty Cycle Error	-	0.05	UI	1, 5, 12
tBCK_1UI_Rj_NoBUJ	Rj value of 1-UI Jitter	-	0.0037	UI (RMS)	3, 6, 12, 13
tBCK_1UI_Dj_NoBUJ	Dj pp value of 1-UI Jitter	-	0.03	UI	3, 7, 12, 13
tBCK_1UI_Tj_NoBUJ	Tj value of 1-UI Jitter	-	0.09	UI	3, 7, 12, 13
tBCK_NUI_Rj_NoBUJ	Rj value of N-UI Jitter, where N= 2 - 5	-	0.004	UI (RMS)	3, 8, 12, 13
tBCK_NUI_Dj_NoBUJ	Dj pp value of N-UI Jitter, where N=2 - 5	-	0.074	UI	3, 9, 12, 13
tBCK_NUI_Tj_NoBUJ,	Tj value of N-UI Jitter, where N= 2 - 5	-	0.14	UI	3, 9, 12, 13
*UI=tBCK(avg)min/2					
NOTE 1 f0 = Data Rate/2, example: if data rate is 3200MT/s, then f0=1600.					
NOTE 2 Rise and fall time slopes (V/nsec) are measured between +100 mV and -100 mV of the differential output of reference clock.					
NOTE 3 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or cannot be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being DDR5MDB02 component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining Tx lanes send patterns to the corresponding Rx receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.					
NOTE 4 Duty Cycle defined as the ratio between any even UI and tBCK.					
NOTE 5 Duty Cycle Error defined as absolute difference between average value of all UI with that of average of odd UI, which in magnitude would equal absolute difference between average of all UI and average of all even UI.					
NOTE 6 Rj RMS value of 1-UI jitter without BUJ, but on-die system-like noise present. This extraction is to be done after software correction of DCD.					
NOTE 7 Dj pp value of 1-UI jitter (after software assisted DCC). Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.					
NOTE 8 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 2 < N < 5. This extraction is to be done after software correction of DCD.					
NOTE 9 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 2 < N < 5. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.					
NOTE 10 Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 5 < N < 31. This extraction is to be done after software correction of DCD.					
NOTE 11 Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Evaluated for 5 < N < 31. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.					
NOTE 12 The validation methodology for these parameters will be covered in future ballots.					
NOTE 13 If the clock meets total jitter Tj at BER of 1E-16, then meeting the individual Rj and Dj components of the spec can be considered optional. Tj is defined as Dj + 16.2*Rj for BER of 1E-16.					

### 15.8.2 RX BCK Voltage Sensitivity - BCOM Interface

The differential input clock voltage sensitivity test provides the methodology for testing the receiver's sensitivity to clock by varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter ( $R_j$ ,  $D_j$ , DCD) and crosstalk noise.

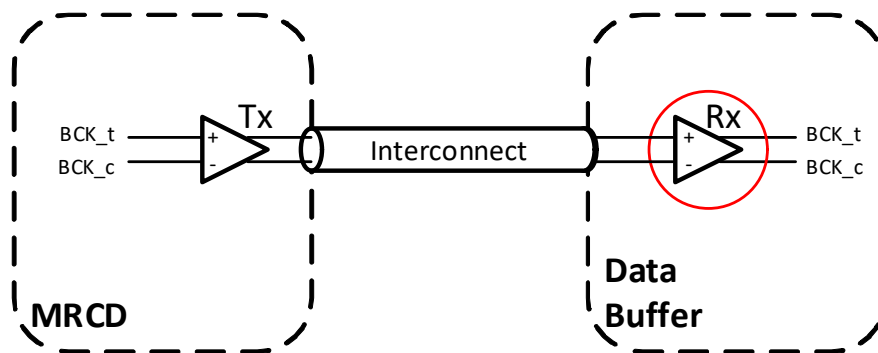


Figure 120 — Example of DDR5 Memory Interconnect

Differential input clock (BCK\_t, BCK\_c) VR<sub>x</sub>\_CK is defined Table 264 and measured as in Figure 121. The clock receiver must pass the minimum BER requirements for DDR5.

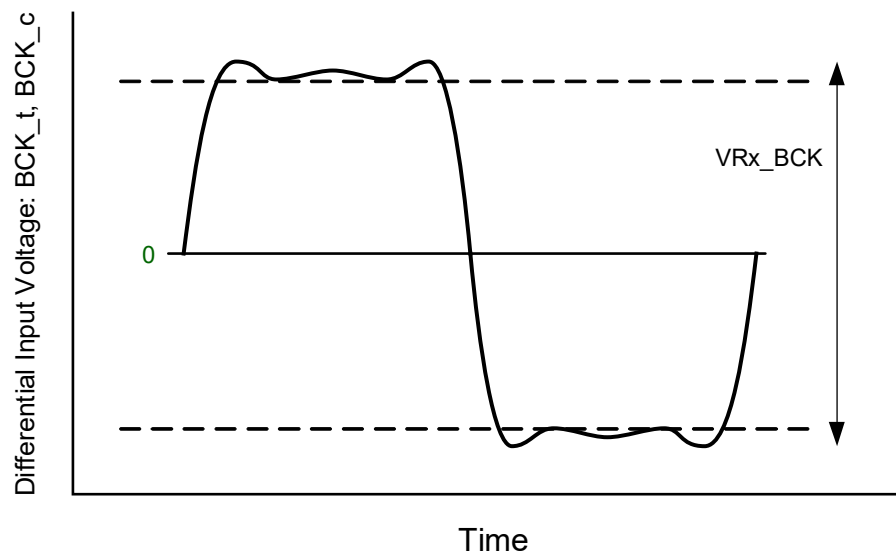


Figure 121 — VR<sub>x</sub>\_BCK

15.8.3 Rx [M]DQS Voltage Sensitivity

The receiver strobe input voltage sensitivity test provides the methodology for testing the receiver’s sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter (Rj, Dj, DCD), and crosstalk noise.

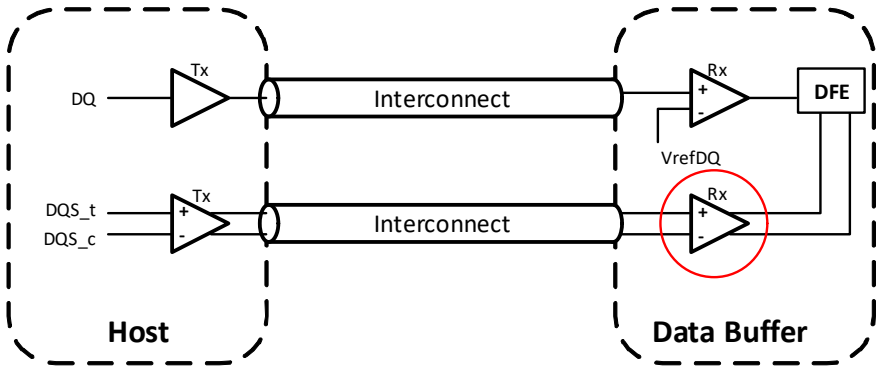


Figure 122 — Data Buffer’s RX Forward Strobe for Jitter Sensitivity Testing

Input differential (DQS\_t, DQS\_c) VRx\_DQS is defined in Table 264 and measured as shown in Figure 123. The receiver must pass the minimum BER requirements for DDR5.

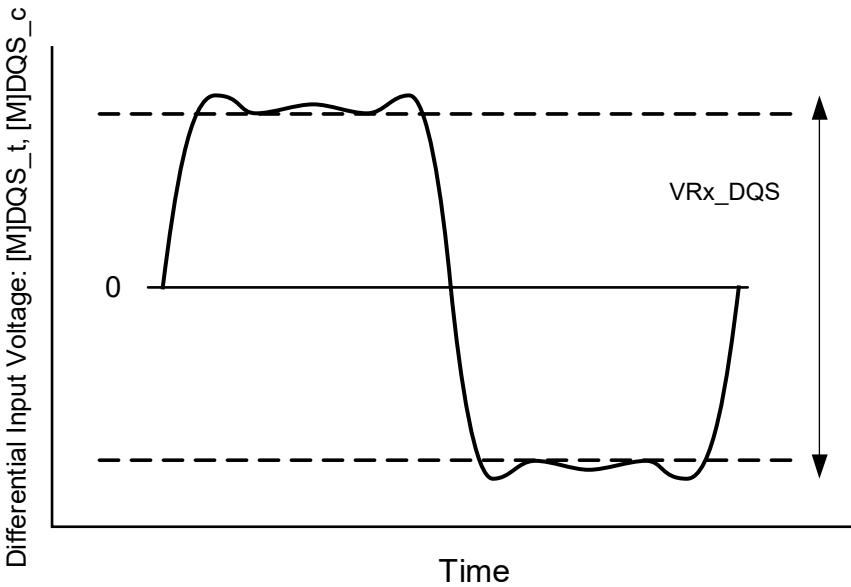


Figure 123 — VRx\_DQS

### 15.8.4 RX [M]DQ Voltage Sensitivity

The receiver data input voltage sensitivity test provides the methodology for testing the receiver's sensitivity to varying input voltage in the absence of Inter-Symbol Interference (ISI), jitter ( $R_j$ ,  $D_j$ , DCD), and crosstalk noise.

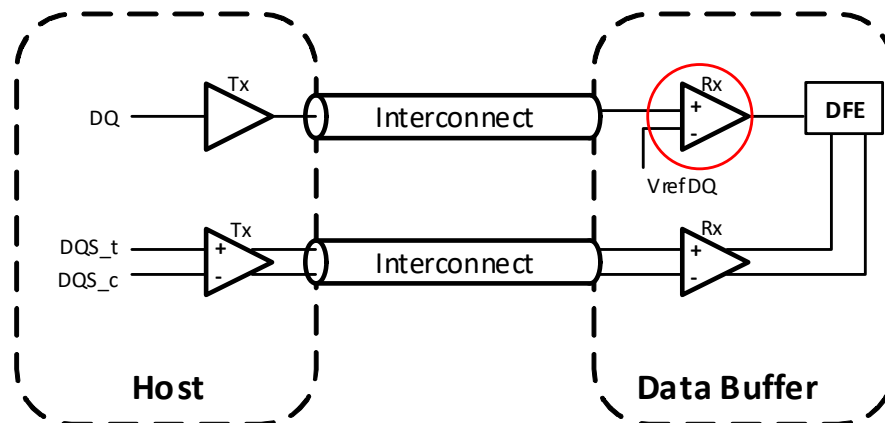


Figure 124 — Example of DDR5 Memory Interconnect

Input differential ( $DQS_t$ ,  $DQS_c$ )  $VRx\_DQ$  is defined in Table 264 and measured as shown in Figure 125. The receiver must pass the minimum BER requirements for DDR5. These parameters are tested with neither additive gain nor Rx Equalization set.

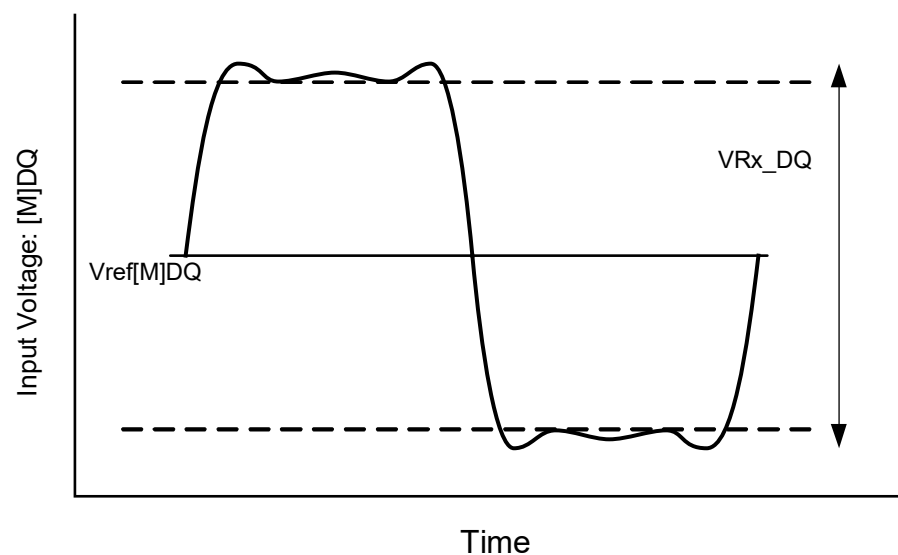


Figure 125 —  $VRx\_DQ$

#### 15.8.4 RX [M]DQ Voltage Sensitivity (cont'd)

**Table 264 — RX Voltage Sensitivity Parameters for DDR5-3200 to 12800**

Symbol	Parameter	DDR5 3200 to 12800		Unit	NOTE
		Min	Max		
VRx_BCK	Minimum input clock voltage sensitivity (differential p-p)	-	80	mV	1, 3, 5
VRx_BCOM	Minimum input BCOM voltage sensitivity (guaranteed by design)	-	55	mV	1,2
VRx_DQS	Minimum DQS Rx input voltage sensitivity (differential p-p)	-	80	mV	1, 2, 3, 5
VRx_DQ	Minimum DQ Rx input voltage sensitivity (p-p around VrefDQ)	-	50	mV	1, 2, 3, 4
VRx_CRC	Minimum DQS1 as CRC Rx input voltage sensitivity (differential p-p)	-	100	mV	
VRx_MDQS	Minimum MDQS Rx input voltage sensitivity (differential p-p)	-	80	mV	1, 2, 3, 5
VRx_MDQ	Minimum MDQ Rx input voltage sensitivity (p-p around VrefDQ)	-	55	mV	1, 2, 3, 4

\*DQ/DQS up to DDR5-12800. MDQ/MDQS/BCK/BCOM/BCS up to DDR5-6400.

NOTE 1 The BER for DDR5 during normal operation is  $E^{-16}$ . For validation purposes, the BER used is  $E^{-9}$ .

NOTE 2 Test using clock-like pattern of repeating 3 “1s” and 3 “0s” without applying cross-talk or SSO conditions.

NOTE 3 This test should be done in typical temperature and voltage conditions (i.e., VDD = 1.1 V, 25 °C).

NOTE 4 This test should be done with default Vref[M]DQ settings.

NOTE 5 The common-mode voltage that provides the best input voltage sensitivity performance can be chosen for this measurement.

#### 15.8.5 RX [M]DQS Input Jitter Sensitivity

The receiver clock jitter sensitivity test provides the methodology for testing the receiver’s strobe sensitivity to an applied duty cycle distortion (DCD) and/or random jitter (Rj) at the forwarded strobe input while keeping the data input jitter free, noise free and ISI free. The receiver must pass the appropriate BER rate when the equivalent crosstalk pattern is applied through the combination of applied DCD and Rj.

Data Buffer’s RX Forward Strobe for Jitter Sensitivity Testing is illustrated in the following figure.

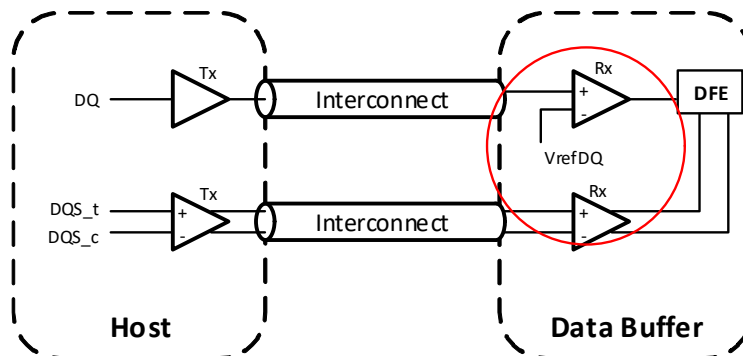


Table 265 provides Rx DQS Jitter Sensitivity Specification for the DDR5MDB02 receivers when operating at various possible transfer rates. These parameters are tested with neither additive gain nor Rx Equalization set.

## 15.8.5 RX [M]DQS Input Jitter Sensitivity (cont'd)

Table 265 — Rx [M]DQS Jitter Sensitivity Specification for DDR5-3200 to 12800

Symbol	Parameter	DDR5-3200 to 12800		Unit	NOTE
		Min	Max		
tRx_DQ_tMargin_Ref	DQ Timing Width target for design and simulation, assuming ideal fixture with no Rj or DCD	0.875	-	Host UI	1, 2, 7, 8, 9
tRx_MDQ_tMargin_Ref	MDQ Timing Width target for design and simulation, assuming ideal fixture with no Rj or DCD	0.875	-	DRAM UI	1, 2, 7, 8, 9
$\Delta$ tRx_DQ_tMargin_Rj_DQS_Ref	Degradation of timing width compared to tRx_DQ_tMargin_Ref, with Rj injection in DQS. Target for design and simulation.	-	0.075	Host UI	1, 4, 7, 8, 9
$\Delta$ tRx_DQ_tMargin_DCD_Rj_DQS_Ref	Degradation of timing width compared to tRx_DQ_tMargin_Ref, with both DCD and Rj injection in DQS. Target for design and simulation.	-	0.125	Host UI	1, 5, 7, 8, 9
$\Delta$ tRx_MDQ_tMargin_Rj_MDQS_Ref	Degradation of timing width compared to tRx_MDQ_tMargin_Ref, with Rj injection in MDQS. Target for design and simulation.	-	0.075	DRAM UI	1, 4, 7, 8, 9
$\Delta$ tRx_MDQ_tMargin_DCD_Rj_MDQS_Ref	Degradation of timing width compared to tRx_MDQ_tMargin_Ref, with both DCD and Rj injection in MDQS. Target for design and simulation.	-	0.125	DRAM UI	1, 5, 7, 8, 9
tRx_DQ_tMargin_Rj_DQS	DQ Timing Width with Rj injection in DQS	0.8	-	Host UI	1, 2, 7, 8, 9
tRx_MDQ_tMargin_Rj_MDQS	MDQ Timing Width with Rj injection in MDQS	0.8	-	DRAM UI	1, 2, 7, 8, 9
$\Delta$ tRx_DQ_tMargin_DCD_DQS	Degradation of timing width compared to tRx_DQ_tMargin_Rj_DQS, with DCD injection in DQS.	-	0.05	Host UI	1, 3, 7, 8, 9
$\Delta$ tRx_MDQ_tMargin_DCD_MDQS	Degradation of timing width compared to tRx_MDQ_tMargin_Rj_MDQS, with DCD injection in MDQS.	-	0.05	DRAM UI	1, 3, 7, 8, 9
tRx_DQS2DQ_Skew	Delay of any data lane relative to the DQS_t/DQS_c crossing	0	3	Host UI	1, 6, 7, 8, 9
tRx_DQ2DQ	Delay between any different data lanes within the same nibble in x4 mode or the same byte in x8 mode	-	50	ps	1, 2, 6, 7, 8, 9
tRx_MDQS2MDQ_Skew	Delay of any data lane relative to the MDQS_t/MDQS_c crossing	Min: 0; Max: 3 for unmatched receivers. Min: -0.1; Max: +0.1 for matched receivers.		DRAM UI	1, 6, 7, 8, 9
tRx_MDQ2MDQ	Delay between any different data lanes within the same nibble in x4 mode or the same byte in x8 mode	-	0.1	DRAM UI	1, 6, 7, 8, 9
*Host UI=tHDQS(avg)min/2. DRAM UI=tBCK(avg)min/2.					
*DQ/DQS up to DDR5-12800. MDQ/MDQS up to DDR5-6400.					
NOTE 1 Validation methodology will be defined in future ballots.					
NOTE 2 Including the DQS1/CRC pin. DQ Timing Width - timing width for any data lane using repetitive patterns (check notes 3 to 5 for the pattern) measured at BER=E-9.					
NOTE 3 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD injection in forwarded strobe [M]DQS compared to tRx_DQ_tMargin, measured at BER=E-9. The magnitude of DCD is specified under Test Conditions for Rx Strobe Jitter Sensitivity Testing5. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.					
NOTE 4 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with only Rj injection in forwarded strobe [M]DQS measured at BER=E-9, compared to tRx_tMargin. The magnitude of Rj is specified under Test Conditions for Rx Strobe Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.					
NOTE 5 Magnitude of degradation of timing width for any data lane using repetitive no ISI patterns with DCD and Rj injection in forwarded strobe [M]DQS measured at BER=E-9, compared to tRx_tMargin. The magnitudes of DCD and Rj are specified under Test Conditions for Rx Strobe Jitter Sensitivity Testing. Test using clock-like pattern of repeating 3 “1s” and 3 “0s”.					
NOTE 6 Delay of any data lane relative to the [M]DQS lane, as measured at the end of Tx+Channel. This parameter is a collective sum of effects of data clock mismatches in Tx and on the medium connecting Tx and Rx.					
NOTE 7 All measurements at BER=E-9.					
NOTE 8 This test should be done in typical temperature and voltage conditions (i.e., V <sub>DD</sub> = 1.1 V, 25 °C) with default Vref[M]DQ settings.					
NOTE 9 The user has the freedom to set the voltage swing and slew rates for strobe and [M]DQ signals as long as they meet the specification.					

### 15.8.6 Test Conditions for RX Strobe Jitter Sensitivity Tests

Table 266 lists the amount of Duty Cycle Distortion (DCD) and/or Random Jitter (Rj) that must be applied to the forwarded clock when measuring the Rx Clock Jitter Sensitivity parameters specified in Table 265.

**Table 266 — RX Strobe Jitter Sensitivity Specification for DDR5-3200 to 12800**

Symbol	Parameter	DDR5-3200 to 12800		Unit	NOTE
		Min	Max		
tRx_DQS_DCD	Applied DCD to the DQS	-	0.045	Host UI	1, 2, 3, 6, 7, 10
tRx_DQS_Rj	Applied Rj RMS to the DQS	-	0.00625	Host UI (RMS)	1, 2, 4, 6, 8, 10
tRx_DQS_DCD_Rj	Applied DCD and Rj RMS to the DQS	-	0.045 UI DCD + 0.00625 UI (RMS) Rj	Host UI	1, 2, 5, 6, 7, 9, 10
tRx_MDQS_DCD	Applied DCD to the MDQS	-	0.045	DRAM UI	1, 2, 3, 6, 7, 10
tRx_MDQS_Rj	Applied Rj RMS to the MDQS	-	0.00625	DRAM UI (RMS)	1, 2, 4, 6, 8, 10
tRx_MDQS_DCD_Rj	Applied DCD and Rj RMS to the MDQS	-	0.045 UI DCD + 0.00625 UI (RMS) Rj	DRAM UI	1, 2, 5, 6, 7, 9, 10
*Host UI=tHDQS(avg)min/2 *DRAM UI=tBCK(avg)min/2 *DQ/DQS up to DDR5-12800. MDQ/MDQS up to DDR5-6400.					
NOTE 1 While imposing this spec, the strobe lane is stressed, but the data input is kept large amplitude and no jitter or ISI injection. The specified voltages are at the Rx input pin. The DQS and DQ input voltage swing and/or slew rate can be adjusted, without exceeding the specifications, for this test.					
NOTE 2 The jitter response of the forwarded strobe channel will depend on the input voltage, primarily due to bandwidth limitations of the clock receiver. For this revision, no separate specification of jitter as a function of input amplitude is specified, instead the response characterization done at the specified clock amplitude only. The specified voltages are at the Rx input pin.					
NOTE 3 Various DCD values should be tested, complying within the maximum limits.					
NOTE 4 Various Rj values should be tested, complying within the maximum limits.					
NOTE 5 Various combinations of DCD and Rj should be tested, complying within the maximum limits. The maximum timing margin degradation as a result of these injected jitter is specified in a separate table.					
NOTE 6 Although DDR5 has bursty traffic, in order to ensure that current available BERTs can be used for this test, a continuous strobe and continuous DQ are used for this parameter. The clock like pattern repeating 3 “1s” and 3 “0s” is used for this test.					
NOTE 7 Duty Cycle Distortion (in UI DCD) as applied to the input forwarded DQS from BERT (UI).					
NOTE 8 RMS value of Rj (specified as Edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).					
NOTE 9 Duty cycle distortion (specified as UI DCD) and rms values of Rj (specified as edge jitter) applied to the input forwarded DQS from BERT (values of the edge jitter RMS values specified as % of UI).					
NOTE 10 The user has the freedom to set the voltage swing and slew rates for strobe and DQ signals as long as they meet the specification.					

### 15.8.7 Rx [M]DQ Stressed Eye

The stressed eye tests provide the methodology for creating the appropriate stress for the Data Buffer's receiver with the combination of ISI (both loss and reflective), jitter (Rj, Dj, DCD), and crosstalk noise. The receiver must pass the appropriate BER rate when the equivalent stressed eye is applied through the combination of ISI, jitter and crosstalk.

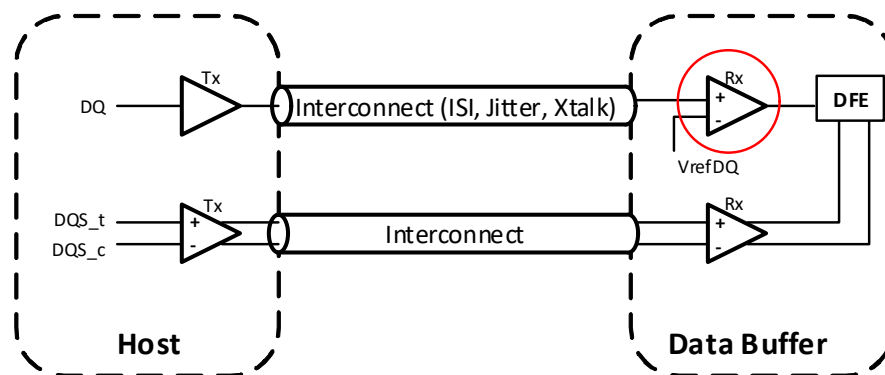


Figure 126 — Example of Rx Stressed Test Setup in the Presence of ISI, Jitter, and Crosstalk

Table 267 — Test Conditions for Rx Stressed Eye Tests

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p=peak to peak]

Symbol	Parameter	DDR5-3200 to 12800		Unit	NOTE
		Min	Max		
RxEH_Stressed_Eye_DQ	Eye height of stressed eye	50	-	mV	1, 2, 3, 4, 5, 6, 7
RxEW_Stressed_Eye_DQ	Eye width of stressed eye	0.15	-	Host UI	1, 2, 3, 4, 5, 6, 7
Vswing_Stressed_Eye_DQ	Vswing stress to meet above data eye	0	600	mV	1, 2
Sj_Stressed_Eye_DQ	Injected sinusoidal jitter at 200 MHz to meet above data eye	0	0.45	Host UI (p-p)	1, 2
Rj_Stressed_Eye_DQ	Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	0	0.2	ps RMS	1, 2
Vnoise_Stressed_Eye_DQ	Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz to meet above data eye	0	125	mV (p-p)	1, 2
RxEH_Stressed_Eye_MDQ	Eye height of stressed eye	55	-	mV	1, 2, 3, 4, 5, 6, 7
RxEW_Stressed_Eye_MDQ	Eye width of stressed eye	0.15	-	DRAM UI	1, 2, 3, 4, 5, 6, 7
Vswing_Stressed_Eye_MDQ	Vswing stress to meet above data eye	0	600	mV	1, 2
Sj_Stressed_Eye_MDQ	Injected sinusoidal jitter at 200 MHz to meet above data eye	0	0.45	DRAM UI (p-p)	1, 2
Rj_Stressed_Eye_MDQ	Injected Random wide band (10 MHz-1 GHz) Jitter to meet above data eye	0	0.2	ps RMS	1, 2



**Table 267 — Test Conditions for Rx Stressed Eye Tests (cont'd)**

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p=peak to peak]

Symbol	Parameter	DDR5-3200 to 12800		Unit	NOTE
		Min	Max		
Vnoise_Stressed_Eye_MDQ	Injected voltage noise as PRBS23, or Injected voltage noise at 2.1 GHz to meet above data eye	0	125	mV (p-p)	1, 2
*Host UI=tHDQS(avg)min/2 *DRAM UI=tBCK(avg)min/2 *DQ/DQS up to DDR5-12800. MDQ/MDQS up to DDR5-6400.  NOTE 1 Must meet 1E-9 BER requirement with eye at receiver after equalization per pin. NOTE 2 These parameters are applied on the reference channel. NOTE 3 Evaluated with no DC supply voltage drift. NOTE 4 Evaluated with no temperature drift. NOTE 5 Supply voltage noise limited according to DC bandwidth spec, see Recommended DC Operating Conditions. NOTE 6 The stressed eye is to be assumed to have a diamond shape. NOTE 7 The VrefDQ, VrefMDQ, DFE Gain Bias Step, and DFE Taps 1,2,3,4, 5, 6, 7, 8 Bias Step can be adjusted as needed, without exceeding the specifications, for this test.					

## 15.9 tRX\_DQS2DQ Offset due to Temperature and Voltage Variation

As temperature and voltage change on the MDB die, the DQS clock tree will shift and may require retraining. The tRX\_DQS2DQ offset due to temperature and voltage variation specification can be used for guiding the Host to design and evaluate retraining interval on write data interface.

**Table 268 — tRX\_DQS2DQ Offset due to Temperature and Voltage Variation for DDR5-3200 to 12800**

Symbol	Parameter	DDR5-3200 to 12800		Unit	NOTE
		Min	Max		
tRX_DQS2DQ_temp	DQS to DQ offset temperature variation	-	1.2	ps/10 °C	1,3,4
tRX_DQS2DQ_volt	DQS to DQ offset voltage variation	-	1	ps/50mV	2,3,4
NOTE 1 tRX_DQS2DQ max delay variation as a function of temperature NOTE 2 tRX_DQS2DQ max delay variation as a function of the DC voltage variation for VDD. AC noise impact for frequencies >20MHz and max voltage of 45 mV pk-pk from DC -20 MHz at a fixed temperature on the package. NOTE 3 Absolute value of DQS to DQ offset. NOTE 4 tRX_DQS2DQ is not subject to production test but is a design guideline only and verified by design.					

## 16 TX Output Specifications

### 16.1 [M]DQ/[M]DQS Output Driver DC Electrical Characteristics

The values in Table 269 are valid for the entire operating temperature range after proper ZQ calibration and assume  $R_{ZQ} = 240\ \Omega \pm 1\%$ .

**Table 269 — [M]DQ/[M]DQS Output Driver DC Electrical Characteristics**

RON <sub>NOM</sub>	Resistor	V <sub>OUT</sub>	Min	Nom	Max	Unit	Note
34 Ω	RON <sub>34Pd</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DD</sub>	0.8	1.0	1.1	R <sub>ZQ</sub> /7	1, 2
		V <sub>OMdc</sub> = 0.8 x V <sub>DD</sub>	0.9	1.0	1.1	R <sub>ZQ</sub> /7	1, 2
		V <sub>OHdc</sub> = 0.95 x V <sub>DD</sub>	0.9	1.0	1.25	R <sub>ZQ</sub> /7	1, 2
	RON <sub>34Pu</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DD</sub>	0.9	1.0	1.25	R <sub>ZQ</sub> /7	1, 2
		V <sub>OMdc</sub> = 0.8 x V <sub>DD</sub>	0.9	1.0	1.1	R <sub>ZQ</sub> /7	1, 2
		V <sub>OHdc</sub> = 0.95 x V <sub>DD</sub>	0.8	1.0	1.1	R <sub>ZQ</sub> /7	1, 2
40 Ω	RON <sub>40Pd</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DD</sub>	0.8	1.0	1.1	R <sub>ZQ</sub> /6	1, 2
		V <sub>OMdc</sub> = 0.8 x V <sub>DD</sub>	0.9	1.0	1.1	R <sub>ZQ</sub> /6	1, 2
		V <sub>OHdc</sub> = 0.95 x V <sub>DD</sub>	0.9	1.0	1.25	R <sub>ZQ</sub> /6	1, 2
	RON <sub>40Pu</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DD</sub>	0.9	1.0	1.25	R <sub>ZQ</sub> /6	1, 2
		V <sub>OMdc</sub> = 0.8 x V <sub>DD</sub>	0.9	1.0	1.1	R <sub>ZQ</sub> /6	1, 2
		V <sub>OHdc</sub> = 0.95 x V <sub>DD</sub>	0.8	1.0	1.1	R <sub>ZQ</sub> /6	1, 2
48 Ω	RON <sub>48Pd</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DD</sub>	0.8	1.0	1.1	R <sub>ZQ</sub> /5	1, 2
		V <sub>OMdc</sub> = 0.8 x V <sub>DD</sub>	0.9	1.0	1.1	R <sub>ZQ</sub> /5	1, 2
		V <sub>OHdc</sub> = 0.95 x V <sub>DD</sub>	0.9	1.0	1.25	R <sub>ZQ</sub> /5	1, 2
	RON <sub>48Pu</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DD</sub>	0.9	1.0	1.25	R <sub>ZQ</sub> /5	1, 2
		V <sub>OMdc</sub> = 0.8 x V <sub>DD</sub>	0.9	1.0	1.1	R <sub>ZQ</sub> /5	1, 2
		V <sub>OHdc</sub> = 0.95 x V <sub>DD</sub>	0.8	1.0	1.1	R <sub>ZQ</sub> /5	1, 2
60 Ω	RON <sub>60Pd</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DD</sub>	0.8	1.0	1.1	R <sub>ZQ</sub> /4	1, 2
		V <sub>OMdc</sub> = 0.8 x V <sub>DD</sub>	0.9	1.0	1.1	R <sub>ZQ</sub> /4	1, 2
		V <sub>OHdc</sub> = 0.95 x V <sub>DD</sub>	0.9	1.0	1.25	R <sub>ZQ</sub> /4	1, 2
	RON <sub>60Pu</sub>	V <sub>OLdc</sub> = 0.5 x V <sub>DD</sub>	0.9	1.0	1.25	R <sub>ZQ</sub> /4	1, 2
		V <sub>OMdc</sub> = 0.8 x V <sub>DD</sub>	0.9	1.0	1.1	R <sub>ZQ</sub> /4	1, 2
		V <sub>OHdc</sub> = 0.95 x V <sub>DD</sub>	0.8	1.0	1.1	R <sub>ZQ</sub> /4	1, 2
Mismatch between pull-up and pull-down, MM <sub>PuPd</sub>		V <sub>OMdc</sub> = 0.8 x V <sub>DD</sub>	-10		10	%	1, 2, 4
Mismatch [M]DQ-[M]DQ within byte variation pull-up, MM <sub>Pudd</sub>		V <sub>OMdc</sub> = 0.8 x V <sub>DD</sub>	0		8	%	1, 2, 3
Mismatch [M]DQ-[M]DQ within byte variation pull-down, MM <sub>Pddd</sub>		V <sub>OMdc</sub> = 0.8 x V <sub>DD</sub>	0		8	%	1, 2, 3

NOTE: A functional representation of the output buffer is shown in Figure 127 Output impedance  $R_{ON}$  is defined by the value of the external reference resistor  $R_{ZQ}$  as defined in Table 269.

## 16.1 [M]DQ/[M]DQS Output Driver DC Electrical Characteristics (cont'd)

The individual pull-up and pull-down resistors ( $RON_{Pu}$  and  $RON_{Pd}$ ) are defined as follows:

$$RON_{Pu} = \frac{(V_{DD} - V_{Out})}{|I_{Out}|} \quad \text{under the condition that } RON_{Pd} \text{ is turned off}$$

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|} \quad \text{under the condition that } RON_{Pu} \text{ is turned off.}$$

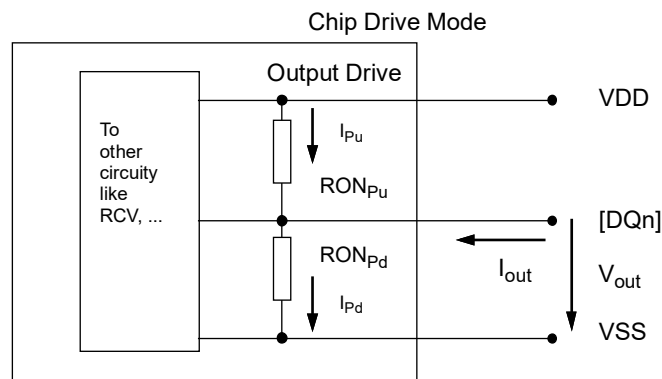


Figure 127 — Output Driver: Definition of Voltages and Currents

- NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see Clause 16.5.
- NOTE 2 Pull-up and pull-down output driver impedances are recommended to be calibrated at  $0.8 * V_{DD}$ . Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at  $0.5 * V_{DD}$  and  $0.95 * V_{DD}$ .
- NOTE 3 [M]DQ to [M]DQ mismatch within byte variation for a given component including [M]DQS\_t and [M]DQS\_c (characterized).
- NOTE 4 Measurement definition for mismatch between pull-up and pull-down,  $MM_{PuPd}$ :  
Measure  $RON_{Pu}$  and  $RON_{Pd}$ , both at  $0.8 * V_{DD}$  separately. Ron-nom is the nominal Ron value:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} \times 100$$

- NOTE 5 RON variance range ratio to RON nominal value in a given component, including [M]DQS\_t and [M]DQS\_c.

$$MM_{Pudd} = \frac{RON_{PuMax} - RON_{PuMin}}{RON_{Nom}} \times 100$$

$$MM_{Pddd} = \frac{RON_{PdMax} - RON_{PdMin}}{RON_{Nom}} \times 100$$

## 16.2 Output Driver DC Electrical Characteristics for LBTXDQS, LBTXDQ

The DDR5 Loopback driver supports 34 ohms. A functional representation of the output buffer is shown in Figure 128. When PG[70]RWE0[7] = 1,  $RON_{Pu}$  is disabled for LBTXDQ.

$$RON_{Pu} = \frac{(V_{DD} - V_{Out})}{|I_{Out}|} \text{ under the condition that } RON_{Pd} \text{ is turned off}$$

$$RON_{PD} = \frac{V_{Out}}{|I_{Out}|} \text{ under the condition that } RON_{Pu} \text{ is turned off.}$$

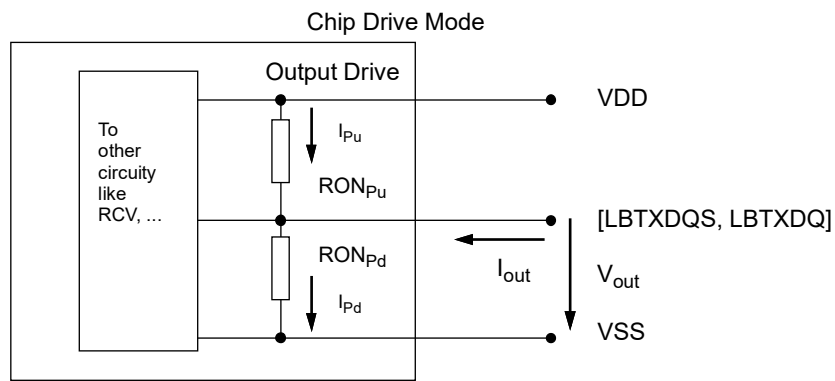


Figure 128 — Output Driver DC Electrical Characteristics for Loopback

### 16.3 tDQSS tDQSD

The following specifies the relationship between the write enable timing window  $t_{WPRE\_EN\_nCycle}$  and the Data Buffer related DQS to BCK drift window  $t_{DQSD}$  as well as the system related DQS to BCK drift window  $t_{DQSS}$  around the final DQS to BCK offset trained pass/fail point based on write leveling feedback in order to support n-Cycle pre-amble mode. Functional operation requires that the following condition be met:

$$t_{WPRE\_EN\_nCycle} \geq |t_{DQSSmin}| + t_{DQSSmax} + |t_{DQSDmin}| + t_{DQSDmax}$$

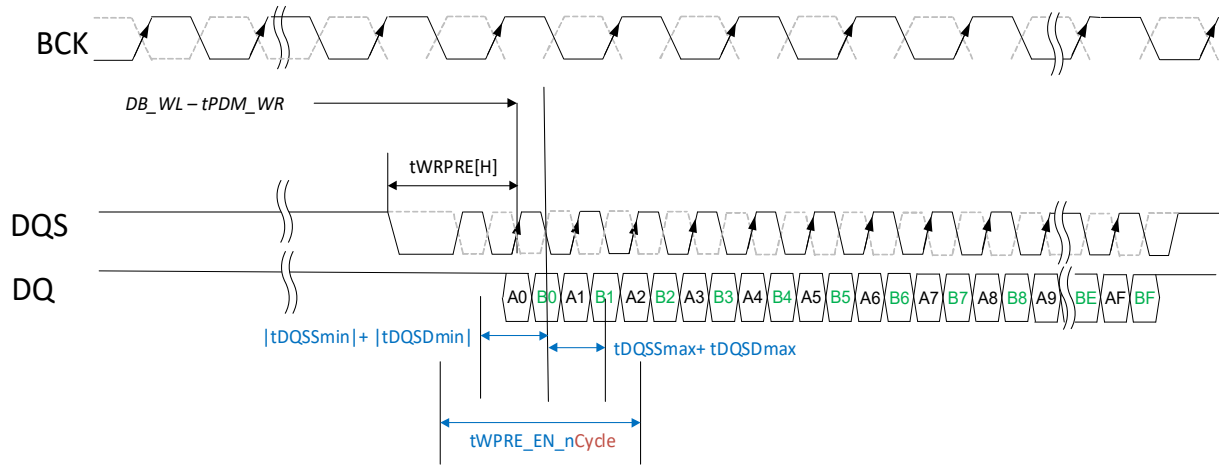


Figure 129 — tDQSS and tDQSD

Table 270 — Write Enable MDB Timing Parameters

Symbol	Parameter	DDR5-3200 to 12800		Units
		Min	Max	
$t_{WPRE\_EN\_3Cycle}$	3-Cycle Write pre-amble enable window	2.5	-	tHDQS
$t_{WPRE\_EN\_4Cycle}$	4-Cycle Write pre-amble enable window	2.5	-	tHDQS
$t_{WPRE\_EN\_5Cycle}$	5-Cycle Write pre-amble enable window	2.5	-	tHDQS
$t_{WPRE\_EN\_6Cycle}$	6-Cycle Write pre-amble enable window	2.5	-	tHDQS
$t_{WPRE\_EN\_7Cycle}$	7-Cycle Write pre-amble enable window	2.5	-	tHDQS
$t_{DQSD}$	MDB voltage/temperature drift window of first rising DQS_t preamble edge relative to MDB DB_WL endpoint with tPDM_WR adjusted	$-0.25 * t_{WPRE\_EN\_nCycle}$	$0.25 * t_{WPRE\_EN\_nCycle}$	tHDQS
$t_{DQSS}$	Host and system voltage/temperature drift window of first rising DQS_t pre-amble edge relative to MDB DB_WL endpoint with tPDM_WR adjusted	$-0.25 * t_{WPRE\_EN\_nCycle}$	$0.25 * t_{WPRE\_EN\_nCycle}$	tHDQS

## 16.4 Clock to Read DQS Timing Parameters

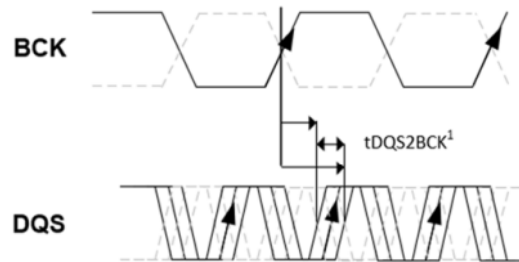


Figure 130 —  $t_{DQS2BCK}$

NOTE:  $t_{DQS2BCK}$  is the variance window on DQS, measured from the earliest phase to the latest phase as defined by BCK.

Table 271 — Read Enable Timing Parameters 3200 to 12800

Symbol	Parameter	DDR5-3200 to 12800		Unit
		Min	Max	
$t_{DQS2BCK}^{1,2,3}$	DQS_t-DQS_c rising edge output variance window	-	0.75	tHDQS

NOTE 1 Measured over full VDD and Temperature spec range

NOTE 2 Measured for a given MDB part and for each DQS\_t/DQS\_c pair

NOTE 3 These parameters are verified by design and characterization

## 16.5 Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the following tables.

Table 272 — Output Driver and Termination Resistor Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	Note
$R_{ONPD}$	$0.8 \times VDD$	$90 - (dR_{ONPD}dT \times  \Delta T ) - (dR_{ONPD}dV \times  \Delta V )$	$110 + (dR_{ONPD}dT \times  \Delta T ) + (dR_{ONPD}dV \times  \Delta V )$	%	1,2
$R_{ONPU}$	$0.8 \times VDD$	$90 - (dR_{ONPU}dT \times  \Delta T ) - (dR_{ONPU}dV \times  \Delta V )$	$110 + (dR_{ONPU}dT \times  \Delta T ) + (dR_{ONPU}dV \times  \Delta V )$	%	1,2
$R_{RTT}$	$0.8 \times VDD$	$90 - (dR_{RTT}dT \times  \Delta T ) - (dR_{RTT}dV \times  \Delta V )$	$110 + (dR_{RTT}dT \times  \Delta T ) + (dR_{RTT}dV \times  \Delta V )$	%	1,2

NOTE 1  $\Delta T = T - T(@ \text{Calibration})$ ,  $\Delta V = V - V(@ \text{Calibration})$

NOTE 2  $dR_{ONPD}dT$ ,  $dR_{ONPD}dV$ ,  $dR_{ONPU}dT$ ,  $dR_{ONPU}dV$ ,  $dR_{RTT}dV$ , and  $dR_{RTT}dT$  are not subject to production test but are verified by design and characterization.

## 16.5 Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity (cont'd)

**Table 273 — Output Driver and Termination Resistor Temperature and Supply Voltage Sensitivity**

Symbol	Parameter	Min	Max	Unit
$dR_{ONPD}dT$	$R_{ONPD}$ Temperature Sensitivity	0.0	0.1	%/°C
$dR_{ONPD}dV$	$R_{ONPD}$ Voltage Sensitivity	0.0	0.1	%/mV
$dR_{ONPU}dT$	$R_{ONPU}$ Temperature Sensitivity	0.0	0.1	%/°C
$dR_{ONPU}dV$	$R_{ONPU}$ Voltage Sensitivity	0.0	0.1	%/mV
$dR_{RTT}dT$	$R_{RTT}$ Temperature Sensitivity	0.0	0.1	%/°C
$dR_{RTT}dV$	$R_{TT}$ Voltage Sensitivity	0.0	0.1	%/mV

## 16.6 Single-ended AC and DC Output Levels

**Table 274 — Single-ended AC and DC output Levels**

Symbol	Parameter	DDR5-3200 to 12800	Unit	Note
$V_{OH}(DC)$	DC output HIGH measurement level (for IV curve linearity)	$0.95 \times V_{DD}$	V	
$V_{OM}(DC)$	DC output MID measurement level (for IV curve linearity)	$0.80 \times V_{DD}$	V	
$V_{OL}(DC)$	DC output LOW measurement level (for IV curve linearity)	$0.50 \times V_{DD}$	V	
$V_{OH}(AC)$	AC output HIGH measurement level (for output SR)	$0.75 \times V_{pk-pk}$	V	1
$V_{OL}(AC)$	AC output LOW measurement level (for output SR)	$0.25 \times V_{pk-pk}$	V	1

NOTE 1  $V_{pk-pk}$  is the mean HIGH voltage minus the mean LOW voltage over 1e6 samples.

## 16.7 Differential AC Output Levels

**Table 275 — Differential AC output levels**

Symbol	Parameter	DDR5-3200 to 12800	Unit	Note
$V_{OHdiff}(AC)$	AC differential output HIGH measurement level (for output SR)	$0.75 \times V_{diffpk-pk}$	V	1
$V_{OLdiff}(AC)$	AC differential output LOW measurement level (for output SR)	$0.25 \times V_{diffpk-pk}$	V	1

NOTE 1  $V_{diffpk-pk}$  is the mean HIGH voltage minus the mean LOW voltage over 1e6 samples.

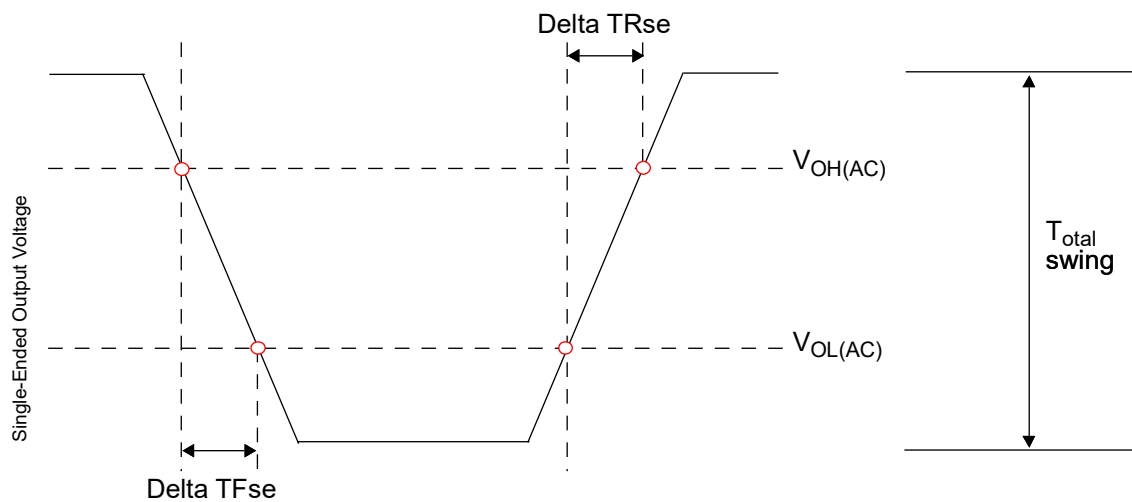
## 16.8 Single-Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between  $V_{OL(AC)}$  and  $V_{OH(AC)}$  for single-ended signals as shown in Table 276 and Figure 131.

**Table 276 — Single-ended Output Slew Rate Definition**

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta t_{Rse}$
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}] / \Delta t_{Fse}$

NOTE 1 Output slew rate is verified by design and characterization, and may not be subject to production test.



**Figure 131 — Output Single-Ended Slew Rate Definition**

**Table 277 — Output Single-Ended Edge Rates over Specified Operating Temperature Range**

Symbol	Parameter	Conditions	DDR5-3200 to 12800		Unit
			Min	Max	
$dV/dt_{se\_r}$	DQS rising edge single-ended Slew Rate <sup>1,2</sup>	1.1V operation	10	-	V/ns
$dV/dt_{se\_f}$	DQS falling edge single-ended Slew Rate <sup>1,2</sup>	1.1V operation	10	-	V/ns
$dV/dt_{se\_r}$	DQ rising edge single-ended Slew Rate <sup>3,2</sup>	1.1V operation	12	-	V/ns
$dV/dt_{se\_f}$	DQ falling edge single-ended Slew Rate <sup>3,2</sup>	1.1V operation	12	-	V/ns
$dV/dt_{se\_r}$	MDQ, MDQS rising edge single-ended Slew Rate <sup>4,2</sup>	1.1V operation	8	-	V/ns
$dV/dt_{se\_f}$	MDQ, MDQS falling edge single-ended Slew Rate <sup>5,2</sup>	1.1V operation	8	-	V/ns

NOTE 1 These parameters are for the DQS[1:0]\_t, DQS[1:0]\_c. The base range values are applicable only for  $R_{on}=RZQ/7$ ,  $V_{DD}=1.1V$ , and  $25^{\circ}C$ .

NOTE 2 Measured into 50- $\Omega$  reference load terminated to  $V_{DD}$ , as shown in Figure 160.

NOTE 3 These parameters are for the DQ[7:0]. The base range values are applicable only for  $R_{on}=RZQ/7$ ,  $V_{DD}=1.1V$ , and  $25^{\circ}C$ .

NOTE 4 These parameters are for the MDQ[7:0], MDQS[1:0]\_t, and MDQS[1:0]\_c outputs.



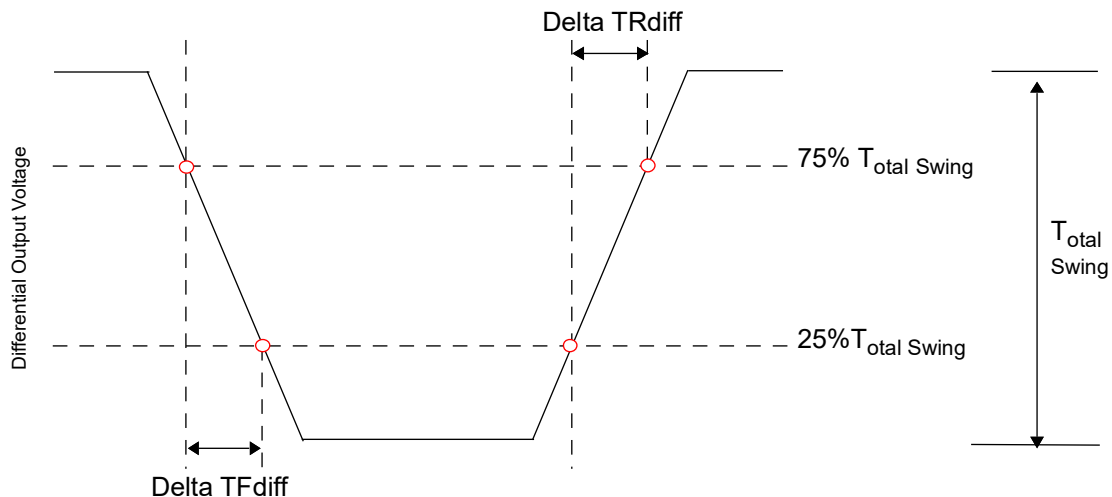
## 16.9 Differential Output Slew Rate

Output slew rates for differential signals  $DQS\_t / DQS\_c$  and  $MDQS\_t / MDQS\_c$  are defined and measured as shown in Table 278 and Figure 132.

**Table 278 — Output Clock Differential Slew Rate Definition for  $DQS\_t/DQS\_c$  and  $MDQS\_t/MDQS\_c$**

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge ( $DQS\_t / DQS\_c$ and $MDQS\_t / MDQS\_c$ ).	25%	75%	$[ 25\% - 75\% ] / \Delta TR_{diff}$
Differential output slew rate for falling edge ( $DQS\_t / DQS\_c$ and $MDQS\_t / MDQS\_c$ ).	75%	25%	$[ 75\% - 25\% ] / \Delta TF_{diff}$

**NOTE** Differential output slew rate is verified by design and characterization, and may not be subject to production test.



**Figure 132 — Differential Output Slew Rate Definition for  $DQS\_t / DQS\_c$  and  $MDQS\_t / MDQS\_c$**

**Table 279 — Output Differential Edge Rates over Specified Operating Temperature Range**

Symbol	Parameter	Conditions	DDR5-3200 to 12800		Unit
			Min	Max	
$dV/dt\_r$	DQS rising edge differential Slew Rate <sup>1,2</sup>	1.1V operation	20	-	V/ns
$dV/dt\_f$	DQS falling edge differential Slew Rate <sup>1,2</sup>	1.1V operation	20	-	V/ns
$dV/dt\_r$	MDQS rising edge differential Slew Rate <sup>3,2</sup>	1.1V operation	16	-	V/ns
$dV/dt\_f$	MDQS falling edge differential Slew Rate <sup>3,2</sup>	1.1V operation	16	-	V/ns

NOTE 1 These parameters are for the  $DQS0\_t/DQS0\_c$ ,  $DQS1\_t/DQS1\_c$  outputs. The base range values are applicable only for  $R_{on}=RZQ/7$ ,  $V_{DD}=1.1V$ , and  $25^{\circ}C$ .

NOTE 2 Measured into 50- $\Omega$  reference load terminated to  $V_{DD}$ , as shown in Figure 160.

NOTE 3 These parameters are for the  $A(B)\_MDQS0\_t/A(B)\_MDQS0\_c$ , and  $A(B)\_MDQS1\_t/A(B)\_MDQS1\_c$  outputs.

16.10 Differential Output Cross Point Voltage

The differential cross point output voltage is defined as the max to min cross point measured on the differential signals DQS\_t / DQS\_c and MDQS\_t / MDQS\_c with respect to the output common mode voltage ( $V_{OCM}$ ).

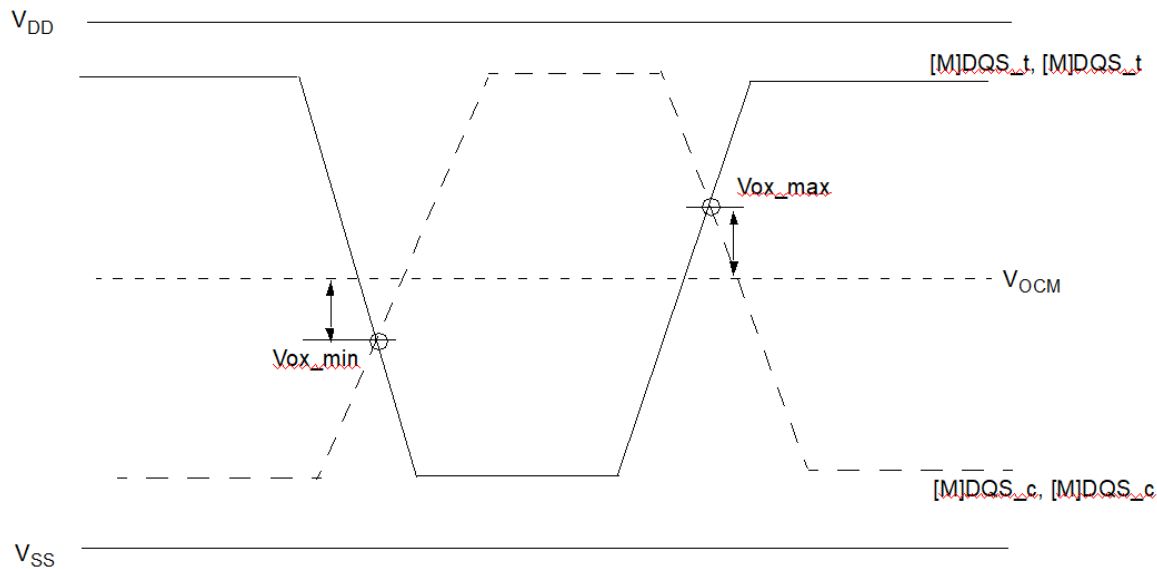


Figure 133 —  $V_{ox}$  Definition (DQS and MDQS)

Table 280 — Output Cross Point Voltage for DQS\_t / DQS\_c and MDQS\_t / MDQS\_c

Symbol	Parameter	DDR5-3200 to 12800		Unit	NOTE
		Min	Max		
$V_{ox\_DQS\_Ratio}$	DQS Differential Output Cross-Point Voltage Ratio	-	20	%	1, 2
$V_{ox\_MDQS\_Ratio}$	MDQS Differential Output Cross-Point Voltage Ratio	-	20	%	1,2

NOTE 1 Referenced to  $V_{OCM} = \text{avg} ([M]DQS_t + [M]DQS_c)/2$  where the average is over 1e6 UI.  
NOTE 2  $V_{ox\_DQS\_Ratio} = 100 \times (|V_{ox\_DQS}|/V_{diff\_DQS} \text{ pk-pk})$  where  $V_{diffDQS} \text{ pk-pk} = 2 \times |VDQS_t - VDQS_c|$ .

## 16.11 TX Transmit Statistical Parameters

### 16.11.1 Tx DQS Jitter - Host Interface

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5MDB02 device output jitter must not exceed maximum values specified in Table 281.

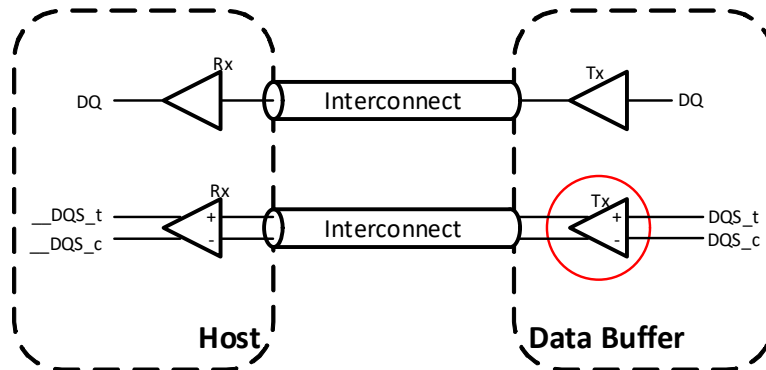


Figure 134 — Example of DQS TX

## 16.11.1 Tx DQS Jitter - Host Interface (cont'd)

Table 281 — Tx DQS Jitter Parameters

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Symbol	Parameter	DDR5-3200 to 12800		Unit	NOTE
		Min	Max		
tTx_DQS_1UI_Rj_NoBUJ	Rj RMS Value of 1-UI Jitter without BUJ	-	0.0042	UI (RMS)	1, 2, 3, 4, 8, 9, 10, 11
tTx_DQS_1UI_Dj_NoBUJ	Dj pp Value of 1-UI Jitter without BUJ	-	0.045	UI	1, 2, 4, 5, 8, 9, 10, 11
tTx_DQS_NUI_Rj_NoBUJ	Rj RMS Value of N-UI Jitter without BUJ, where $1 < N < 4$ when at or below 4800MT/s, or $1 < N < 6$ when above 4800MT/s.	-	0.0045	UI (RMS)	1, 2, 4, 6, 8, 9, 10, 11
tTx_DQS_NUI_Dj_NoBUJ	Dj pp Value of N-UI Jitter without BUJ, where $1 < N < 4$ when at or below 4800MT/s, or $1 < N < 6$ when above 4800MT/s.	-	0.070	UI	1, 2, 4, 7, 8, 9, 10, 11
* UI=tHDQS(avg)min/2					
NOTE 1 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being MDB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.					
NOTE 2 On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being MDB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.					
NOTE 3 Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD.					
NOTE 4 This test should be done in typical temperature and voltage conditions (i.e., $V_{DD} = 1.1 \text{ V}$ , $25^\circ\text{C}$ ).					
NOTE 5 Dj pp value of 1-UI jitter. Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.					
NOTE 6 Rj RMS Value of N-UI jitter. Without BUJ but on-die system like noise present. This extraction is to be done after software correction of DCD.					
NOTE 7 Dj pp RMS value of N-UI jitter. Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.					
NOTE 8 See Clause 14.2.2 for details on minimum BER requirements.					
NOTE 9 See Clause 14.2.3 for details on UI, NUI and Jitter definitions.					
NOTE 10 Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test.					
NOTE 11 These parameters are tested using the continuous burst mode which are sent out from the DDR5MDB02 device without the need for sending out continuous MRR commands. Control Word Bit RW90 OP[0] is set to "1" to enable this feature.					

### 16.11.2 Tx DQ Jitter - Host Interface

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 282.

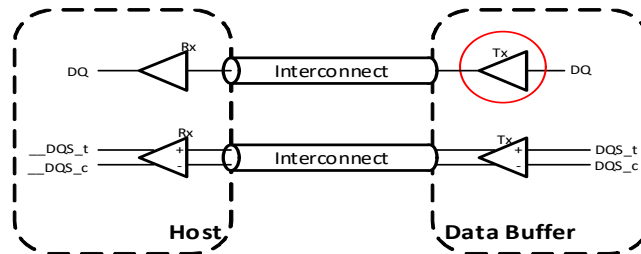


Figure 135 — Example of DQ TX

Table 282 — Tx DQ Jitter Parameters

[BER=Bit Error Rate; DCD = Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Symbol	Parameter	DDR5-3200 to 12800		Unit	NOTE
		Min	Max		
tTx_DQ_1UI_Rj_NoBUJ	Rj RMS of 1-UI jitter without BUJ	-	0.0042	UI (RMS)	1, 2, 3, 4, 9, 10, 11, 12, 13
tTx_DQ_1UI_Dj_NoBUJ	Dj pp 1-UI jitter without BUJ	-	0.045	UI	1, 2, 4, 5, 9, 10, 11, 12, 13
tTx_DQ_NUI_Rj_NoBUJ	Rj RMS of N-UI jitter without BUJ, where $1 < N < 4$ when at or below 4800MT/s, or $1 < N < 6$ when above 4800MT/s.	-	0.0045	UI (RMS)	1, 2, 4, 6, 9, 10, 11, 12, 13
tTx_DQ_NUI_Dj_NoBUJ	Dj pp value of N-UI jitter without BUJ, where $1 < N < 4$ when at or below 4800MT/s, or $1 < N < 6$ when above 4800MT/s.	-	0.070	UI	1, 2, 4, 7, 9, 10, 11, 12, 13
tTx_DQS2DQ	Delay of any data lane relative to strobe lane	-0.2	0.2	UI	4, 8, 9, 10, 12, 13

**Table 282 — Tx DQ Jitter Parameters (cont'd)**

[BER=Bit Error Rate; DCD = Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Symbol	Parameter	DDR5-3200 to 12800		Unit	NOTE
		Min	Max		
* UI=tHDQS(avg)min/2					
NOTE 1	On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being MDB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.				
NOTE 2	On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being MDB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.				
NOTE 3	Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD.				
NOTE 4	This test should be done in typical temperature and voltage conditions (i.e., V <sub>DD</sub> = 1.1 V, 25 °C).				
NOTE 5	Dj pp value of 1-UI jitter without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.				
NOTE 6	Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD.				
NOTE 7	Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.				
NOTE 8	Delay of any data lane relative to strobe lane, as measured at Tx output.				
NOTE 9	Vref noise level to DQ jitter should be adjusted to minimize DCD.				
NOTE 10	See Clause 14.2.2 for details on the minimum BER requirements.				
NOTE 11	See Clause 14.2.3 for details on UI, NUI and Jitter definitions.				
NOTE 12	Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test.				
NOTE 13	These parameters are tested using the continuous burst mode which are sent out from the DDR5MDB02 device without the need for sending out continuous MRR commands. Control Word Bit RW90 OP[0] is set to “1” to enable this feature.				

### 16.11.3 TX DQ Stressed Eye - Host Interface

Tx DQ stressed eye height and eye width must meet minimum specification values at BER = E-9 and confidence level 99.5%. Tx DQ Stressed Eye shows the DQS to DQ skew for both Eye Width and Eye Height. In order to support different Host Receiver (Rx) designs, it is the responsibility of the Host to insure the advanced DQS edges are adjusted accordingly via the Read DQS Offset Timing mode register settings ([RW8F OP\[3:0\]](#)).

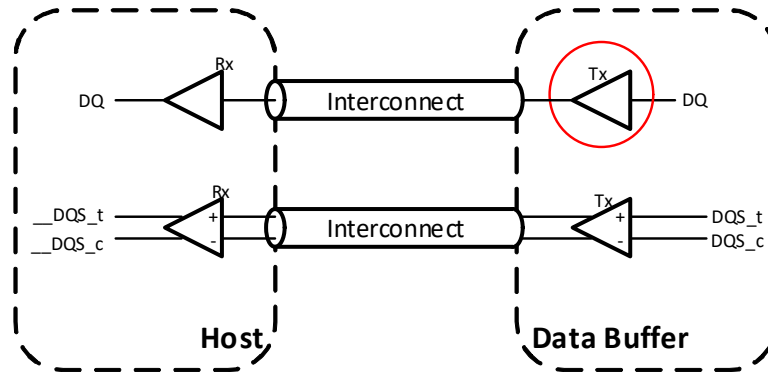


Figure 136 — Example of DQ TX

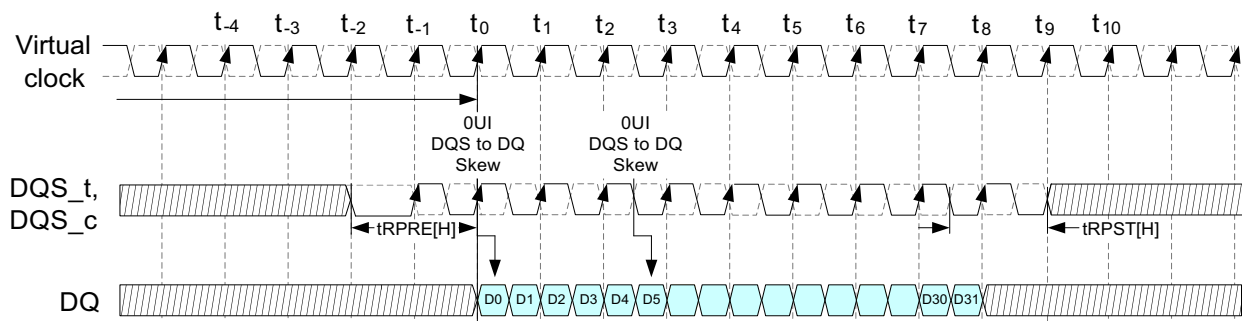


Figure 137 — Read Burst Example for Pin DQx Depicting Bit 0 and 5 Relative to the DQS Edge for 0 UI Skew

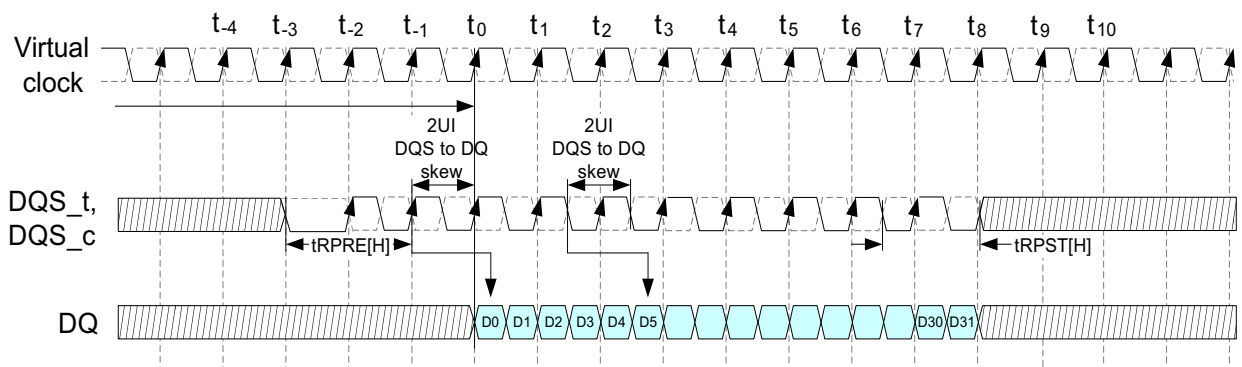


Figure 138 — Read Burst Example for Pin DQx Depicting Bit 0 and 5 Relative to the DQS Edge for 2 UI Skew with Read DQS Offset Timing Set to 1 Clock (2UI) Skew

## 16.11.3 TX DQ Stressed Eye - Host Interface (cont'd)

Table 283 — TX DQ Stressed Eye Parameters

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate, SES=Stressed Eye Skew]

Symbol	Parameter	DDR5-3200 to 12800		Unit	NOTE
		Min	Max		
TxEW_DQ_SES_1UI	Eye Width specified at the transmitter with a skew between DQ and DQS of 1UI	0.78	-	UI	1,2,3,4,6,7,8,9,10,11
TxEW_DQ_SES_2UI	Eye Width specified at the transmitter with a skew between DQ and DQS of 2UI	0.78	-	UI	1,2,3,4,6,7,8,9,10,11
TxEW_DQ_SES_3UI	Eye Width specified at the transmitter with a skew between DQ and DQS of 3UI	0.78	-	UI	1,2,3,4,6,7,8,9,10,11
TxEW_DQ_SES_4UI	Eye Width specified at the transmitter with a skew between DQ and DQS of 4UI	0.78	-	UI	1,2,3,4,5,6,7,8,9,10,11
TxEW_DQ_SES_5UI	Eye Width specified at the transmitter with a skew between DQ and DQS of 5UI	0.78	-	UI	1,2,3,4,5,6,7,8,9,10,11
<p>* UI=tHDQS(avg)min/2</p> <p>NOTE 1 Minimum BER 1E-9 and Confidence Level of 99.5% per pin</p> <p>NOTE 2 Refer to the minimum Bit Error Rate (BER) requirements for DDR5</p> <p>NOTE 3 The validation methodology for these parameters will be covered in future ballot(s)</p> <p>NOTE 4 Mismatch is defined as DQS to DQ mismatch, in UI increments</p> <p>NOTE 5 The number of UIs accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable</p> <p>NOTE 6 The Duty Cycle of the DQ pins must be adjusted as close to 50% as possible using the Duty Cycle Adjuster feature prior to running this test</p> <p>NOTE 7 The Configuration Registers for the Duty Cycle Adjuster are PG[C]RW[E0]. The Registers for the Per Nibble DCA are PC[C]RW[E4:E1]. The Registers for the Per Pin DCA are PG[C]RW[F5:F0, FD:F8].</p> <p>NOTE 8 Spread Spectrum Clocking (SSC) must be disabled while running this test</p> <p>NOTE 9 These parameters are tested in Mux mode and HIR using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the MDB without the need for sending out continuous RD commands. The RW90[0] is set to “1” to enable this feature.</p> <p>NOTE 10 Tested on the CTC2 card only.</p> <p>NOTE 11 Matched DQS to DQ would require the DQS to be adjusted by 0.5UI to place it in the center of the DQ eye. 1UI skew would require the DQS to be adjusted 1.5UI. Generally, for xUI skew the DQ must be adjusted (x + 0.5) UI to be placed in the center of the eye.</p>					



#### 16.11.4 TX MDQ Stressed Eye - DRAM Interface

Tx MDQ stressed eye height and eye width must meet minimum specification values at BER = E-9 and confidence level 99.5%. Tx MDQ Stressed Eye shows the MDQS to MDQ skew for both Eye Width and Eye Height. In order to support the full range of DRAM tRx\_DQS2DQ, it is the responsibility of the Host to insure MDQ phases with respect to MDQS are adjusted accordingly via the MDQ Write Baseline Delay register settings (PG[1:0]RWE6 and PG[1:0]RWE7).

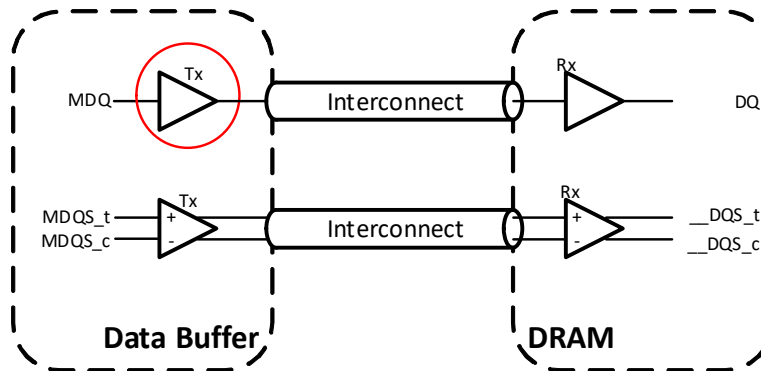


Figure 139 — Example of MDQ TX

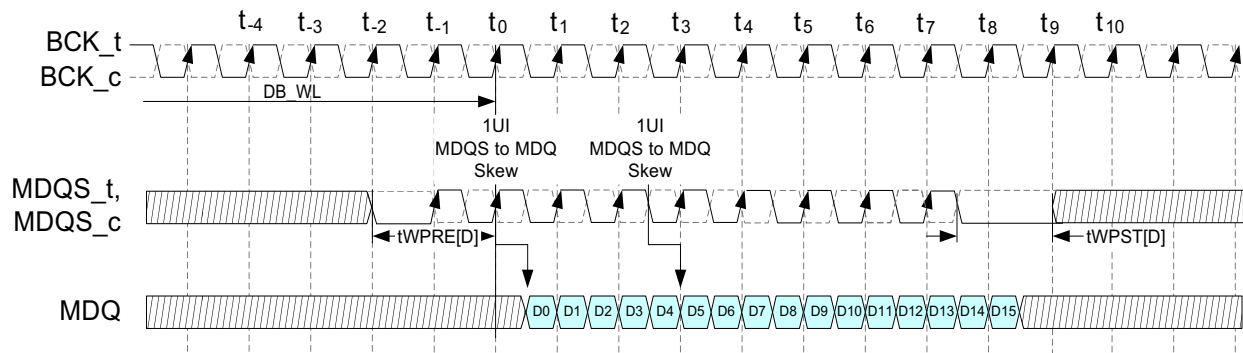


Figure 140 — Write Burst Example for Pin MDQx Depicting Bit 0 and 5 Relative to the MDQS Edge for 1 UI Skew

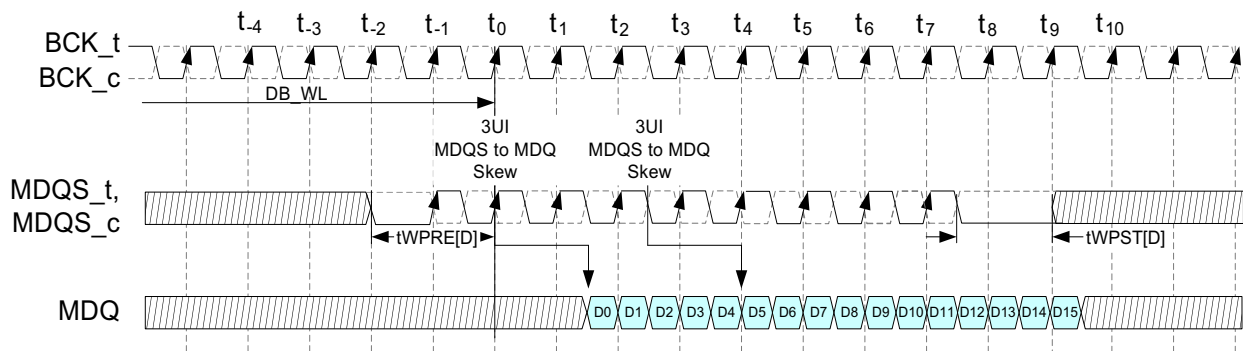


Figure 141 — Write Burst Example for Pin MDQx Depicting Bit 0 and 5 Relative to the MDQS Edge for 3 UI Skew with MDQ Write Baseline Delay Timing Set to 1.5 Clock (3UI)

**16.11.4 TX MDQ Stressed Eye - DRAM Interface (cont'd)****Table 284 — TX MDQ Stressed Eye Parameters**

[EH=Eye Height, EW=Eye Width; BER=Bit Error Rate, SES=Stressed Eye Skew]

Symbol	Parameter	DDR5-3200 to 6400		Unit	NOTE
		Min	Max		
TxEW_MDQ_SES_1UI	Eye Width specified at the transmitter with a skew between MDQ and MDQS of 1UI	0.78	-	UI	1,2,3,4,6,7,8,9
TxEW_MDQ_SES_2UI	Eye Width specified at the transmitter with a skew between MDQ and MDQS of 2UI	0.78	-	UI	1,2,3,4,6,7,8,9
TxEW_MDQ_SES_3UI	Eye Width specified at the transmitter with a skew between MDQ and MDQS of 3UI	0.78	-	UI	1,2,3,4,6,7,8,9
TxEW_MDQ_SES_4UI	Eye Width specified at the transmitter with a skew between MDQ and MDQS of 4UI	0.78	-	UI	1,2,3,4,5,6,7,8,9
TxEW_MDQ_SES_5UI	Eye Width specified at the transmitter with a skew between MDQ and MDQS of 5UI	0.78	-	UI	1,2,3,4,5,6,7,8,9
<p>* <math>UI = tBCK(ave)min/2</math></p> <p>NOTE 1 Minimum BER 1E-9 and Confidence Level of 99.5% per pin</p> <p>NOTE 2 Refer to the minimum Bit Error Rate (BER) requirements for DDR5</p> <p>NOTE 3 The validation methodology for these parameters will be covered in future ballot(s)</p> <p>NOTE 4 Mismatch is defined as DQS to DQ mismatch, in UI increments</p> <p>NOTE 5 The number of UIs accumulated will depend on the speed of the link. For higher speeds, higher UI accumulation may be specified. For lower speeds, N=4,5 UI may not be applicable</p> <p>NOTE 6 Spread Spectrum Clocking (SSC) must be disabled while running this test</p> <p>NOTE 7 These parameters are tested in Mux mode and MWD using the continuous PRBS8 LFSR training pattern which are sent out on all DQ lanes off the MDB without the need for sending out continuous WR commands. The <a href="#">RW90[0]</a> is set to “1” to enable this feature.</p> <p>NOTE 8 Tested on the CTC2 card only</p> <p>NOTE 9 MDQS to MDQ would require the MDQS to be placed in the center of the MDQ eye. 1UI skew would require the MDQS to be adjusted 1UI. Generally, for xUI skew the MDQ must be adjusted xUI to be placed in the center of the eye.</p>					

### 16.11.5 Tx MDQS Jitter - Dram Interface

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5MDB02 device output jitter must not exceed maximum values specified in Table 285.

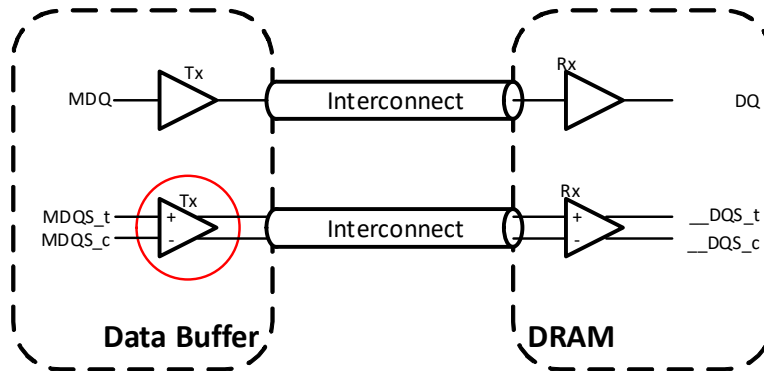


Figure 142 — Example of MDQS TX

Table 285 — Tx MDQS Jitter Parameters

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Symbol	Parameter	DDR5-3200 to 6400		Unit	NOTE
		Min	Max		
tTx_MDQS_1UI_Rj_NoBUJ	Rj RMS Value of 1-UI Jitter without BUJ	-	0.003	UI (RMS)	1, 2, 3, 4, 8, 9, 10, 11
tTx_MDQS_1UI_Dj_NoBUJ	Dj pp Value of 1-UI Jitter without BUJ	-	0.028	UI	1, 2, 4, 5, 8, 9, 10, 11
tTx_MDQS_NUI_Rj_NoBUJ	Rj RMS Value of N-UI Jitter without BUJ, where $1 < N < 4$ when at or below 4800MT/s, or $1 < N < 6$ when above 4800MT/s.	-	0.0035	UI (RMS)	1, 2, 4, 6, 8, 9, 10, 11
tTx_MDQS_NUI_Dj_NoBUJ	Dj pp Value of N-UI Jitter without BUJ, where $1 < N < 4$ when at or below 4800MT/s, or $1 < N < 6$ when above 4800MT/s.	-	0.065	UI	1, 2, 4, 7, 8, 9, 10, 11

**Table 285 — Tx MDQS Jitter Parameters (cont'd)**

[BER=Bit Error Rate; DCD=Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Symbol	Parameter	DDR5-3200 to 6400		Unit	NOTE
		Min	Max		
* UI=tBCK(avg)min/2					
NOTE 1	On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being MDB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.				
NOTE 2	On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being MDB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers, so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.				
NOTE 3	Rj RMS value of 1-UI jitter. Without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD.				
NOTE 4	This test should be done in typical temperature and voltage conditions (i.e., V <sub>DD</sub> = 1.1 V, 25 °C).				
NOTE 5	Dj pp value of 1-UI jitter. Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.				
NOTE 6	Rj RMS Value of N-UI jitter. Without BUJ but on-die system like noise present. This extraction is to be done after software correction of DCD.				
NOTE 7	Dj pp RMS value of N-UI jitter. Without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.				
NOTE 8	See Clause 14.2.2 for details on minimum BER requirements.				
NOTE 9	See Clause 14.2.3 for details on UI, NUI and Jitter definitions.				
NOTE 10	Spread Spectrum Clocking (SSC) must be disabled while running the Tx DQ Jitter test.				
NOTE 11	These parameters are tested using the continuous burst mode which are sent out from the DDR5MDB02 device without the need for sending out continuous MRR commands. Control Word Bit RW90 OP[0] is set to “1” to enable this feature.				

### 16.11.6 Tx MDQ Jitter - DRAM Interface

The Random Jitter (Rj) specified is a random jitter meeting a Gaussian distribution. The Deterministic Jitter (Dj) specified is bounded. The DDR5 device output jitter must not exceed maximum values specified in Table 286.

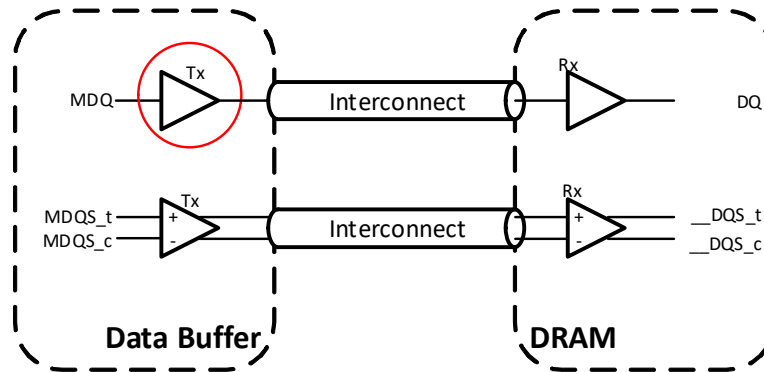


Figure 143 — Example of MDQ TX

Table 286 — Tx MDQ Jitter Parameters for DDR5-3200 to 6400

[BER=Bit Error Rate; DCD = Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Symbol	Parameter	DDR5-3200 to 6400		Unit	NOTE
		Min	Max		
tTx_MDQ_1UI_Rj_NoBUJ	Rj RMS of 1-UI jitter without BUJ	-	0.003	UI (RMS)	1, 2, 3, 4, 9, 10, 11, 12, 13
tTx_MDQ_1UI_Dj_NoBUJ	Dj pp 1-UI jitter without BUJ	-	0.028	UI	1, 2, 4, 5, 9, 10, 11, 12, 13
tTx_MDQ_NUI_Rj_NoBUJ	Rj RMS of N-UI jitter without BUJ, where $1 < N < 4$ when at or below 4800MT/s, or $1 < N < 6$ when above 4800MT/s.	-	0.0035	UI (RMS)	1, 2, 4, 6, 9, 10, 11, 12, 13
tTx_MDQ_NUI_Dj_NoBUJ	Dj pp value of N-UI jitter without BUJ, where $1 < N < 4$ when at or below 4800MT/s, or $1 < N < 6$ when above 4800MT/s.	-	0.065	UI	1, 2, 4, 7, 9, 10, 11, 12, 13

**Table 286 — Tx MDQ Jitter Parameters for DDR5-3200 to 6400 (cont'd)**

[BER=Bit Error Rate; DCD = Duty Cycle Distortion; Rj=Random Jitter; Sj=Sinusoidal Jitter; p-p =peak to peak]

Symbol	Parameter	DDR5-3200 to 6400		Unit	NOTE
		Min	Max		
* UI=tBCK(avg)min/2					
NOTE 1	On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of the cross-talk is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being MDB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.				
NOTE 2	On-die noise similar to that occurring with all the transmitter and receiver lanes toggling need to be stimulated. When there is no socket in transmitter measurement setup, in many cases, the contribution of BUJ is not significant or can be estimated within tolerable error even with all the transmitter lanes sending patterns. When a socket is present, such as DUT being MDB component, the contribution of the cross-talk could be significant. To minimize the impact of crosstalk on the measurement results, a small group of selected lanes in the vicinity of the lane under test may be turned off (sending DC), while the remaining TX lanes send patterns to the corresponding RX receivers so as to excite realistic on-die noise profile from device switching. Note that there may be cases when one of Dj and Rj specs is met and another violated in which case the signaling analysis should be run to determine link feasibility.				
NOTE 3	Rj RMS value of 1-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD.				
NOTE 4	This test should be done in typical temperature and voltage conditions (i.e., VDD = 1.1 V, 25 °C).				
NOTE 5	Dj pp value of 1-UI jitter without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.				
NOTE 6	Rj RMS value of N-UI jitter without BUJ, but on-die system like noise present. This extraction is to be done after software correction of DCD.				
NOTE 7	Dj pp value of N-UI jitter without BUJ, but on-die system like noise present. Dj indicates Djdd of dual-Dirac fitting, after software correction of DCD.				
NOTE 8	Delay of any data lane relative to strobe lane, as measured at Tx output.				
NOTE 9	Vref noise level to MDQ jitter should be adjusted to minimize DCD.				
NOTE 10	See Clause 14.2.2 for details on the minimum BER requirements.				
NOTE 11	See Clause 14.2.3 for details on UI, NUI and Jitter definitions.				
NOTE 12	Spread Spectrum Clocking (SSC) must be disabled while running the Tx MDQ Jitter test.				
NOTE 13	These parameters are tested using the continuous burst mode which are sent out from the DDR5MDB02 device without the need for sending out continuous MRR commands. Control Word Bit RW90 OP[0] is set to “1” to enable this feature.				

## 17 Vref Specifications

### 17.1 VrefDQ, VrefMDQ, and BVref Specifications

The internal VrefDQ, VrefMDQ, and BVref specifications parameters are Vref operating range, Vref step size, Vref set tolerance, Vref step time, and Vref valid tolerance.

The Vref operating range specifies the minimum required Vref setting range for DDR5MDB02 devices and is specific by a Vref min operating point and a Vref max operating point, as depicted in Figure 144.

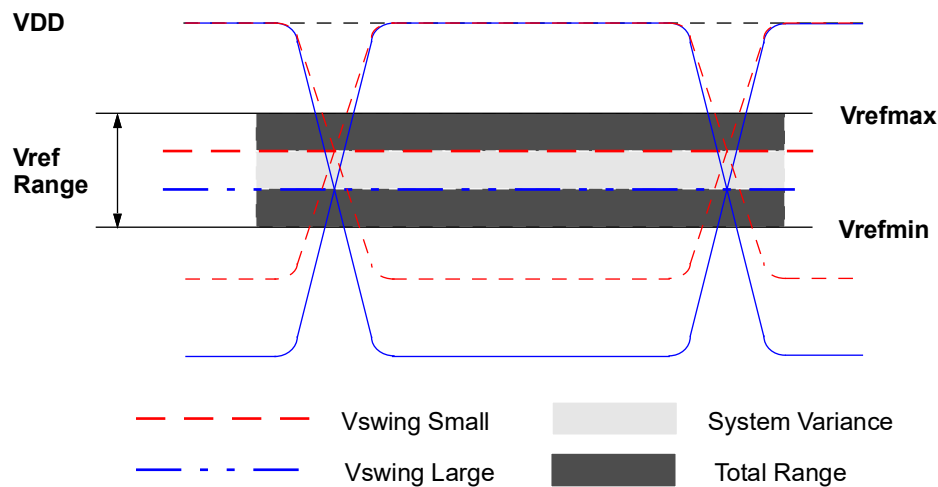
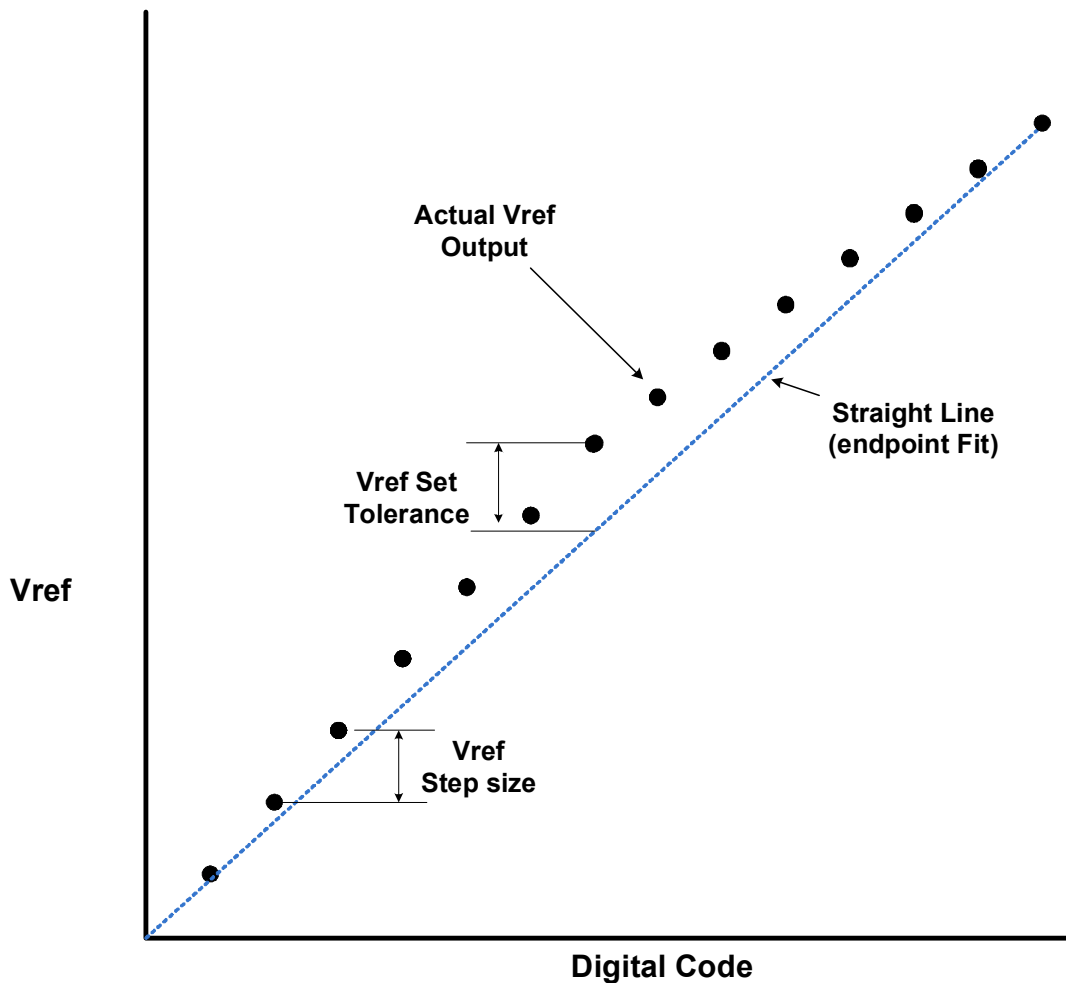


Figure 144 — Vref operating range (Vrefmin, Vrefmax)

The Vref step size is defined as the target voltage increment between adjacent steps. For a given design, the DDR5MDB02 VrefDQ, VrefMDQ, and BVref step size must be within the range specified.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two parameters for Vref set tolerance uncertainty for different numbers of steps  $n$ . The Vref set tolerance is measured with respect to the ideal line, which is based on two endpoints, where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the step size and Vref set tolerance is shown below in Figure 145.

## 17.1 VrefDQ, VrefMDQ, and BVref Specifications (cont'd)



**Figure 145 — Example of Vref Set Tolerance (only Max Case is Shown) and Step Size**

The Vref increment/decrement step times are defined by Vref\_time. Vref\_time is defined from t0 to t1 as shown in Figure 146, where t0 is referenced to when the RW write occurs and t1 is referenced to when the Vref voltage is at the final DC level within the Vref valid tolerance (Vref\_val\_tol).

The Vref valid level is defined by Vref\_val\_tol to qualify the step time t1 as shown in Figure 147. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for component level validation/characterization.

Vref\_time is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change in Vref voltage.

t0 - is referenced to RW write command clock

t1 - is referenced to the Vref\_val\_tol



17.1 VrefDQ, VrefMDQ, and BVref Specifications (cont'd)

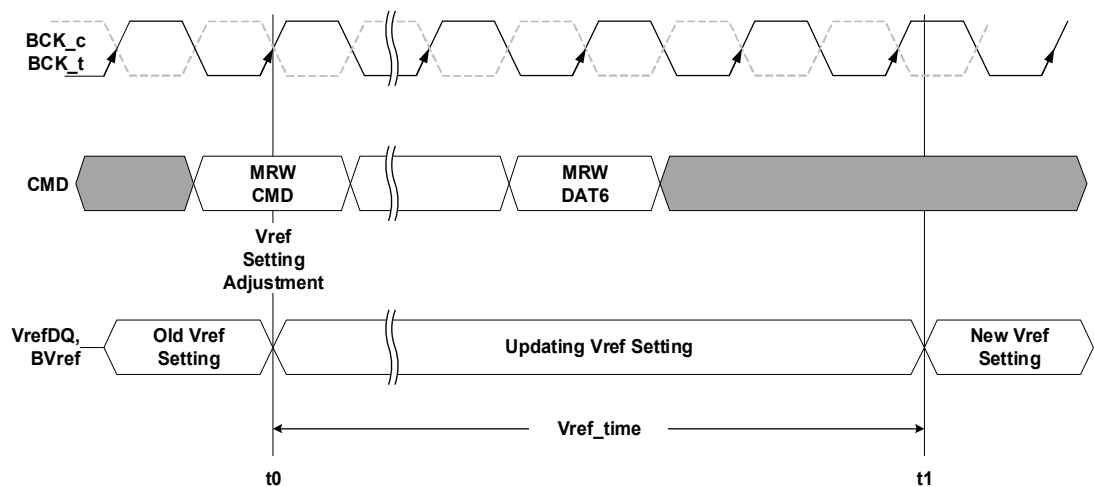


Figure 146 — Vref\_time Timing Diagram

An MRW write to the (Internal Vref Control Word) is used to program the Vref value.

The minimum time required between two Vref MRW commands is Vref\_time\_short, for  $n < 16$  steps, and Vref\_time\_long, for  $n \geq 16$  steps. See Table 287 for details.

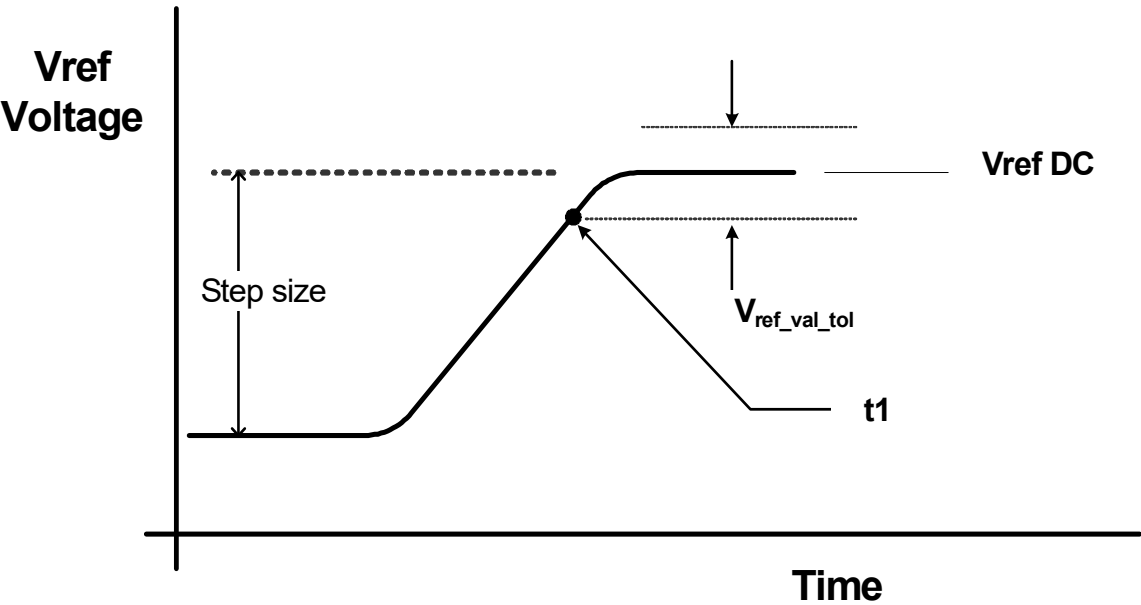


Figure 147 — Vref Step Single Step Size Increment Case

## 17.1 VrefDQ, VrefMDQ, and BVref Specifications (cont'd)

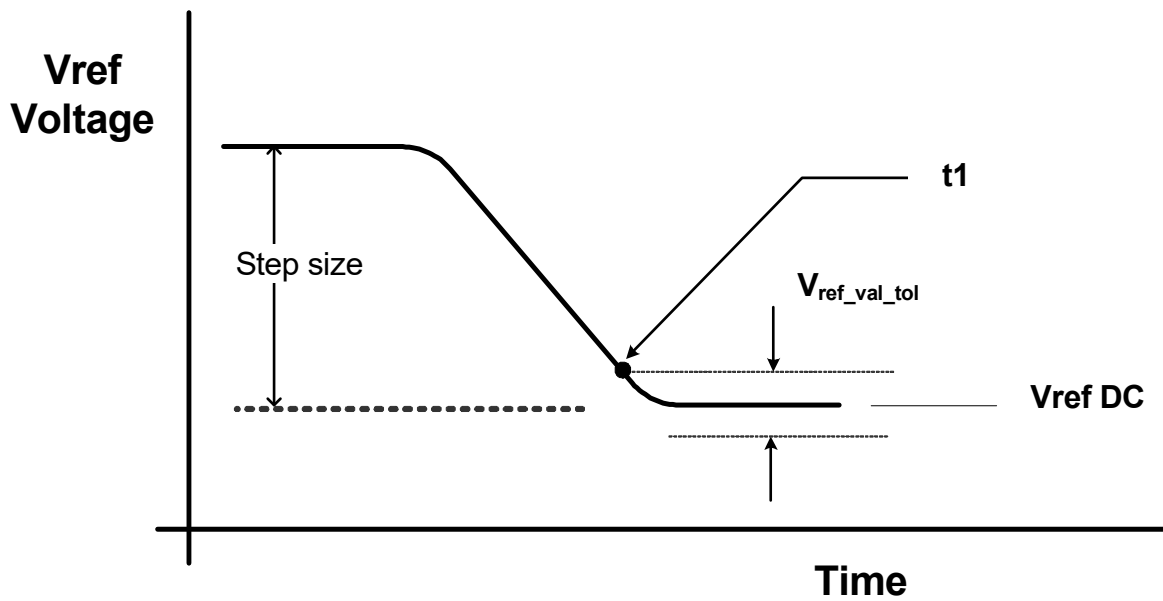


Figure 148 — Vref Step Single Step Size Decrement Case

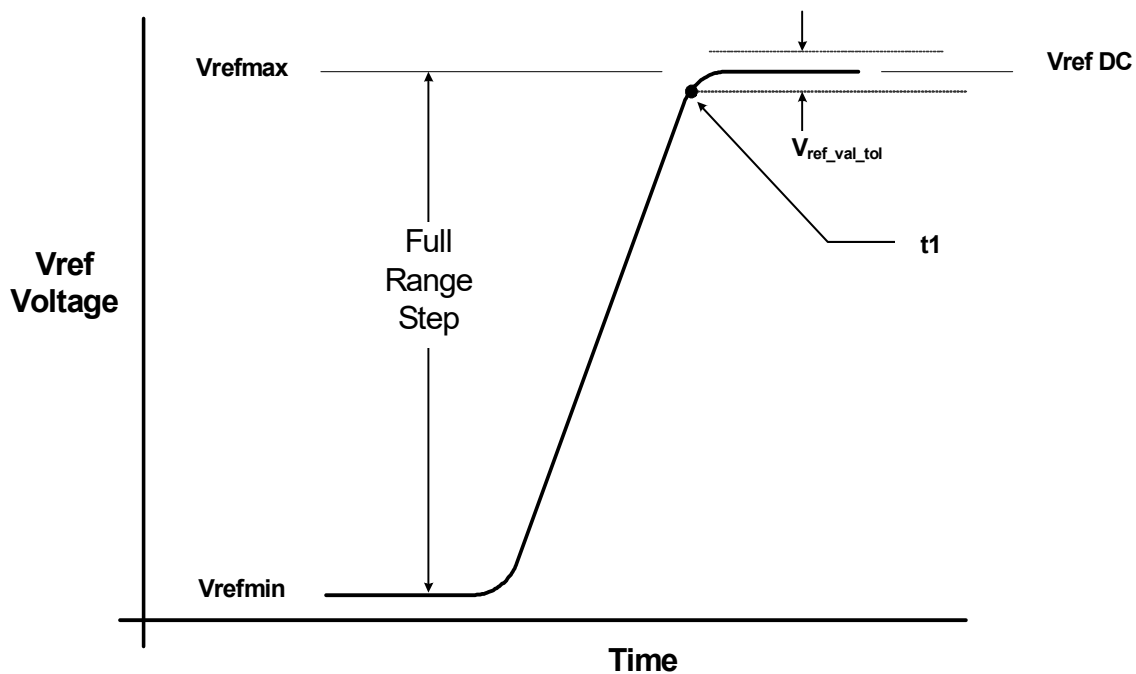


Figure 149 — Vref Full Step from Vrefmin to Vrefmax Case

### 17.1 VrefDQ, VrefMDQ, and BVref Specifications (cont'd)

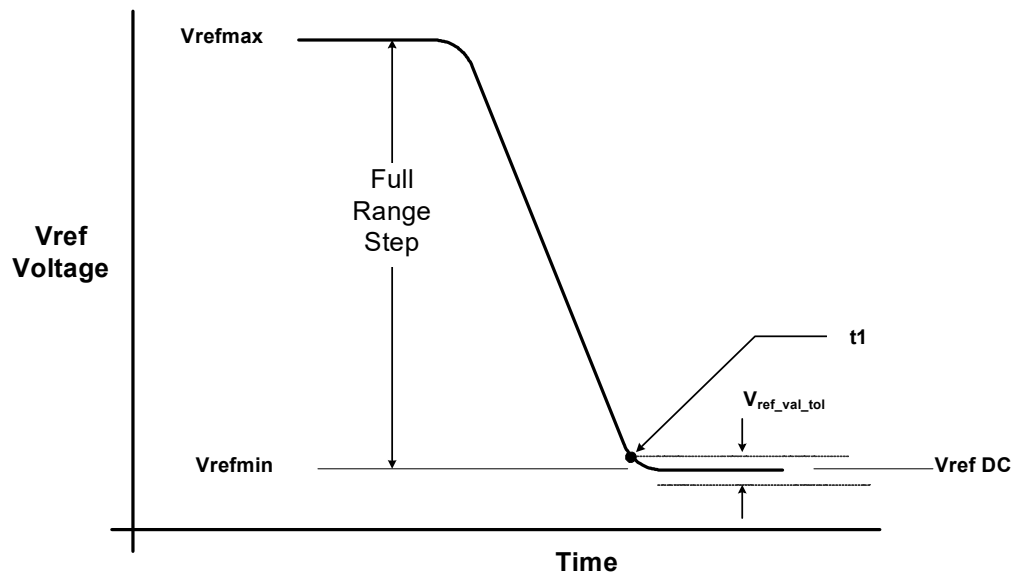


Figure 150 — Vref Full Step from Vrefmax to Vrefmin Case

Table 287 contains the internal Vref specifications that will be characterized at the component level for compliance. The characterization method is defined in a separate specification.

Table 287 — Internal Vref [M]DQ and BVref Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Vref Max Operating Point	Vref_max	97.5%	-	-	V <sub>DD</sub>	1
Vref Min Operating Point	Vref_min	-	-	35%	V <sub>DD</sub>	1
Vref Step size	Vref_step	0.41%	0.50%	0.59%	V <sub>DD</sub>	2, 10
Vref Set Tolerance	Vref_set_tol	-1.625%	0.0%	1.625%	V <sub>DD</sub>	3, 4, 6
	Vref_set_tol	-0.15%	0.0%	0.15%	V <sub>DD</sub>	3, 5, 7
Vref Step Time Short	Vref_time_short	-	-	150	ns	8, 11
Vref Step Time Long	Vref_time_long	-	-	500	ns	8, 11
Vref Valid Tolerance	Vref_val_tol	-0.15%	0.0%	0.15%	V <sub>DD</sub>	9

NOTE 1 Vref DC voltage referenced to VDD

NOTE 2 Vref step size increment/decrement range. Vref at DC level.

NOTE 3  $V_{ref\_new} = V_{ref\_old} + n \cdot V_{ref\_step}$ ; n= number of steps; if increment use "+"; If decrement use "-".

NOTE 4 The minimum value of Vref setting tolerance =  $V_{ref\_new} - 1.625\% \cdot V_{DD}$ . The maximum value of Vref setting tolerance =  $V_{ref\_new} + 1.625\% \cdot V_{DD}$ . For  $n \geq 4$ .

NOTE 5 The minimum value of Vref setting tolerance =  $V_{ref\_new} - 0.15\% \cdot V_{DD}$ . The maximum value of Vref setting tolerance =  $V_{ref\_new} + 0.15\% \cdot V_{DD}$ . For  $n < 4$ .

NOTE 6 Measured by recording the min and max values of the Vref output over the full range, drawing a straight line between those points and comparing all other Vref output settings to that line.

NOTE 7 Measured by recording the min and max values of the Vref output across 4 consecutive steps ( $n=4$ ), drawing a straight line between those points and comparing all other Vref output settings to that line.

NOTE 8 Time from MRW command updating Vref to increment or decrement.

NOTE 9 Only applicable for component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.

NOTE 10  $V_{ref\_step(avg)} = (V_{ref\_max} - V_{ref\_min}) / 125$ .

NOTE 11 The maximum value of Vref[M]DQ step time = 150 ns for  $n < 16$  and 500 ns for  $n \geq 16$ , where n = number of steps.

## 17.2 DFE\_Vref Tolerance

### 17.2.1 DFE\_Vref INL Tolerance

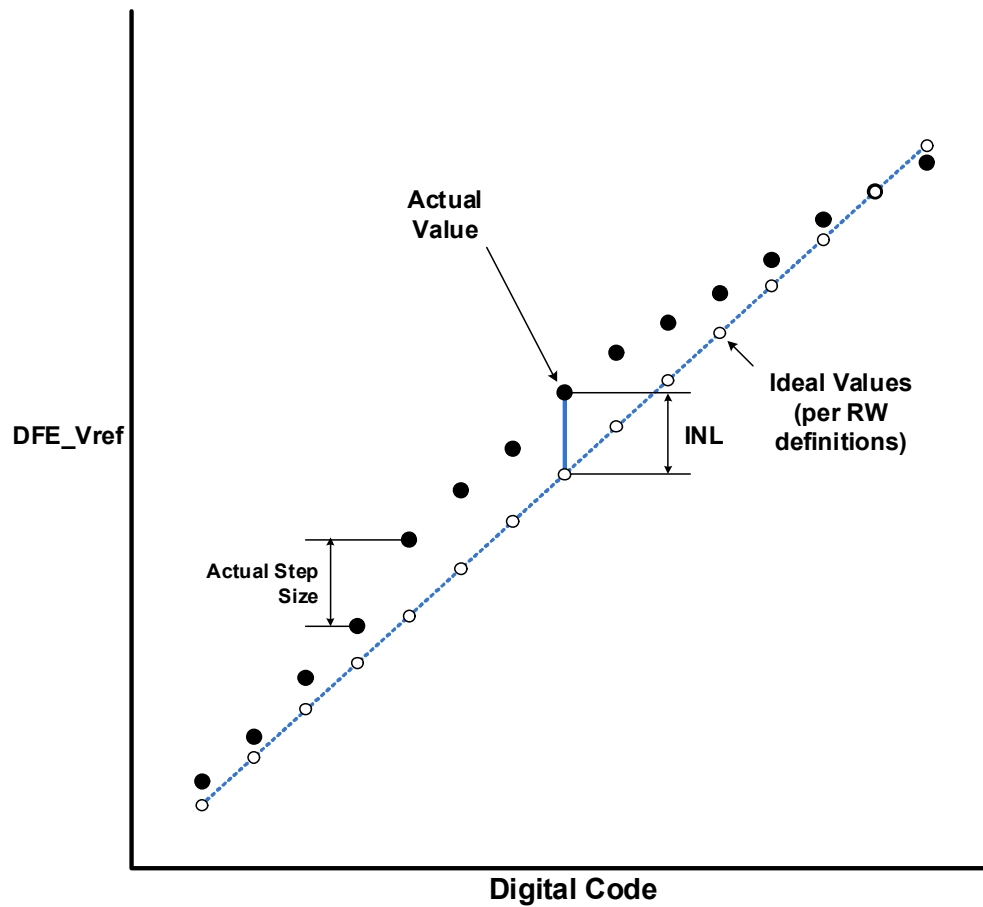


Figure 151 — Example of DFE\_Vref INL Tolerance

Integral nonlinearity (INL) is the deviation between effective analog values and expected ideal values for the corresponding settings in Receiver DFE\_Vref Control words as defined in [PG\[6\]RW\[E2, E6, EA, EE, F2, F6, FA, FE\]](#), and [PG\[6\]RW\[E3, E7, EB, EF, F3, F7, FB, FF\]](#).

17.2.1 DFE\_Vref INL Tolerance (cont'd)

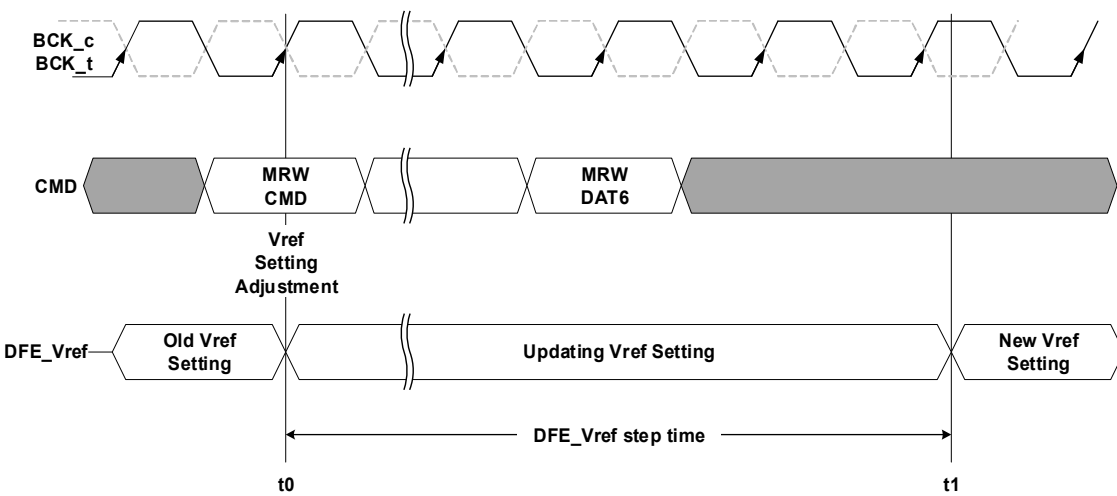


Figure 152 — DFE\_Vref Step Time Timing Diagram

An MRW write to the (Internal Vref Control Word) is used to program the Vref value.  
The minimum time required between two DFE\_Vref MRW commands is DFE\_Vref Step Time.

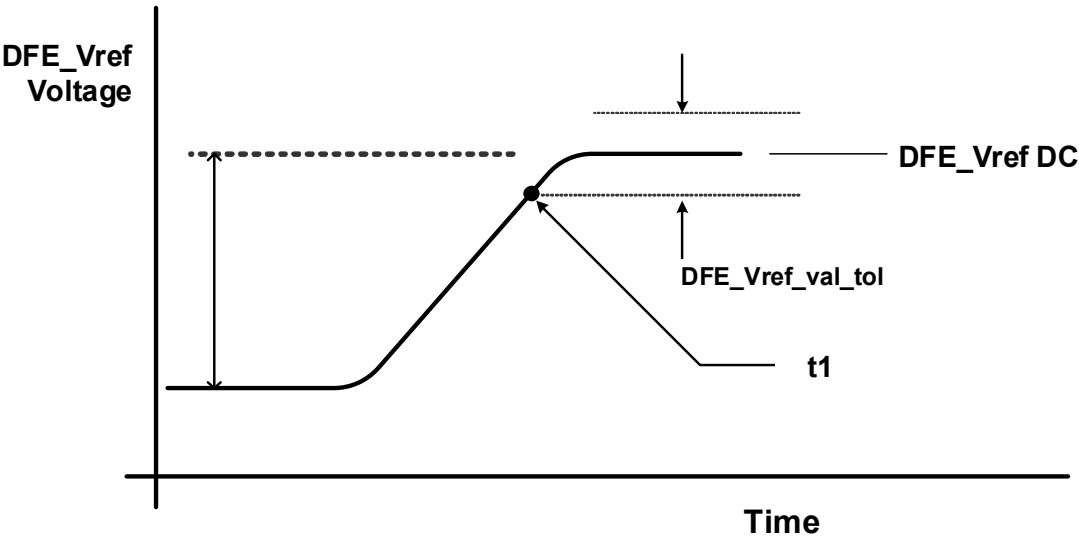


Figure 153 — DFE\_Vref Increment Case

## 17.2.1 DFE\_Vref INL Tolerance (cont'd)

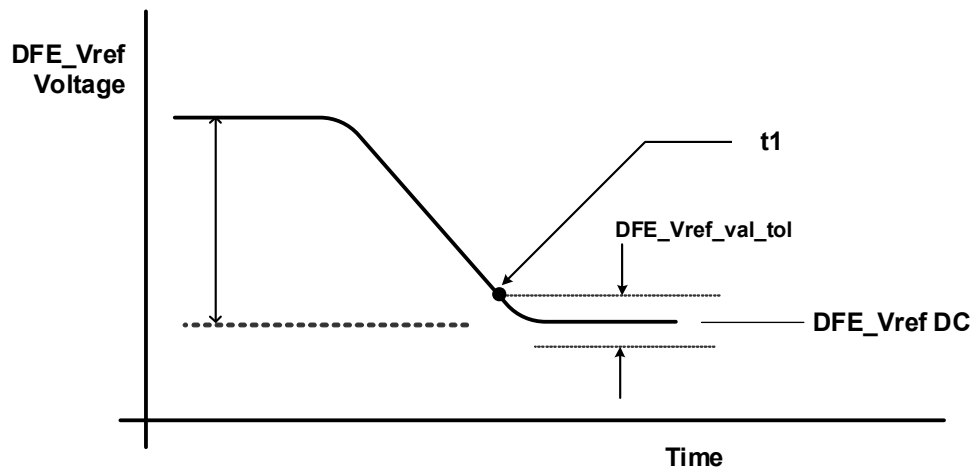


Figure 154 — DFE VREF Decrement Case

Table 288 contains the DFE Training Vref specifications that will be characterized at the component level for compliance. The characterization method is described in Clause 17.2.2.

Table 288 — DFE\_Vref Specification

Parameter	Symbol	Min	Typ	Max	Unit	Note
DFE_Vref Step Time Short	DFE_Vref_Short_16	-	-	200	ns	1, 2
	DFE_Vref_Short_32	-	-	300	ns	1, 3
DFE_Vref Step Time Long	DFE_Vref_Long	-	-	600	ns	1, 4
DFE_Vref Valid Tolerance	DFE_Vref_val_tol	- 1.65	0	1.65	mV	1

NOTE 1 Only applicable for component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is used to qualify the step times which will be characterized at the component level.

NOTE 2 The maximum value of DFE\_Vref step time = 200 ns for  $n < 16$ , where  $n$  = number of steps.

NOTE 3 The maximum value of DFE\_Vref step time = 300 ns for  $16 \leq n < 32$ , where  $n$  = number of steps.

NOTE 4 The maximum value of DFE\_Vref step time = 600 ns for  $n \geq 32$ , where  $n$  = number of steps.

Table 289 — DFE\_Vref INL Tolerance

Dfe_vref Setting	Lower Limit	Upper Limit	Note
- 500 mV ~ 300 mV	-	$V_{ideal} * 80\%$	1,3,4
- 300 mV ~ 0 mV	$\text{Min}(V_{ideal} * 120\%, V_{ideal} - 4 * \text{LSB})$	$\text{Max}(V_{ideal} * 80\%, V_{ideal} + 4 * \text{LSB})$	1,2,3,4
0 mV ~ + 300 mV	$\text{Min}(V_{ideal} * 80\%, V_{ideal} - 4 * \text{LSB})$	$\text{Max}(V_{ideal} * 120\%, V_{ideal} + 4 * \text{LSB})$	1,2,3,4
+300 mV ~ + 500 mV	$V_{ideal} * 80\%$	-	1,3,4

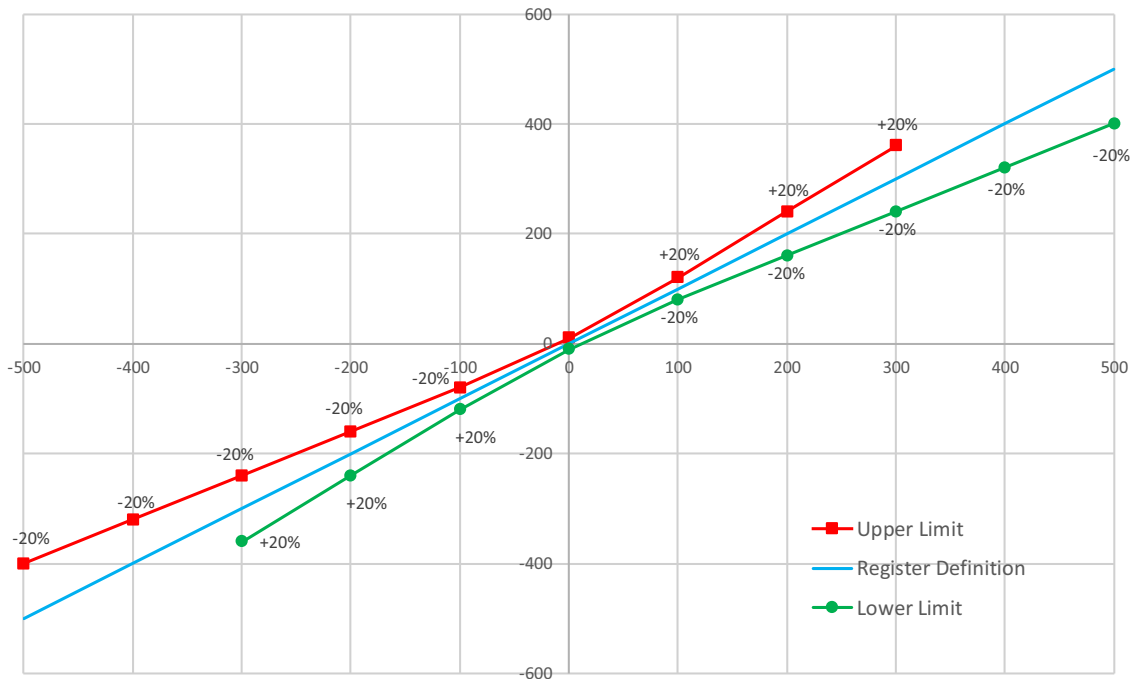
NOTE 1  $V_{ideal}$  refers to the ideal DFE\_Vref value based on the setting.

NOTE 2 LSB is 2.5 mV.

NOTE 3 DFE\_Vref must be monotonic.

NOTE 4 The range values specified in the table are applicable for default VrefDQ and DFE Gain Offset setting, under VDD = 1.1 V and 25 °C ambient temperature.

### 17.2.1 DFE\_Vref INL Tolerance (cont'd)



X axis = ideal control word setting value  
Y axis = actual implementation value

Note: The values shown in this diagram should be considered examples for reference only.

**Figure 155 — Illustration Example of DFE\_Vref INL Tolerance**

### 17.2.2 Measurement Steps

1. Make sure VrefDQ is at default setting, DFE\_Vref setting is 0, power supply is 1.1 V. Configure Margin Monitor [RWA1\[2:0\]](#) to 3'b001.
2. Sweep input signal from 1.1 V to 0 V to find the lowest level for HIGH and record this input signal HIGH level as V1 when HIGH-to-LOW transition starts.
3. Sweep input signal from 0 V to 1.1 V to find the highest level for LOW and record this input signal LOW level as V2 when LOW-to-HIGH transition starts.
4. Transition level  $V = (V1 + V2)/2$ .
5. Set DFE\_Vref, wait for DFE\_Vref Step Time to let the new setting settle.
6. Repeat steps 2 ~ 4, to get a new transition level V'.
7. Validate  $(V' - V)$  is within specification.
8. Repeat steps 2 ~ 7 until all the settings of DFE\_Vref are measured.

## 18 Input/Output Capacitance

### 18.1 I/O Capacitance Values

**Table 290 — Silicon Pad I/O Capacitance Values**

Symbol	Parameter	Conditions	DDR5-3200 to 12800 <sup>1</sup>		Unit
			Min	Max	
HIC <sub>IO</sub>	Host Interface Input/Output capacitance, DQ, DQS IOs	see footnote <sup>2,3</sup>	0	0.4 <sup>4</sup>	pF
DIC <sub>IO</sub>	DRAM Interface Input/Output capacitance, A(B)_MDQ, A(B)_MDQS IOs	see footnote <sup>2,5</sup>	0.3	0.7	pF
C <sub>IOD</sub>	Delta capacitance over all DQ IOs of each interface (i.e., within the DQ/DQS group or the A(B)_MDQ/A(B)_MDQS group)	see footnote <sup>2</sup>	-	0.1	pF
C <sub>DQSD</sub>	Delta capacitance between DQS_t and DQS_c (within each *DQS_t, *DQS_c pair), and between A(B)_MDQS_t and A(B)_MDQS_c (within each *MDQS_T, *MDQS_c pair)	see footnote <sup>2</sup>	-	0.04	pF
C <sub>I</sub>	Input capacitance, Control inputs	see footnote <sup>2,6</sup>	0.2	0.7	pF
C <sub>ID</sub>	Delta capacitance over all control inputs	see footnote <sup>2,6</sup>	-	0.4	pF
C <sub>CK</sub>	Input capacitance, BCK_t, BCK_c	see footnote <sup>2</sup>	0.2	0.7	pF
C <sub>CKD</sub>	Input capacitance delta BCK_t and BCK_c	see footnote <sup>2,7</sup>	-	0.04	pF
C <sub>OLB</sub>	Output capacitance LB	see footnote <sup>2</sup>	-	0.9	pF
C <sub>IR</sub>	Input Reset, BRST_n	see footnote <sup>2</sup>	-	3.0	pF

NOTE 1 DQ and DQS up to DDR5-12800. BCK, BCOM, BCS, MDQ, and MDQS up to DDR5-6400.

NOTE 2 This parameter does not include package capacitance.

NOTE 3 Data inputs are DQ[7:0], DQS[1:0]\_t, DQS[1:0]\_c,

NOTE 4 Effective pad CAP

NOTE 5 A(B)\_MDQ and A(B)\_MDQS pins

NOTE 6 BCOM[2:0], BCS.

NOTE 7 Absolute value BCK\_t - BCK\_c.



## 18.1 I/O Capacitance Values (cont'd)

**Table 291 — Package Electrical Specifications**

Symbol	Parameter	DDR5 3200 - 12800		Unit	Notes
		Min	Max		
Z <sub>I CTRL</sub>	Input CTRL pins Zpkg	30	60	Ω	1, 2, 4
Td <sub>I CTRL</sub>	Input CTRL pins Pkg Delay	5	25	ps	1, 3, 4
DTd <sub>I CTRL</sub>	Delta CTRL pins Pkg Delay	-	3	ps	1,3, 4
Z <sub>I DQS</sub>	Input/Output [M]DQS pins Zpkg	30	55	Ω	1, 2, 5
Td <sub>DQS</sub>	Input/Output [M]DQS pins Pkg Delay	5	30	ps	1, 3, 5
DZ <sub>DQS</sub>	Delta [M]DQS pins Zpkg (within each *DQS_t, *DQS_c pair)	-	2	Ω	1, 2, 5
DTd <sub>DQS</sub>	Delta [M]DQS pins Pkg Delay (within each *DQS_t, *DQS_c pair)	-	1	ps	1, 3, 5
Z <sub>I DQ</sub>	Input/Output [M]DQ pins Zpkg	30	55	Ω	1, 2, 5
Td <sub>DQ</sub>	Input/Output [M]DQ pins Pkg Delay	5	30	ps	1, 3, 5
DZ <sub>DQ</sub>	Delta [M]DQ pins Zpkg (for each [M]DQ nibble)	-	3	Ω	1, 2, 5
DTd <sub>DQ</sub>	Delta [M]DQ pins Pkg Delay for all pins within the same interface (i.e., Host Side or DRAM Side)	-	4	ps	1, 3, 5
Z <sub>CK</sub>	Input BCK pins ZPkg	30	60	Ω	1, 2, 8
Td <sub>CK</sub>	Input BCK pins Pkg Delay	5	25	ps	1, 3
DZ <sub>BCK</sub>	Delta Zpkg BCK_t and BCK_c	-	2	Ω	1, 2, 6
DTd <sub>BCK</sub>	Delta Delay BCK_t and BCK_c	-	1	ps	1,3,7
Z <sub>O ZQ</sub>	Output ZQCAL Zpkg	20	70	Ω	1, 2
Z <sub>I LB</sub>	Output Loopback pins Zpkg	30	60	Ω	1, 2, 9
Td <sub>I LB</sub>	Output Loopback pins Pkg Delay	5	25	ps	1, 3, 9
DTd <sub>I LB</sub>	Delta Loopback pins Pkg Delay	-	1	ps	1, 3, 9

NOTE 1 DQ and DQS up to DDR5-12800. BCK, BCOM, BCS, MDQ, and MDQS up to DDR5-6400. This parameter is not subject to production test. It is verified by design and characterization.

NOTE 2 This parameter is measured by using vendor specific measurement methodology to calculate the average Zpkg\_xx over the interval Tpkg\_delay\_xx).

NOTE 3 This parameter is measured by using vendor specific measurement methodology.

NOTE 4 This value applies to BCOM[2:0], BCS.

NOTE 5 This value applies to DQ[7:0], DQS[1:0]\_t, DQS[1:0]\_c, A(B)\_MDQ[7:0], A(B)\_MDQS[1:0]\_t, and A(B)\_MDQS[1:0]\_c.

NOTE 6 Absolute value of ZCK\_t - ZCK\_c.

NOTE 7 Absolute value of TdBCK\_t - TdBCK\_c.

NOTE 8 Single-ended impedance.

NOTE 9 This value applies to LBTXDQ, LBTXDQS.

## 18.2 Electrostatic Discharge Sensitivity Characteristics

**Table 292 — Electrostatic Discharge Sensitivity Characteristics**

Parameter	Symbol	Min	Max	Unit	Notes
Human body model (HBM)	ESD <sub>HBM</sub>	1000	-	V	1, 2
Charged-device model (CDM)	ESD <sub>CDM</sub>	250	-	V	1, 3

NOTE 1 State-of-the-art basic ESD control measures have to be in place when handling devices.

NOTE 2 Refer to JEDEC / ESDA Joint Standard JS-001 for measurement procedures.

NOTE 3 Refer to ANSI / ESDA / JEDEC Joint Standard JS-002 f for measurement procedures.

## 18.3 EOS Requirement

**Table 293 — EOS Requirement<sup>1</sup>**

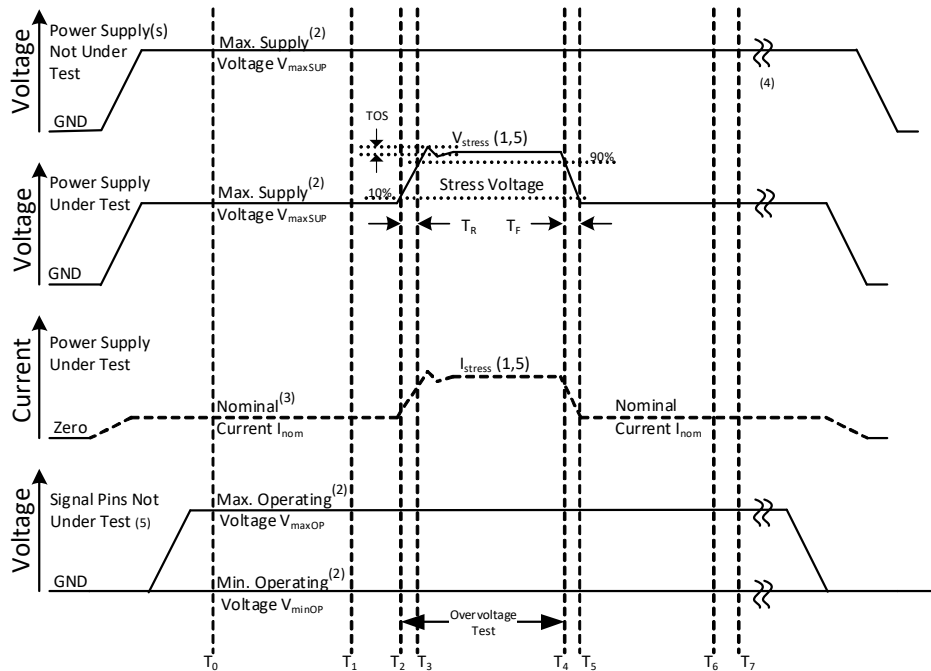
Pin	Maximum Stress Voltage	Maximum Stress Current	Stress Pulse Duration
VDD	12 V	3 A	10 ms

NOTE 1 During the stress, neither voltage nor current should exceed the specified maximum values.

NOTE: Refer to JESD78F.01 for measurement procedure. The following figures are references from JESD78F.01.

### 18.3 EOS Requirement (cont'd)

Figure 156 visualizes the waveform during the EOS test with the timing requirements defined in Table 294.



- NOTE 1 The waveforms when shown in a solid line are the forced voltages or currents and when shown in dashed lines are the measured voltages or currents.
- NOTE 2 During the Supply Test, the supply currents for all supply groups are monitored before and after the stress pulse. Latch-up occurs if any supply current meets the failure criteria shown in Table 3 of JESD78F.01.
- NOTE 3 The pre-stress and post-stress current  $I_{psPRE}$  and  $I_{psPOST}$  depend on the state and the circuitry of the  $V_{supply}$  pin (or pin group).
- NOTE 4 At the conclusion of the stress, returning all power supplies to ground is an option to reset the DUT. Resetting supplies is recommended for stability during testing.
- NOTE 5 Input pins Not Under Test shall be considered Signal Pins Not Under Test and should be controlled according to whether they are tied to  $V_{maxOP}$  or  $V_{minOP}$ . Output pins are not included and floated when not under test.
- NOTE 6 In this Supply Test example, the  $V_{Stress}$  reaches the intended Trigger Voltage of Table 293, and the  $I_{limit}$  is not reached. During the full waveform (including pre-stress, stress, and post-stress) the voltage is at set values, therefore, the full voltage waveform is a solid line. The current is being measured; thus the full current waveform is drawn as a dashed line.

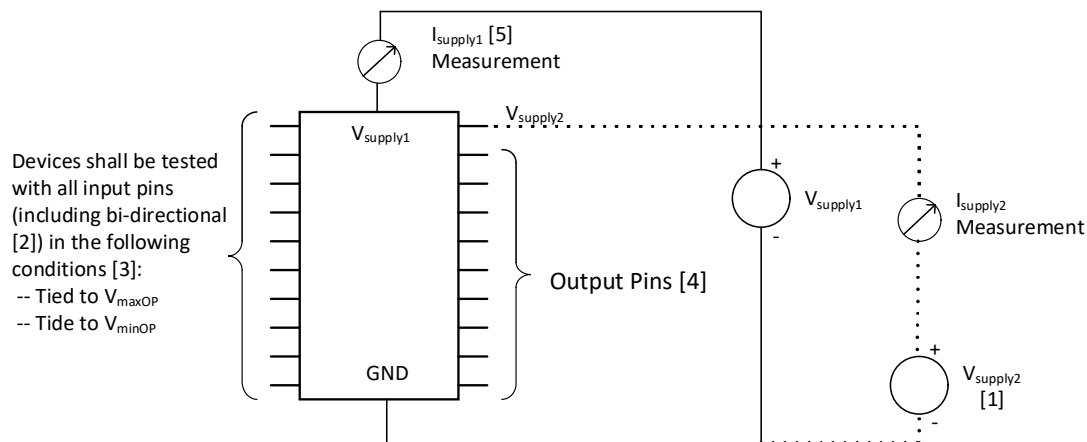
**Figure 156 — Test Waveform for Supply Test**

Note that  $V_{maxSUP}$ ,  $V_{maxOP}$  and  $V_{minOP}$  should refer to Table 253 for VDD voltage range.

### 18.3 EOS Requirement (cont'd)

**Table 294 — Timing Requirements**

Symbol	Time Interval	Parameter	Limits	
			Min	Max
$t_{wait}$	T0 to T1 T5 to T6	Wait time before measuring $I_{supply}$ . The wait time shall be sufficient to allow for power supply ramp up/down and stabilization of $I_{supply}$	3 ms	5 s
$t_{measure}$	T1 and T6	Measure $I_{supply}$	Measurement Point	
$t_r$	T2 to T3	Trigger rise time	87 $\mu$ s	5 ms
$t_{width}$	T3 to T4	Trigger duration	10 ms	
$t_f$	T4 to T5	Trigger fall time	87 $\mu$ s	5 ms
$t_{cool}$	T7 to Next Pulse	Cool down time		
TOS		Trigger over-shot	+/- 5% of pulse	



NOTE 1 DUT biasing includes additional  $V_{supply}$  sources as required.

NOTE 2 DUT is preconditioned so that all signal pins are placed in a valid state. Signal pins in the output state are open circuit.

NOTE 3  $V_{maxOP}$  and  $V_{minOP}$  shall be per the device specification. When bias levels are used with respect to a non-digital device, it means the maximum high ( $V_{maxOP}$ ) or minimum low ( $V_{minOP}$ ) voltage that can be supplied to the pin per the device specifications, unless these conditions violate device setup condition requirements.

NOTE 4 Output pins are open circuit.

NOTE 5 The trigger test condition is defined in Figure 156 and Table 294.

**Figure 157 — Equivalent Circuit for Supply Test**

## 19 Test Circuits

### 19.1 Parameter Measurement Information

All input pulses are supplied by generators having the following characteristics:  $1400 \text{ MHz} \leq \text{PRR}$  (Pulse Repetition Rate)  $\leq 3240 \text{ MHz}$ ;  $Z_o = 50 \Omega$ ; input slew rate =  $1 \text{ V/ns} \pm 20\%$ , unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.

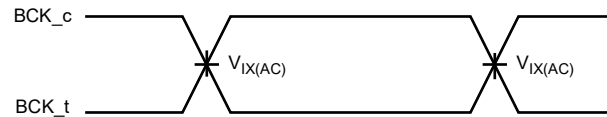
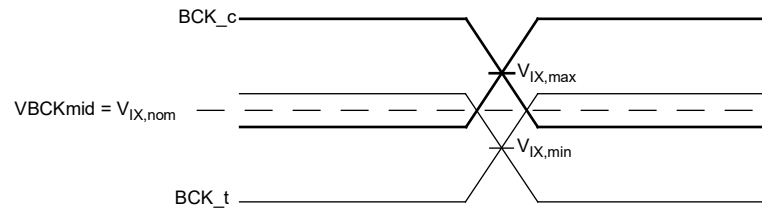


Figure 158 — Voltage Waveforms; Input Clock



For  $V_{IX}$  Range testing common mode voltage of BCK\_t and BCK\_c is shifted around  $V_{DD}/2$ . Functional Tests are performed with this  $V_{IX}$  shift.

Figure 159 — Input Waveforms  $V_{IX}$  Range Measurement

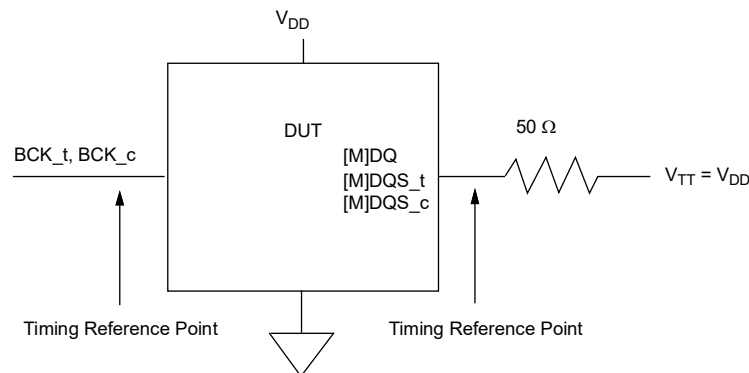


Figure 160 — Reference Load for Output Timing and Output Slew Rate

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## 20 IDD Measurement Conditions

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### 20.1 IDD Specification Parameters and Test Conditions

In this section, IDD measurement conditions, such as test load and patterns, are defined. Figure 161 shows the setup and test load for IDD measurements.

- IDD currents are measured as time-averaged currents with all  $V_{DD}$  balls of the DDR5MDB02 under test tied together.
- IDD currents can be measured for each speed bin. Each measurement shall use the minimum tCK (avg) for each speed bin as specified in Table 246.
- **ATTENTION:** IDD values cannot be directly used to calculate IO power of the DDR5MDB02. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 162.

For IDD measurements, the following definitions apply:

- “0” and “LOW” is defined as  $V_{IN} \leq V_{IL(AC).max}$ .
- “1” and “HIGH” is defined as  $V_{IN} \geq V_{IH(AC).min}$ .
- Basic IDD Measurement Conditions are described in Table 295.
- Detailed IDD Measurement-Loop Patterns are described in Table 296 through Table 306.
- IDD Measurements are done after properly initializing the DDR5MDB02 in the Mux mode. This includes but is not limited to setting the following:
  - Host interface DQS\_RTT\_PARK =  $R_{ZQ}/7$  (34  $\Omega$  in [RW86](#));
  - Host Interface DQ\_RTT\_PARK =  $R_{ZQ}/7$  (34  $\Omega$  in [RW87](#));
  - Host interface RON Pull-up and RON Pull-down =  $R_{ZQ}/7$  (34  $\Omega$  in [RW8A](#) and [PG\[70\]RWE2](#));
  - DRAM interface MDQS\_RTT\_PARK and MDQ\_RTT\_PARK =  $R_{ZQ}/5$  (48  $\Omega$  in [RW8C](#));
  - DRAM interface RON Pull-up and RON Pull-down =  $R_{ZQ}/7$  (34  $\Omega$  in [RW8B](#) and [PG\[70\]RWE3](#));
  - Host interface DQ/DQS and DRAM interface DQ/DQS drivers enabled in [RW8A](#) and [RW8B](#), respectively;
  - Fixed burst length = 16(Fixed) in [PG\[8\]RWE0](#);
  - Write and Read CRC disabled in [PG\[8\]RWE8](#);
  - Read preamble = 3 cycles and Write Preamble = 3 cycles in [PG\[8\]RWE1](#) and [PG\[8\]RWED](#);
  - Read post-amble = 1/2 cycle and Write post-amble = 1/2 cycle in [PG\[8\]RWE1](#) and [PG\[8\]RWED](#).
- **ATTENTION:** The IDD Measurement-Loop Patterns need to be executed at least one time before actual IDD measurement is started.

20.1 IDD Specification Parameters and Test Conditions (cont'd)

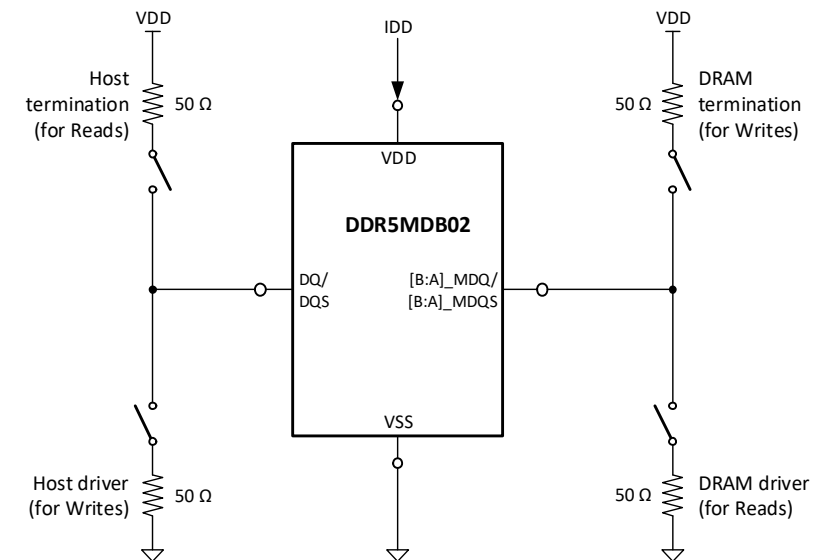


Figure 161 — Measurement Setup and Test Load for IDD Measurements

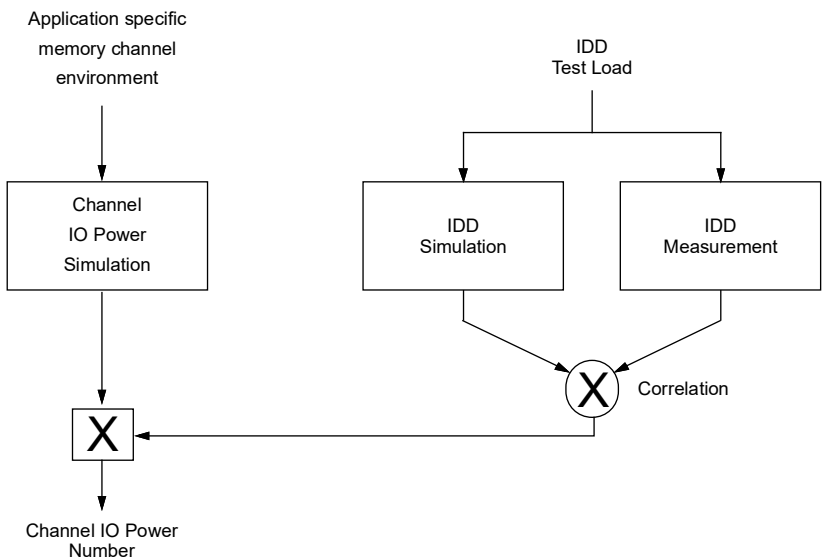


Figure 162 — Correlation from Simulated Channel IO Power to Actual Channel IO Power Supported by IDD Measurement

**20.1 IDD Specification Parameters and Test Conditions (cont'd)****Table 295 — Basic IDD Measurement Conditions**

Symbol	Description	Conditions
IDD3N1	Active Idle Current with 50% LOW / 50% HIGH Host Side Data Pattern Details: see Table 296	External Clock: On; Host interface ODT: DQS_RTT_PARK = 34 $\Omega$ , DQ_RTT_PARK = 34 $\Omega$ .
IDD3N2	Active Idle Current with 100% LOW Host Side Data Pattern Details: see Table 297	
IDD3N3	Active Idle Current with 100% HIGH Host Side Data Pattern Details: see Table 298	
IDD4R1	Operating Burst Read Current with 84% utilization and 50% LOW / 50% HIGH Host Side Data Data IO: Seamless READ data burst with different data between one burst and the next one according to Table 299 Pattern Details: see Table 299	External clock: On; BL: 16; Host interface Output Buffer: RON = 34 $\Omega$ ; DRAM drive strength: Ron = 50 $\Omega$ ; DRAM interface ODT: MDQS_RTT_PARK = 48 $\Omega$ , MDQ_RTT_PARK = 48 $\Omega$ .
IDD4R2	Operating Burst Read Current with 25% utilization and 50% LOW / 50% HIGH Host Side Data Pattern Conditions: see Table 300 Pattern Details: see Table 300	
IDD4R3	Operating Burst Read Current with 84% utilization and 100% LOW Host Side Data Pattern Details: see Table 301	
IDD4R4	Operating Burst Read Current with 25% utilization and 100% LOW Host Side Data Pattern Details: see Table 302	
IDD4W1	Operating Burst Write Current with 84% utilization and 50% LOW / 50% HIGH Host Side Data Data IO: Seamless WRITE data burst with different data between one burst and the next one according to Table 303 Pattern Details: see Table 303	External clock: On; BL: 16; Host drive strength: Ron = 50 $\Omega$ ; Host interface ODT: RTT_PARK = 60 $\Omega$ ; DRAM interface Output Buffer: RON = 34 $\Omega$ ; DRAM ODT: RTT_WR = 50 $\Omega$ .
IDD4W2	Operating Burst Write Current with 25% utilization and 50% LOW / 50% HIGH Host Side Data Pattern Details: see Table 304	
IDD4W3	Operating Burst Write Current with 84% utilization and 100% LOW Host Side Data Pattern Details: see Table 305	
IDD4W4	Operating Burst Write Current with 25% utilization and 100% LOW Host Side Data Pattern Details: see Table 306	
IDD6R	Static Reset Current Host Side Data IO: V <sub>DD</sub>	External clock: Off; BCK_t and BCK_c: HIGH.
IDD6S	Self Refresh with Clock Stop Power Down Current Data IO: V <sub>DD</sub>	



## 20.1 IDD Specification Parameters and Test Conditions (cont'd)

Table 296 — IDD3N1 Measurement-Loop Pattern

BCK_t, BCK_c	Sub-Loop	tBCK Cycle Number	BCS_n	BCOM	Host Side Data <sup>1</sup>
Toggling	0	0	Static HIGH	111 (DES)	D0=00, D1=FF, D2=FF, D3=00 D4=FF, D5=FF, D6=FF, D7=FF D8=00, D9=FF, D10=00, D11=00 D12=FF, D13=00, D14=00, D15=00 D16=00, D17=FF, D18=FF, D19=00 D20=FF, D21=FF, D22=FF, D23=FF D24=00, D25=FF, D26=00, D27=00 D28=FF, D29=00, D30=00, D31=00
		1		111 (DES)	-
		2		111 (DES)	-
		3		111 (DES)	-
		4		111 (DES)	-
		5		111 (DES)	-
		6		111 (DES)	-
		7		111 (DES)	-
	1	8		111 (DES)	D0=00, D1=FF, D2=FF, D3=00 D4=FF, D5=FF, D6=FF, D7=FF D8=00, D9=FF, D10=00, D11=00 D12=FF, D13=00, D14=00, D15=00 D16=00, D17=FF, D18=FF, D19=00 D20=FF, D21=FF, D22=FF, D23=FF D24=00, D25=FF, D26=00, D27=00 D28=FF, D29=00, D30=00, D31=00
		9		111 (DES)	-
		10		111 (DES)	-
		11		111 (DES)	-
		12		111 (DES)	-
		13		111 (DES)	-
		14		111 (DES)	-
		15		111 (DES)	-

NOTE 1 DQS signals are driven HIGH, and DQ signals are driven HIGH or LOW by another bus agent according to specified burst sequence. MDQ and MDQS signals are V<sub>DD</sub>.

## 20.1 IDD Specification Parameters and Test Conditions (cont'd)

Table 297 — IDD3N2 Measurement-Loop Pattern

BCK_t, BCK_c	Sub-Loop	tBCK Cycle Number	BCS_n	BCOM	Host Side Data <sup>1</sup>
Toggling	0	0	Static HIGH	111 (DES)	D0=00, D1=00, D2=00, D3=00 D4=00, D5=00, D6=00, D7=00 D8=00, D9=00, D10=00, D11=00 D12=00, D13=00, D14=00, D15=00 D16=00, D17=00, D18=00, D19=00 D20=00, D21=00, D22=00, D23=00 D24=00, D25=00, D26=00, D27=00 D28=00, D29=00, D30=00, D31=00
		1		111 (DES)	-
		2		111 (DES)	-
		3		111 (DES)	-
		4		111 (DES)	-
		5		111 (DES)	-
		6		111 (DES)	-
		7		111 (DES)	-
	1	8		111 (DES)	D0=00, D1=00, D2=00, D3=00 D4=00, D5=00, D6=00, D7=00 D8=00, D9=00, D10=00, D11=00 D12=00, D13=00, D14=00, D15=00 D16=00, D17=00, D18=00, D19=00 D20=00, D21=00, D22=00, D23=00 D24=00, D25=00, D26=00, D27=00 D28=00, D29=00, D30=00, D31=00
		9		111 (DES)	-
		10		111 (DES)	-
		11		111 (DES)	-
		12		111 (DES)	-
		13		111 (DES)	-
		14		111 (DES)	-
		15		111 (DES)	-

NOTE 1 DQS signals are driven HIGH, and DQ signals are driven HIGH or LOW by another bus agent according to specified burst sequence. MDQ and MDQS signals are V<sub>DD</sub>.

## 20.1 IDD Specification Parameters and Test Conditions (cont'd)

Table 298 — IDD3N3 Measurement-Loop Pattern

BCK_t, BCK_c	Sub-Loop	tBCK Cycle Number	BCS_n	BCOM	Host Side Data <sup>1</sup>
Toggling	0	0	Static HIGH	111 (DES)	D0=FF, D1=FF, D2=FF, D3=FF D4=FF, D5=FF, D6=FF, D7=FF D8=FF, D9=FF, D10=FF, D11=FF D12=FF, D13=FF, D14=FF, D15=FF D16=FF, D17=FF, D18=FF, D19=FF D20=FF, D21=FF, D22=FF, D23=FF D24=FF, D25=FF, D26=FF, D27=FF D28=FF, D29=FF, D30=FF, D31=FF
		1		111 (DES)	-
		2		111 (DES)	-
		3		111 (DES)	-
		4		111 (DES)	-
		5		111 (DES)	-
		6		111 (DES)	-
		7		111 (DES)	-
	1	8		111 (DES)	D0=FF, D1=FF, D2=FF, D3=FF D4=FF, D5=FF, D6=FF, D7=FF D8=FF, D9=FF, D10=FF, D11=FF D12=FF, D13=FF, D14=FF, D15=FF D16=FF, D17=FF, D18=FF, D19=FF D20=FF, D21=FF, D22=FF, D23=FF D24=FF, D25=FF, D26=FF, D27=FF D28=FF, D29=FF, D30=FF, D31=FF
		9		111 (DES)	-
		10		111 (DES)	-
		11		111 (DES)	-
		12		111 (DES)	-
		13		111 (DES)	-
		14		111 (DES)	-
		15		111 (DES)	-

NOTE 1 DQS signals are driven HIGH, and DQ signals are driven HIGH or LOW by another bus agent according to specified burst sequence. MDQ and MDQS signals are V<sub>DD</sub>.

## 20.1 IDD Specification Parameters and Test Conditions (cont'd)

Table 299 — IDD4R1 - 84% Utilization Measurement-Loop Pattern<sup>1</sup>

BCK_t, BCK_c	Sub-Loop	tBCK Cycle Number	BCS_n	BCOM	DRAM Side Data <sup>2</sup>	
Toggling	0	0	0	001 (RD, Format 0)	PS0: D0=00, D1=FF, D2=FF, D3=FF D4=00, D5=00, D6=FF, D7=00 D8=00, D9=FF, D10=FF, D11=FF D12=00, D13=00, D14=FF, D15=00 PS1: D0=FF, D1=00, D2=FF, D3=FF D4=FF, D5=00, D6=00, D7=00 D8=FF, D9=00, D10=FF, D11=FF D12=FF, D13=00, D14=00, D15=00	
		1	1	010 (PS0, BL16, Rank 0)		
		2	0	011 (RD, Format 1)		
		3	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)		
		4-7	1	111 (DES)		
	1	8	0	001 (RD, Format 0)	PS0: D0=00, D1=FF, D2=FF, D3=FF D4=00, D5=00, D6=FF, D7=00 D8=00, D9=FF, D10=FF, D11=FF D12=00, D13=00, D14=FF, D15=00 PS1: D0=FF, D1=00, D2=FF, D3=FF D4=FF, D5=00, D6=00, D7=00 D8=FF, D9=00, D10=FF, D11=FF D12=FF, D13=00, D14=00, D15=00	
		9	1	010 (PS0, BL16, Rank 0)		
		10	0	011 (RD, Format 1)		
		11	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)		
		12-15	1	111 (DES)		
	2	16-31	-	repeat Sub-Loop 0 and 1		
	3	32-37	1	111 (DES)	All bursts HIGH	
	4	38-75	-	repeat Sub-Loops 0, 1, 2, and 3, using Rank 1 instead		

NOTE 1 [M]DQS0\_t, [M]DQS0\_c and [M]DQS1\_t, [M]DQS1\_c are used according to RD16 Commands.

NOTE 2 Burst Sequence received on each MDQ pin and driven on each DQ pin by RD16 Command.

## 20.1 IDD Specification Parameters and Test Conditions (cont'd)

Table 300 — IDD4R2 - 25% Utilization Measurement-Loop Pattern<sup>1</sup>

BCK_t, BCK_c	Sub-Loop	tBCK Cycle Number	BCS_n	BCOM	DRAM Side Data <sup>2</sup>
Toggling	0	0	0	001 (RD, Format 0)	PS0: D0=00, D1=FF, D2=FF, D3=FF D4=00, D5=00, D6=FF, D7=00 D8=00, D9=FF, D10=FF, D11=FF D12=00, D13=00, D14=FF, D15=00 PS1: D0=FF, D1=00, D2=FF, D3=FF D4=FF, D5=00, D6=00, D7=00 D8=FF, D9=00, D10=FF, D11=FF D12=FF, D13=00, D14=00, D15=00
		1	1	010 (PS0, BL16, Rank 0)	
		2	0	011 (RD, Format 1)	
		3	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)	
		4-7	1	111 (DES)	
		8-31	1	111 (DES)	
	1	32	0	001 (RD, Format 0)	PS0: D0=00, D1=FF, D2=FF, D3=FF D4=00, D5=00, D6=FF, D7=00 D8=00, D9=FF, D10=FF, D11=FF D12=00, D13=00, D14=FF, D15=00 PS1: D0=FF, D1=00, D2=FF, D3=FF D4=FF, D5=00, D6=00, D7=00 D8=FF, D9=00, D10=FF, D11=FF D12=FF, D13=00, D14=00, D15=00
		33	1	010 (PS0, BL16, Rank 0)	
		34	0	011 (RD, Format 1)	
		35	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)	
		36-39	1	111 (DES)	
		40-63	1	111 (DES)	
	2	64-95		repeat Sub-Loop 0, use Rank 1 instead	
	3	96-127		repeat Sub-Loop 1, use Rank 1 instead	

NOTE 1 [M]DQS0\_t, [M]DQS0\_c and [M]DQS1\_t, [M]DQS1\_c are used according to RD16 Commands, otherwise V<sub>DD</sub>.NOTE 2 Burst Sequence received on each MDQ pin and driven on each DQ pin by RD16 Command, otherwise V<sub>DD</sub>.

## 20.1 IDD Specification Parameters and Test Conditions (cont'd)

Table 301 — IDD4R3 - 84% Utilization Measurement-Loop Pattern<sup>1</sup>

BCK_t, BCK_c	Sub-Loop	tBCK Cycle Number	BCS_n	BCOM	DRAM Side Data <sup>2</sup>
Toggling	0	0	0	001 (RD, Format 0)	All PS0 and PS1 bursts LOW
		1	1	010 (PS0, BL16, Rank 0)	
		2	0	011 (RD, Format 1)	
		3	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)	
		4-7	1	111 (DES)	
	1	8	0	001 (RD, Format 0)	All PS0 and PS1 bursts LOW
		9	1	010 (PS0, BL16, Rank 0)	
		10	0	011 (RD, Format 1)	
		11	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)	
		12-15	1	111 (DES)	
	2	16-31	-	repeat Sub-Loop 0 and 1	
	3	32-37	1	111 (DES)	All bursts HIGH
	4	38-75	-	repeat Sub-Loops 0, 1, 2, and 3, using Rank 1 instead	

NOTE 1 [M]DQS0\_t, [M]DQS0\_c and [M]DQS1\_t, [M]DQS1\_c are used according to RD16 Commands.

NOTE 2 Burst Sequence received on each MDQ pin and driven on each DQ pin by RD16 Command.

## 20.1 IDD Specification Parameters and Test Conditions (cont'd)

Table 302 — IDD4R4 - 25% Utilization Measurement-Loop Pattern<sup>1</sup>

BCK_t, BCK_c	Sub-Loop	tBCK Cycle Number	BCS_n	BCOM	DRAM Side Data <sup>2</sup>
Toggling	0	0	0	001 (RD, Format 0)	All PS0 and PS1 bursts LOW
		1	1	010 (PS0, BL16, Rank 0)	
		2	0	011 (RD, Format 1)	
		3	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)	
		4-7	1	111 (DES)	
		8-31	1	111 (DES)	
	1	32	0	001 (RD, Format 0)	All PS0 and PS1 bursts LOW
		33	1	010 (PS0, BL16, Rank 0)	
		34	0	011 (RD, Format 1)	
		35	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)	
		36-39	1	111 (DES)	
		40-63	1	111 (DES)	
	2	64-95		repeat Sub-Loop 0, use Rank 1 instead	
	3	96-127		repeat Sub-Loop 1, use Rank 1 instead	

NOTE 1 [M]DQS0\_t, [M]DQS0\_c and [M]DQS1\_t, [M]DQS1\_c are used according to RD16 Commands, otherwise  $V_{DD}$ .

NOTE 2 Burst Sequence received on each MDQ pin and driven on each DQ pin by RD16 Command, otherwise  $V_{DD}$ .

## 20.1 IDD Specification Parameters and Test Conditions (cont'd)

Table 303 — IDD4W1 - 84% Utilization Measurement-Loop Pattern<sup>1</sup>

BCK_t, BCK_c	Sub-Loop	tBCK Cycle Number	BCS_n	BCOM	Data <sup>2</sup>	
Toggling	0	0	0	000 (WR, Format 0)	D0=00, D1=FF, D2=FF, D3=00 D4=FF, D5=FF, D6=FF, D7=FF D8=00, D9=FF, D10=00, D11=00 D12=FF, D13=00, D14=00, D15=00 D16=00, D17=FF, D18=FF, D19=00 D20=FF, D21=FF, D22=FF, D23=FF D24=00, D25=FF, D26=00, D27=00 D28=FF, D29=00, D30=00, D31=00	
		1	1	010 (PS0, BL16, Rank 0)		
		2	0	010 (WR, Format 1)		
		3	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)		
		4-7	1	111 (DES)		
	1	8	0	000 (WR, Format 0)	D0=00, D1=FF, D2=FF, D3=00 D4=FF, D5=FF, D6=FF, D7=FF D8=00, D9=FF, D10=00, D11=00 D12=FF, D13=00, D14=00, D15=00 D16=00, D17=FF, D18=FF, D19=00 D20=FF, D21=FF, D22=FF, D23=FF D24=00, D25=FF, D26=00, D27=00 D28=FF, D29=00, D30=00, D31=00	
		9	1	010 (PS0, BL16, Rank 0)		
		10	0	010 (WR, Format 1)		
		11	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)		
		12-15	1	111 (DES)		
	2	16-31	-	repeat Sub-Loop 0 and 1		
	3	32-37	1	111 (DES)	All bursts HIGH	
	4	38-75	-	repeat Sub-Loops 0, 1, 2, and 3, using Rank 1 instead		

NOTE 1 [M]DQS0\_t, [M]DQS0\_c and [M]DQS1\_t, [M]DQS1\_c are used according to WR16 Commands.

NOTE 2 Burst Sequence received on each DQ pin and driven on each MDQ pin by WR16 Command.



## 20.1 IDD Specification Parameters and Test Conditions (cont'd)

Table 304 — IDD4W2 - 25% Utilization Measurement-Loop Pattern<sup>1</sup>

BCK_t, BCK_c	Sub-Loop	tBCK Cycle Number	BCS_n	BCOM	Data <sup>2</sup>
Toggling	0	0	0	000 (WR, Format 0)	D0=00, D1=FF, D2=FF, D3=00
		1	1	010 (PS0, BL16, Rank 0)	D4=FF, D5=FF, D6=FF, D7=FF
		2	0	010 (WR, Format 1)	D8=00, D9=FF, D10=00, D11=00
		3	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)	D12=FF, D13=00, D14=00, D15=00
		4-7	1	111 (DES)	D16=00, D17=FF, D18=FF, D19=00
		8-31	1	111 (DES)	D20=FF, D21=FF, D22=FF, D23=FF
	1	32	0	000 (WR, Format 0)	D24=00, D25=FF, D26=00, D27=00
		33	1	010 (PS0, BL16, Rank 0)	D28=FF, D29=00, D30=00, D31=00
		34	0	010 (WR, Format 1)	All bursts HIGH
		35	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)	D0=00, D1=FF, D2=FF, D3=00
		36-39	1	111 (DES)	D4=FF, D5=FF, D6=FF, D7=FF
		40-63	1	111 (DES)	D8=00, D9=FF, D10=00, D11=00
	2	64-95		repeat Sub-Loop 0, use Rank 1 instead	D12=FF, D13=00, D14=00, D15=00
	3	96-127		repeat Sub-Loop 1, use Rank 1 instead	D16=00, D17=FF, D18=FF, D19=00

NOTE 1 [M]DQS0\_t, [M]DQS0\_c and [M]DQS1\_t, [M]DQS1\_c are used according to WR16 Commands, otherwise V<sub>DD</sub>.NOTE 2 Burst Sequence received on each DQ pin and driven on each MDQ pin by WR16 Command, otherwise V<sub>DD</sub>.

## 20.1 IDD Specification Parameters and Test Conditions (cont'd)

Table 305 — IDD4W3 - 84% Utilization Measurement-Loop Pattern<sup>1</sup>

BCK_t, BCK_c	Sub-Loop	tBCK Cycle Number	BCS_n	BCOM	Data <sup>2</sup>	
Toggling	0	0	0	000 (WR, Format 0)	All PS0 and PS1 bursts LOW	
		1	1	010 (PS0, BL16, Rank 0)		
		2	0	010 (WR, Format 1)		
		3	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)		
		4-7	1	111 (DES)		
	1	8	0	000 (WR, Format 0)	All PS0 and PS1 bursts LOW	
		9	1	010 (PS0, BL16, Rank 0)		
		10	0	010 (WR, Format 1)		
		11	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)		
		12-15	1	111 (DES)		
	2	16-31	-	repeat Sub-Loop 0 and 1		
	3	32-37	1	111 (DES)	All bursts HIGH	
	4	38-75	-	repeat Sub-Loops 0, 1, 2, and 3, using Rank 1 instead		

NOTE 1 [M]DQS0\_t, [M]DQS0\_c and [M]DQS1\_t, [M]DQS1\_c are used according to WR16 Commands.

NOTE 2 Burst Sequence received on each DQ pin and driven on each MDQ pin by WR16 Command.

## 20.1 IDD Specification Parameters and Test Conditions (cont'd)

Table 306 — IDD4W4 - 25% Utilization Measurement-Loop Pattern<sup>1</sup>

BCK_t, BCK_c	Sub-Loop	tBCK Cycle Number	BCS_n	BCOM	Data <sup>2</sup>
Toggling	0	0	0	000 (WR, Format 0)	All PS0 and PS1 bursts LOW
		1	1	010 (PS0, BL16, Rank 0)	
		2	0	010 (WR, Format 1)	
		3	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)	
		4-7	1	111 (DES)	
		8-31	1	111 (DES)	All bursts HIGH
	1	32	0	000 (WR, Format 0)	All PS0 and PS1 bursts LOW
		33	1	010 (PS0, BL16, Rank 0)	
		34	0	010 (WR, Format 1)	
		35	1	010 (PS1, -2 clock cycle delay, BL16, Rank 0)	
		36-39	1	111 (DES)	
		40-63	1	111 (DES)	All bursts HIGH
	2	64-95		repeat Sub-Loop 0, use Rank 1 instead	
	3	96-127		repeat Sub-Loop 1, use Rank 1 instead	

NOTE 1 [M]DQS0\_t, [M]DQS0\_c and [M]DQS1\_t, [M]DQS1\_c are used according to WR16 Commands, otherwise VDD.

NOTE 2 Burst Sequence received on each DQ pin and driven on each MDQ pin by WR16 Command, otherwise VDD.

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## 21 Normative References

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JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products*

JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices*

JESD21-C, *Configuration for Solid State Memories*

JESD8-11A, *Definition of Wide Range Non-terminated Logic*

JESD79-5, *DDR5 SDRAM*

JESD82-542, *DDR5MRCD02 Multiplexed Rank Registering Clock Driver*

MO-276, *Plastic Bottom Grid, Array Ball, 0.50 mm Pitch, Rectangular Family*

JS-001-2017, *Joint JEDEC/ESDA Standard for Electrostatic Discharge Sensitivity Test – Human Body Model (HBM) – Component Level*

JS-002-2018, *ANSI/ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level*



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**Standard Improvement Form****JEDEC JESD82-552**

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1. I recommend changes to the following:

☐ Requirement, clause number \_\_\_\_\_

☐ Test method number \_\_\_\_\_ Clause number \_\_\_\_\_

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other \_\_\_\_\_

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2. Recommendations for correction:


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3. Other suggestions for document improvement:


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